Description

The Reticon RT5601B is a monolithic CCD integrated circuit which can perform the bulk of the computation for a 512-point Discrete Fourier Transform. The computations are done in an analog, highly-parallel fashion and have accuracy comparable to a 13-bit FFT. No A/D conversion is needed, reducing external circuit requirements, cost, power consumption, and allowing continuous sampling rates of up to 10 MHz. In addition, the device automatically applies a Hanning window to minimize leakage effects.

The RT5601B is fabricated with N-buried-channel CCD technology and comes in a 22-pin DIP as shown in Figure 1. Package dimensions are shown in Figure 16.

Key Features

- Performs majority of operations necessary for a 512-point DFT
- Sampling rates from 4 kHz to 10 MHz
- No A/D conversion needed, simplifying circuit design
- Continuously-updated output data
- Dynamic range of 60 dB
- Input signals available in time-delayed form at auxiliary outputs

Typical Applications

- Portable instrumentation
- Fast, small, low-cost, low-power spectrum analysis
- Biomedical, geophysical, telecommunications, audio and speech analysis, radar
- Anywhere spectrum analysis is needed but full-digital methods are impractical or undesirable

Device Operation

The RT5601B makes use of the Chirp-Z Transform (CZT) algorithm to do a 512-point Discrete Fourier Transform. The CZT is a method of computing a DFT with convolutions. Some preprocessing and postprocessing is needed; this is done by external circuitry. Internally, the RT5601B uses the CCD split-electrode method to compute the convolution values. This is a very efficient and parallel method: a complete set of 512 DFT values is computed as fast as every 51.2 µsec. At this speed, the chip is performing over 20 billion analog multiply-and-add operations per second.

Figure 2 shows the RT5601B's place in a typical circuit. The preprocessing consists of analog multiplying and applying offsets. The postprocessing involves phase correction or other operations appropriate to the application. The final output of the circuit will be in analog sample-hold form. Due to the cyclic nature of the CZT, the output will continuously update itself every 512 sample periods.

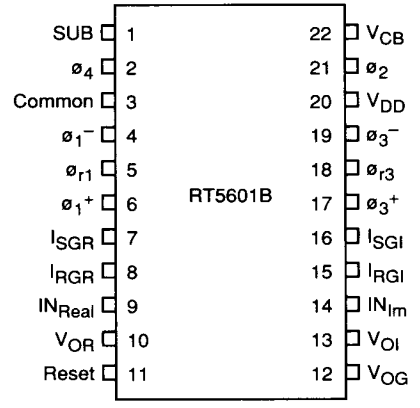

Figure 1. Pinout Configuration

The postprocessing determines whether the output values will represent complex frequencies or power spectrum information.

Basic Theory of the RT5601B

The RT5601B uses several concepts with which the average designer may not be familiar. Once these concepts are grasped, the behavior and requirements of the chip become straightforward.

The RT5601B uses the CCD split-electrode method to implement the Sliding Chirp Z-Transform (SCZT) algorithm for computing a 512-point DFT (Discrete Fourier Transform). A basic understanding of CCD operation can be had by consulting a text on solid-state physics and design. We will examine CCD split-electrodes and the SCZT here briefly.

CCD Operation of the RT5601B

The RT5601B is a four-phase CCD device, driven by clock waveforms ø1, ø2, ø3, ø4 (see Figure 5). The sampling gates (I_{SGR} and I_{SGI}) are driven by ø2; the receive gates (I_{RGR}, I_{RGI}) are driven by ø3.

As Figure 5 implies, there are two CCD channels, Real and Imaginary. Each has an auxilliary output stage with two N-channel MOSFETs. (Note: these are not the DFT-value outputs. These are extra outputs used for testing. The DFT value outputs will be explained shortly.) V_{OG} (output gate bias) allows the charge packets into the N+ diffusion at the end of each delay line. The MOSFET, with its gate connected to the diffusion, acts as a source-follower/output buffer, assuming that its source has an external pull-down resistor to bias it ON.

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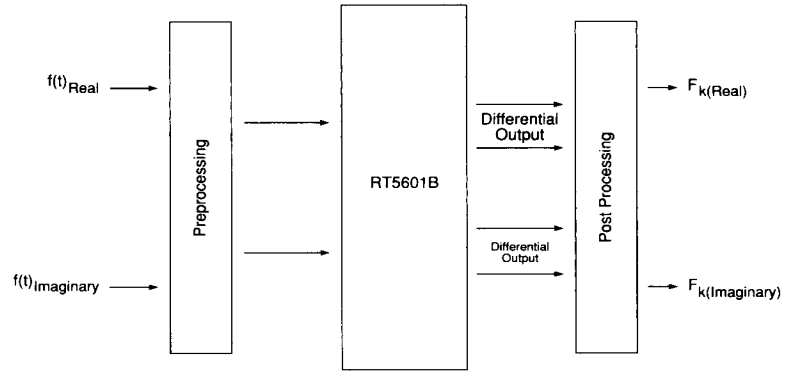
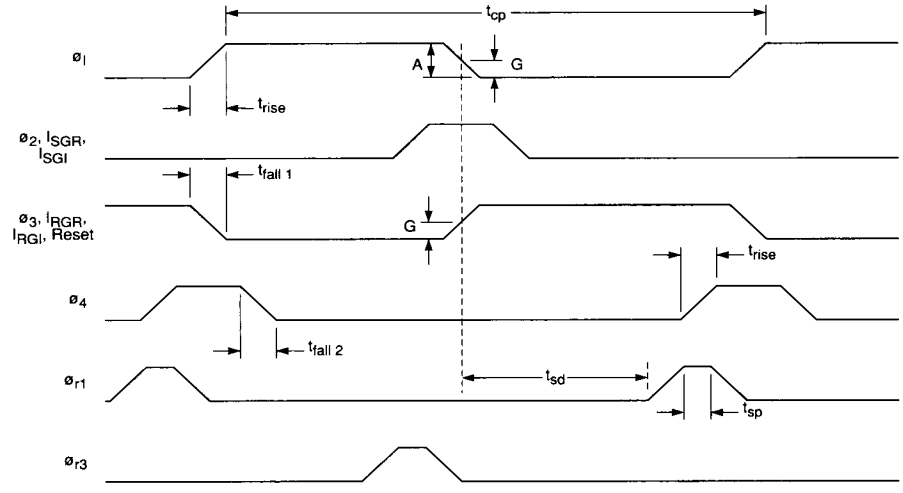


Figure 2. Block Diagram of RT5601B Circuit Application



General Timing Guidelines

1. Rise and fall times are applicable up to a clock frequency of 2 MHz and should be scaled appropriately for higher clock frequencies.
2. ø1 and ø3 have equal rise and fall times and duty cycles; ø2 and ø4 have equal rise and fall times and duty cycles.
3. ø1 and ø3 transition should cross at the midpoint (50%) or above, with ≤50 nsec overlap of ø1 and ø3 high levels.
4. ø2(ø4) should surround the ø1/ø3 crossing with substantial overlap each side, reducing to simple 4-phase clocking at high clock frequencies (not critical). ø2 and ø4 should not overlap.
5. ør1(ør3) rises and falls completely within ø1(ø3) low state, preferably during the latter half of the ø1(ø3) low state.

All time dimensions in nanoseconds t_{cp} = Length of clock period = $1/f_S$

$10 \le t_{rise} \le 50$
$50 \le t_{fall1} \le 100$
$10 \le t_{fall2} \le 50$
$A/2 \le G \le A$
$30 \le t_{sd} \le t_{cp}/8$
$100 \le t_{sp} \le t_{cp}/2$

Figure 3. Timing Diagram

Assume the N+ diffusion is at V_{DD} before the charge packet arrives. The MOSFET gate connected to it is also at V_{DD}, and so the source-follower/buffer is outputting V_{DD} minus the MOSFET's threshold voltage. When ϕ_3 falls and a charge packet is drawn into the diffusion, the gate voltage of the buffer falls an amount proportional to the size of the charge packet. The output of the buffer falls by the same amount. Then the RESET line goes high and charges the diffusion and buffer gate back to V_{DD} to prepare for the next charge packet.

The output of the buffers is thus a train of negative-going pulses whose amplitude envelope represents a sampled-and-delayed version of the input signal at the beginning of the CCD line. These delay-line outputs are typically only used during testing (proper operation of the delay line, DC bias, etc.). They require a pull-down resistor (to COM/Ground) of approximately 10KΩ to be biased ON.

CCD Split-Electrodes

If we view a simplified version of a CCD chip from the top, we get Figure 6a. If we top-view a CCD chip with a split electrode, we see Figure 6b.

Notice that each piece of the split electrode is connected to an external capacitor and then to a common clock (in this case, ϕ_1). This is in contrast to the unsplit electrodes that are directly connected to their clocks. This arrangement is necessary to use the split electrodes to sense charge as well as control it.

If this ϕ_1 clock were directly connected to the split electrode pieces, then the voltages at points A and B in Figure 6b would be exactly the same, and the split electrode would work as any other electrode. When we connect ϕ_1 to the split electrode via the external capacitors, a new result occurs: each piece of the

Data Bits \ Word #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0(ϕ_1)		|	|	|	|	|	|	|	|							
1(ϕ_2)								|	|	|	|					
2(ϕ_3)	|									|	|	|	|	|	|	|
3(ϕ_4)	|	|	|													|
4(ϕ_{r1})																|	|
5(ϕ_{r3})							|	|								
6($_{pulse}^{sync}$)												|				
7($_{used}^{not}$)																
Hex Value	OC	09	09	01	01	01	21	23	03	06	06	44	04	04	14	1C

The RT5601B clocking waveforms can be generated with an 8-bit ROM. An example ROM pattern is shown above. The ROM word address is clocked at 16 times the desired sample rate.

Figure 4. Example ROM Pattern for generating Timing Waveforms

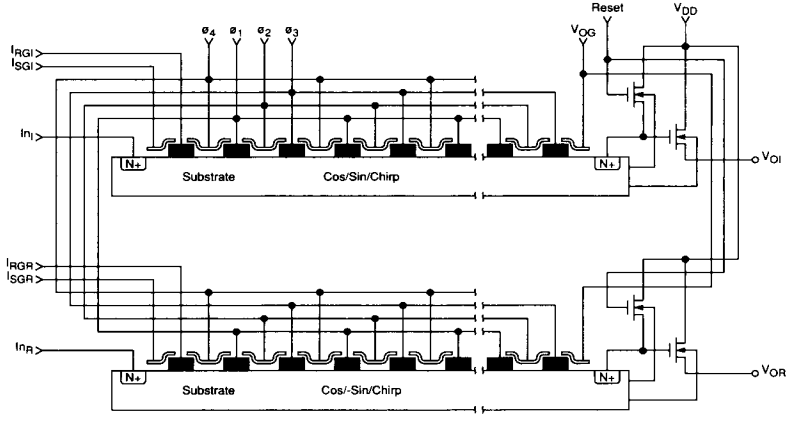


Figure 5. Schematic Layout of the CCD Channels, Edge View

split electrode acts like a capacitor and forms a capacitive voltage divider with its corresponding external capacitor. The two pieces of the electrode are not of the same length or area, so the voltages at A and B are no longer the same when a charge packet is below the electrode. The difference between V_A and V_B is proportional to the difference in electrode length and to the size of the charge packet underneath.

$$V_A - V_B = cTq$$

where c is a scaling constant dependent on fabrication, T (Tap weighting factor) is the relative length difference between electrode pieces, and q is the size of the charge packet beneath the split electrode. By measuring the difference V_A - V_B, we have performed an analog multiply operation on the charge packet—and on the analog input value it represents.

This is a nondestructive phenomenon, so we can have an entire series of split electrodes hundreds or thousands of stages long (see Figure 7). By connecting all the electrodes together on one side to one external capacitor, (C_1^+), and all the electrodes on the other side to the other external capacitor (C_1^-), V_A-V_B represents a summation of **all** the multiplications on **all** the charge packets. Ignoring the scaling constant c, we get

$$(V_A - V_B)_k = \sum_{n=0}^{N-1} q_{k-n} T_n$$

for an N-stage CCD line. Of course, the voltage difference is only valid when there are actually charge packets beneath the split electrodes—in effect, when the clock (ϕ_1) that drives the split electrodes is high. Also, all the split electrodes for a given summation must be driven by the same clock.

Figure 7 shows another extension of the split electrode method. We can interlace two or more series of split electrodes to get different summations on the same N samples. The arrangement shown will output one summation when ϕ_1 is high, and a completely different summation half a sample period later when ϕ_3 is high. The RT5601B uses this method on each of the two CCD channels. It performs four 512-term summations every sample period.

The form of the summation is consistent with convolution and correlation operations. All the terms in the summation are evaluated simply and simultaneously, and the accuracy of the results remains the same no matter how many points are used. Many-point signal processing involving convolution and correlation can be accomplished with truly significant improvements in speed, simplicity, and accuracy.

The Sliding Chirp Z-Transform (SCZT) Algorithm

The RT5601B split electrodes implement a variation of the Chirp Z-Transform (CZT) algorithm called the Sliding CZT, or SCZT. The CZT is used because it performs a DFT using a convolution operation, allowing us to take advantage of the powerful CCD split-electrode method.

The DFT is defined as

$$F_k = \sum_{n=0}^{N-1} f_n e^{-i\pi 2nk/N} \qquad k = 0, 1, 2, \cdots, N-1$$

If we notice that $2nk = n^2 + k^2 - (k - n)^2$,

then substituting gives

$$F_k = e^{-i\pi k^2/N} \sum_{n=0}^{N-1} \left(f_n e^{-i\pi n^2/N}\right) e^{i\pi(k-n)^2/N}$$

$$k = 0, 1, 2, \cdots, N-1$$

This is the standard CZT. Notice that it involves a premultiply of the samples, then a convolution of the weighted samples, and a postmultiply of the summation result. Since it is merely a rewriting of the DFT, it gives exactly the same results. It derives all N of the F_K from the same set of N samples.

The Sliding CZT is a variation well-suited for split-electrode CCDs. The formula for it is

$$F_k = e^{-i\pi k^2/N} \sum_{n=0}^{N-1} \left[\left(f_{k-n} e^{-i\pi(k-n)^2/N}\right) e^{i\pi n^2/N}\right]$$

$$k = 0, 1, \cdots, N-1$$

The last term in the brackets represents the tap weights and demonstrates why two channels are needed: to handle the real part and imaginary part of the computation.

The RT5601B (for which N = 512) carries the SCZT variation one step farther by shifting the tap weights and introducing a window factor into the tap weights:

$$F_k = e^{-i\pi k^2/512} \sum_{n=0}^{N-1} \left[\left(f_{k-n} e^{-i\pi(k-n)^2/512}\right)\left(\omega_n e^{i\pi(n-257)^2/512}\right)\right]$$

$$k = -255, -254, \ldots, -1, 0, 1, \ldots, 255, 256$$

W_n represents the windowing of the tap weights with a Hanning window:

$$W_n = \frac{1}{2} - \frac{1}{2}\cos\left(\frac{2\pi(n-1)}{511}\right)$$

This tap weighting reduces the effects of leakage in the frequency domain. The shifting of the tap weights reduces errors due to transfer inefficiency inherent in CCD operations.

The F_k are calculated with the convolution weights constant and the samples "sliding through" the sequence of tap weights. The outputs are not valid until at least 512 samples have been taken, and then each F_k comes from a different set of 512 samples. F_{-255} will come from samples f_0 through f_{511}, F_{-254} will come from f_1 through f_{512}, and so on. After F_{256} is reached, F_{-255} is output the very next sample period and the cycle begins anew. Each F_k comes from the latest 512 samples.

This is shown more clearly (albeit simplistically) in Figure 8, where we let N = 4. The output is not yet valid in (a) because the CCD line is not full yet. The line is full in (b) and we get our first value, F_0, using samples f_0 through f_3. In (c) we get F_1, using samples f_1 through f_4. F_2 will use f_2 through f_5, F_3 will use f_3 through f_6. 8(d) shows that the next output is F_0 again, using f_4

through f_7, so this is a new, updated value of F_0 using the latest data. The cycle continues, each F_K being updated every N sample periods.

We are effectively extracting one DFT value from each of a series of overlapping time records. This continuous update is valid processing, but does give different results from a standard DFT/FFT, which uses the same set of samples for all N F_K.

As mentioned before, Figure 8 is extremely simplified. It leaves out the other electrodes, the premultiply, the postmultiply, the tap weight shift, and the fact that parallel CCD channels are needed to handle the real and imaginary parts of the complex quantities involved.

We determine the timing for the F_K from the preprocessing function (which also fixes the postprocessing timing). The preprocessing exponential is nonperiodic in the continuous-time domain, but aliasing makes it periodic in the sampled-time domain. Its period is N sample periods (N = 512 for the RT5601B). F_0 comes out 256 periods after the exponential frequency passes through zero. These "zero/DC" points correspond to when the continuous-time exponential would be at integer multiples of the sampling frequency.

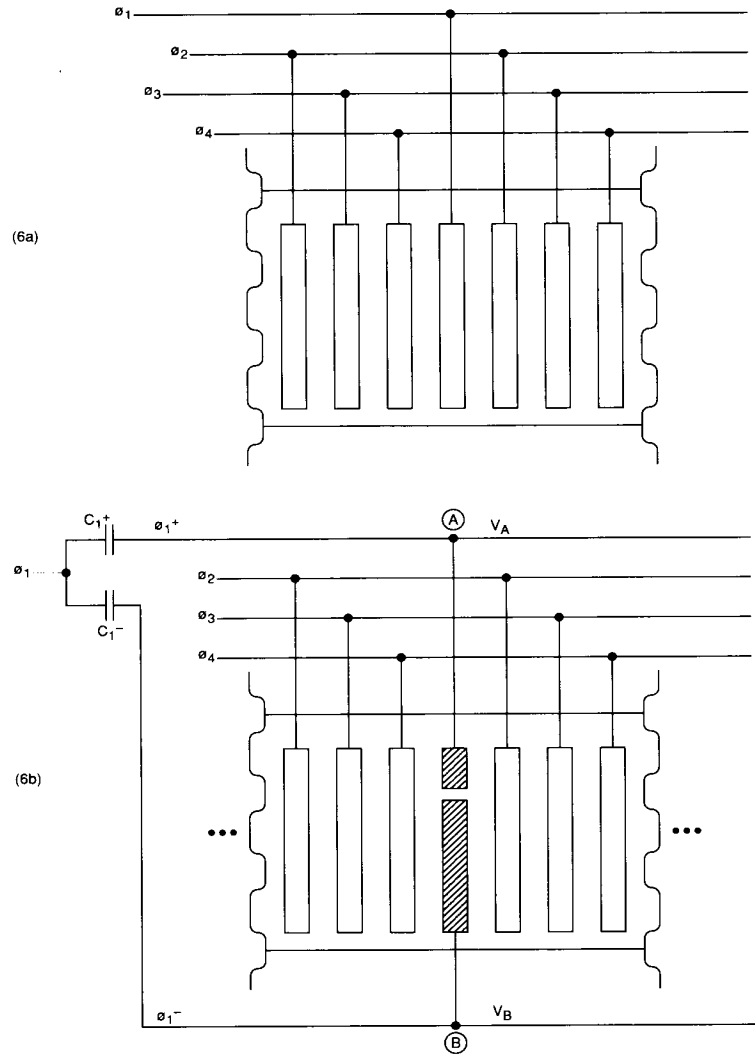


Figure 6. Top View of Normal and Split-electrode CCD

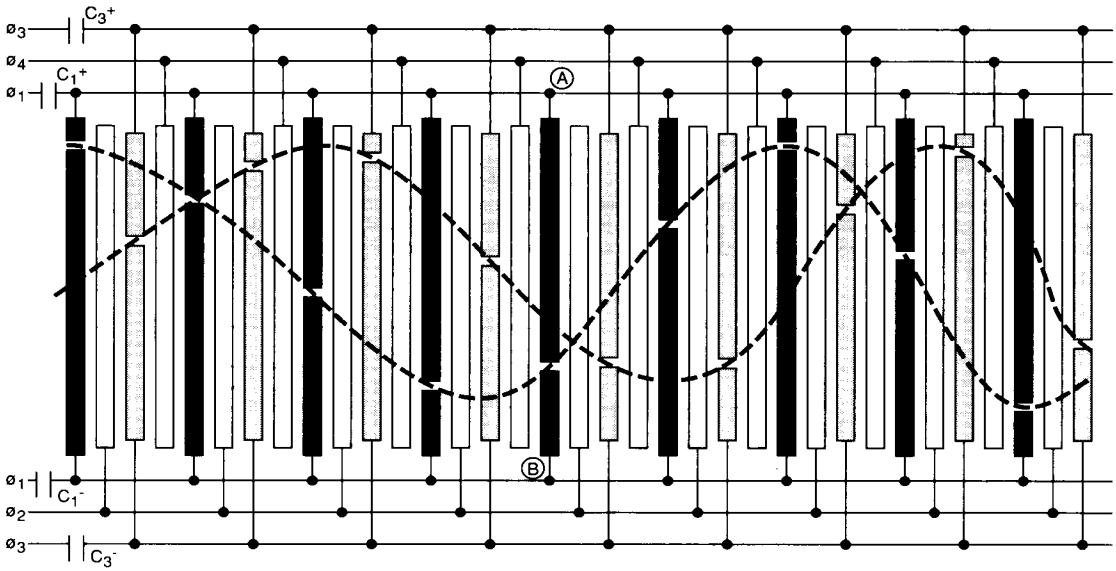


Figure 7. Schematic Layout of the CCD Gates Showing the Split-gate Weighting

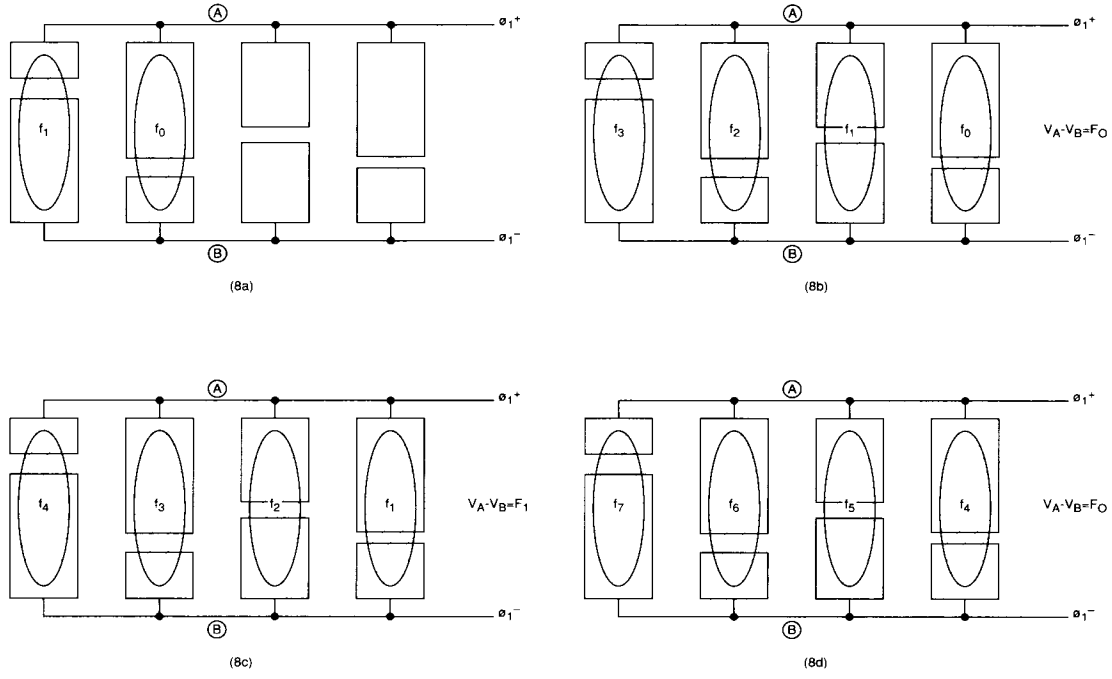


Figure 8. Sliding CZT for N=4

Lest the impression be left that this is all very complex, let us end this section with some block diagrams of the overall operation.

Figure 9 shows the SCZT at a glance. Since the operations are performed on complex numbers, any physical-world implementation will need to handle the real and imaginary parts separately. Figure 10 shows how this is done. It looks complicated, but it is simply a real-world version of Figure 9.

If the input signal is real-only, the preprocessing is simplified. If we only want a power spectrum, the postprocessing is simplified because phase is not part of a power measurement. With both of these assumptions, Figure 10 simplifies to Figure 11. The RC5601 Evaluation Module is based on this simplified application and is described later.

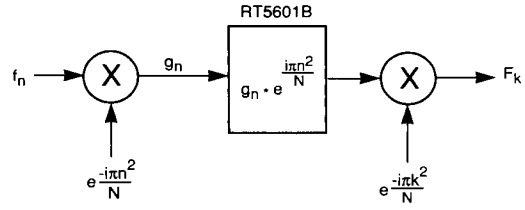


Figure 9. Complex Block Diagram of the CZT Algorithm

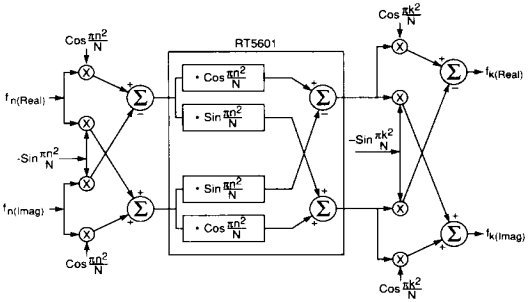


Figure 10. Real-world Diagram of the CZT Algorithm

How to use the RT5601B

The RT5601B requires support circuitry to perform the preprocessing and postprocessing steps of the CZT and to provide the proper inputs and biasing to the chip. These requirements are straightforward—if taken a little at a time! We will examine first the biasing and clocking requirements, then the required input format, then how the outputs are handled.

Biasing and Clocking

Pins 1, 3, 12, 20, and 22 are all bias or power supply pins. These need only an appropriate DC voltage and should be bypassed with capacitors. The voltages listed as typical in the specification tables are suggested, but are non-critical.

Pins 10 and 13 are auxiliary outputs which are used mostly during testing and initial adjustment. The input signals to the chip come out here in negative-going pulse form, delayed by approximately 512 clock periods. Each of these pins should have a pull-down resistor (approximately 10KΩ) to the substrate voltage.

Pins 2, 5, 7, 8, 11, 15, 16, 18, and 21 receive timing waveforms of varying duty cycle and phase (see Timing Diagrams, Figure 3 and 4).

Pins 4, 6, 17, and 19 serve as both input and output pins simultaneously. The ϕ_1 and ϕ_3 waveforms are applied through external capacitors to these major clock pins. The external capacitors interact with the internals of the RT5601B so that the differential output signals are superimposed on the common-mode input signal at the pins. This is explained more fully in the Output Handling section.

Input Requirements

There are two inputs: Real Input (pin 9) and Imaginary Input (pin 14). Each of these connects to its own 512-stage internal CCD "analog shift register" or "delay line"—thus, there are two such CCD "delay lines" (channels). When the ϕ_2 clock goes high, the input signals at these pins are sampled and shifted into the delay lines. Each delay line holds the latest 512 samples taken.

It should be noted here that since there are 2 inputs and 512 stages per input, there are really two (2) (512) = 1024 samples stored at any given time. But since one input is considered real and the other imaginary, we will usually consider the pair of

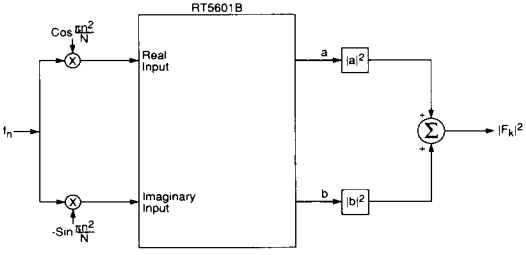


Figure 11. Use of the RT5601B in a Power Spectrum Measurement with Real-only Input

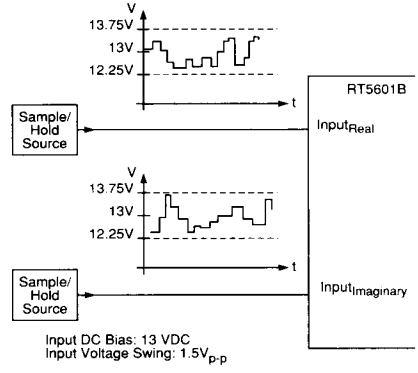


Figure 12. Input Biasing

samples taken when ø2 goes high to be one "complex" sample. Therefore, we say that the RT5601B holds 512 samples of a complex input waveform.

The input signals should be sampled-and-held to ensure that the input is stable and well-defined during the sampling time.

The inputs must be at the proper DC bias level and within the input voltage swing limits. Figure 12 diagrams appropriate DC bias and voltage swing for the RT5601B; see also Table 2.

Output Handling

Just as there are two main inputs, Real and Imaginary, there are two main outputs, Real and Imaginary. That is where the similarity ends. The following points must be understood for successful implementation of the RT5601B:

1. The outputs are differential (voltage). Each output signal is associated with 2 pins.

2. These output pins also serve as input pins for the ø1 and ø3 clock signals.

3. The output differential signal is superimposed onto the common-mode input signal (the ø1 and ø3 clock signal) at each of the 4 output pins.

4. The output signals are only valid when their respective clocks are high. For example, the ø1 (Real) output is valid when ø1 is high.

Figure 13 illustrates this set-up for the ø1 pins. The ø1 clock is of constant amplitude. It is applied to two external capacitors. The $ø1^+$ and $ø1^-$ pins are connected to internal "capacitances" that both drive the internals of the chip and sense the results. The external and internal capacitances interact (they form a capacitive voltage divider) to determine the ø1 clock amplitude at the ø1 pins. The CZT computation result affects this interaction so that the result appears differentially across these pins. This differential signal is small—on the order of tenths of volts—so the clock signal at each of these pins is still large enough to drive the internals of the chip.

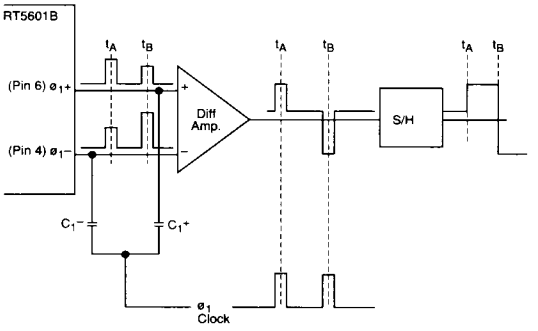


Figure 13. Output Format and Processing

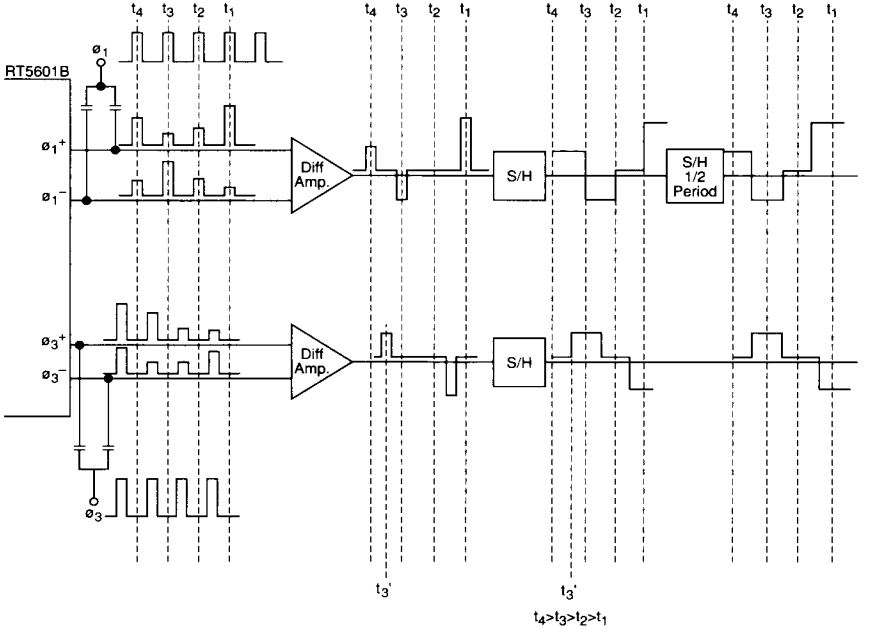


Figure 14. Handling and Synchronization of both Output Channels

The output differential voltage amp extracts the output. A S/H stage to "freeze" the output values after they have settled results in a more usable output signal. Notice that the S/H samples after the output changes in Figure 13.

The next consequence to notice is that the ø1 and ø3 outputs don't come out in phase with each other. Because their respective clocks are offset 1/2 sample period from each other, and each output is only valid when its clock is high, then their outputs are 1/2 sample period apart; the ø1 output component comes out 1/2 sample period before the corresponding ø3 output. To bring the two components together, a 1/2 sample period S/H delay can be applied to the ø1 output.

The entire situation is diagrammed in Figure 14.

RC5601 Evaluation Board

The RC5601 Evaluation Module is a 2-board assembly that gives the engineer a chance to work with the RT5601B without requiring a complete circuit design. It also serves as an example for designing the required external circuitry.

The module implements a 512-point power spectral density measurement and is diagrammed in Figure 15. Since the module is meant for demonstration purposes, real-only inputs are used.

The input is fed into a sample-hold circuit, which feeds into a pair of buffer/amplifiers. The outputs of these amplifiers are used as reference voltages to a pair of MDACs (Multiplying Digital-to-Analog Converters). Also feeding into the MDACs are a pair of ROMs which have the premultiply sine and cosine chirp values stored in digital form. The MDACs thus perform the premultiply needed for the CZT.

The MDAC output currents are converted into voltages. This current-to-voltage conversion also inserts the proper bias levels for the inputs of the RT5601B.

The now-preprocessed samples are clocked through the RT5601B which differentially outputs the CZT convolution values, a pair at a time (actually, the convolution values from the ø3 output pins come 1/2 sample period after their corresponding ø1 values). The differential voltage amplifiers extract the differential output signal and put the results into sample-hold stages to bring the two output channels into phase with each other.

The S/H outputs are fed into absolute-value circuits which combine into a stage that approximates the "hypotenuse function" (the square root of the sum of the squares of the two components).

The clock waveforms for the entire module are generated from a ROM that is driven by a single 1.6 MHz oscillator. The basic RC5601 Evaluation Module runs at a sample rate of 100 kHz, and can be adjusted up to 200 kHz by varying the board oscillator frequency or by using an external clock.

A detailed manual comes with the board.

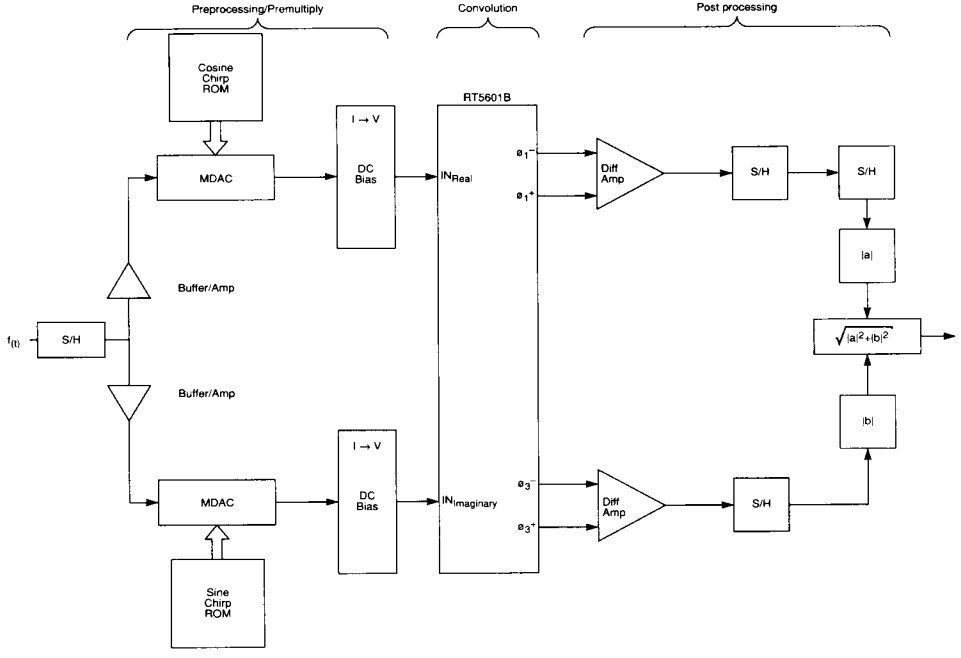


Figure 15. Block Diagram of the RC5601 Evaluation Module

Table 1. Pin Functions and Specifications

Pin	Sym	Function	Min	Typ	Max	Units
1	V_{SUB}	Substrate voltage [3,5]	0	-1.2	-7	V DC
2	ø4	Minor phase clock [1,4]	5	6	10	V_{p-p}
3	COM	Common (GND) connection [2]	-	-	-	-
4	$ø1^-$	Major phase clock and signal output line for minus side of real output [1,4]	10	12	14	V_{p-p}
5	$ø_{r1}$	Reset signal for real output [1,4]	5	15	22	V_{p-p}
6	$ø1^+$	Major phase clock and signal output line for plus side of real output [1,4]	10	12	14	V_{p-p}
7	I_{SGR}	Input sampling gate, real [1,4]	10	15	22	V_{p-p}
8	I_{RGR}	Input receiving gate, real [5]	1/2 I_{SGR}	3/5 I_{SGR}	I_{SGR}	V_{p-p}
9	In_{Real}	Signal input, real (DC bias voltage)	6	13	15	V DC
10	V_{OR}	Delay-line output, real	-	-	-	-
11	RESET	Delay-line output reset control [1]	10	15	22	V_{p-p}
12	V_{OG}	Delay-line output gate control [5]	2	3	5	V DC
13	V_{OI}	Delay-line output, imaginary	-	-	-	-
14	In_{Imag}	Signal input, imaginary (DC bias voltage)	6	13	15	V DC
15	I_{RGI}	Input receiving gate, imaginary [5]	1/2 I_{SGI}	3/5 I_{SGI}	I_{SGI}	V_{p-p}
16	I_{SGI}	Input sampling gate, imaginary [1]	10	15	22	V_{p-p}
17	$ø3^+$	Major phase clock and signal output line for plus side of imaginary output [1,4]	10	12	14	V_{p-p}
18	$ø_{r3}$	Reset signal for Imaginary output [1,4]	5	15	22	V_{p-p}
19	$ø3^-$	Major phase clock and signal output line for minus side of imaginary output [1,4]	10	12	14	V_{p-p}
20	V_{DD}	Positive voltage supply [1,5]	8	15	22	V DC
21	ø2	Minor phase clock [1]	5	6	10	V_{p-p}
22	V_{CB}	Corner bias voltage [1,5]	2	3	5	V DC

Notes:

1 All clocks swing from 0.4V low to as high as specified.

2 Common is reference level for all voltage measurements and is normally grounded.

3 The substrate must be at lowest potential, normally -1.2V.

4 See figure for clock waveform and timing; note that all waveforms must be free from over and under shoots with edges as clean as possible.

5 These are bias input nodes and must be well by-passed.

Table 2. Electrical Specifications (25°C)

Parameter	Sym	Conditions and Comments	Min	Typ	Max	Units
Input bias voltage		The input signals for both the real and imaginary channels are referenced to this level		13		V DC
Input signal swing		Applies to both real and imaginary input pins		1.5		V_{p-p}
Input capacitance	C_{in}	Refers to real and imaginary input pins		5		pF
Split electrode clock amplitude		Appled to external capacitors connected to $ø1^+$, $ø1^-$, $ø3^+$, and $ø3^-$		30		V_{p-p}
Minor clock line capacitance		Refers to $ø2$, $ø4$ pins		200		pF
Split electrode line capacitance		Refers to $ø1^+$, $ø1^-$, $ø3^+$, and $ø3^-$ pins		400		pF
Clock frequency	f_C	Clock frequency = sample frequency, f_S	.004		10	MHz
Power dissipation	P_D			500		mW
Output signal level		Difference voltage between $ø3^+$ and $ø3^-$ pins or between $ø1^+$ and $ø1^-$ pins		.2		V_{p-p}
Dynamic range	DR	Peak signal to RMS noise		60		dB
Total harmonic distortion (Linearity)	THD			1		%
Internal weighting accuracy		Accuracy is 8 bits plus a sign bit. Refers to internal mask-programmed constants.		8		bits

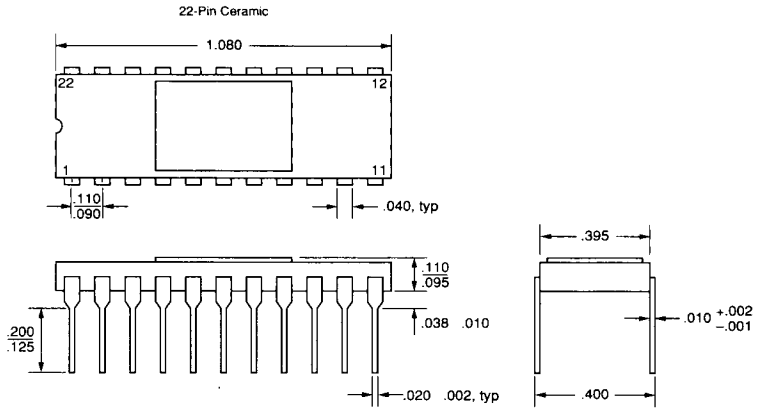


Figure 16. Package Dimensions

Ordering Information

Part Number	Description
RT5601BBB-011	512-point, buried channel CCD DFT processor with Hanning-windowed taps, 22-pin ceramic side brazed package