ADVANCED ANALOG

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Preliminary

DAS862/863

16 Single Ended
8 Differential Input
12-Bit Data Acquisition System

DESCRIPTION

The DAS862/863 is a complete data acquisition subsystem packaged in a hermetically sealed 1" square leadless chip carrier or a 1.1" square pin grid array. The small size and low power consumption provide an ideal data acquisition solution when space is at a premium.

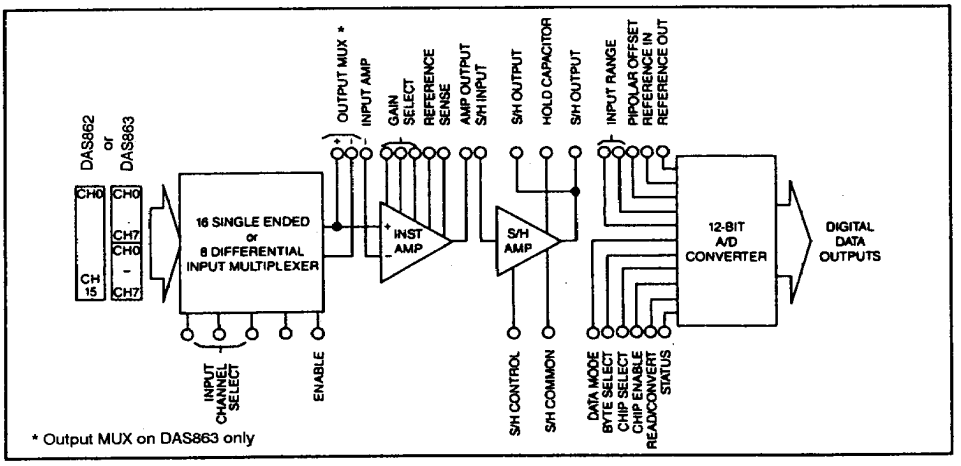
The device consists of an input multiplexer (DAS862 16 single ended inputs, DAS863 8 differential inputs), instrumentation amplifier with selectable gains, sample/hold amplifier and A/D converter with microprocessor interface and tri-state buffers.

The DAS862/863 will accept unipolar or bipolar voltage inputs in the range of 0 to +10V, ±5V and ±10V. For low level signals, jumper selectable gains of 10 or 100 can be applied. The number of input channels can be expanded by the addition of multiplexers. The microprocessor interface and the facility of the sample/hold amplifier being controlled directly by the A/D converter simplifies system integration.

FEATURES

- **Complete 12-bit data acquisition subsystem**
- **Input ranges selectable for unipolar or bipolar operation**
- **Throughput rates**
  - **8-bit accuracy - 45kHz**
  - **12-bit accuracy - 33kHz**
- **Selectable gains of 1, 10 and 100**
- **Full microprocessor compatible interface**
- **Guaranteed no missing codes over temperature**
- **Surface mount or pin grid array package options**
- **Full specification over three temperature ranges**

BLOCK DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

+Vcc to ACOM	-0.5V	Analog input signal range	+Vcc +20V to -VCC -20V
-Vcc to ACOM	+0.5V to -16V	Digital input signal	-0.5V to +VDD
+VDD to DCOM	-0.5V to +5.5V	ACOM to DCOM	±1V

@ 25°C, Vcc = +15V, VDD = +5V external sample/hold capacitor of 4700pF.

Model	DAS862/DAS863 J, A, R			DAS862/DAS863 K, B, S			
	min	typ	max	min	typ	max	units
Resolution			12			*	Bits
INPUT - ANALOG							
Voltage Range - Bipolar			±5, ±10				V
- Unipolar			0 - 10				V
Input impedance - on channel		10^{10}			*		Ω
- off channel		10^{10}			*		Ω
Input capacitance - on channel		20			*		pF
- off channel		20			*		pF
CMRR (20V, DC to 1kHz)		60	85	*	*		dB
Crosstalk (20Vp-p, 1kHz)[1]		-85	-80		*	*	dB
Feedthrough (at 1kHz)[1]		-85	-80		*	*	dB
Offset (channel to channel) G = 1[2]		30	10		*	*	µV
Input bias current/channel		1	5		*	*	nA
Input voltage range[3]	+10	+11		*	*		V
	-10	-15					
DIGITAL							
Multiplexer channel select - Logic "1" (2V)		5	30		*	*	µA
- Logic "0" (0.8V)		5	30		*	*	µA
S/H Command - Logic "1" (2V)		0.2			*		nA
- Logic "0" (0.8V)		5	30		*	*	µA
ADC section - Logic "1" (2.4V)			10			*	µA
- Logic "0" (0.8V)			10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Integral linearity[4]			±0.024			±0.012	% of FSR
Differential linearity[4]			±0.024			±0.012	% of FSR
Gain error[5] - G = 1		0.7			*		%
- G = 100		0.9			*		%
Unipolar offset error[5]		16			*		mV
Bipolar offset error[5]		50			*		mV
Noise error (measured at S/H output) G = 1		0.5	1		*	*	mV p-p
Droop rate		50	500		*	*	µV/mS
Temperature coefficients - Unipolar offset			20			15	ppm FSR/°C
- Bipolar offset			30			25	ppm FSR/°C
- Full scale calibration			60			35	ppm FSR/°C
SYSTEM TIMINGS							
ADC conversion time		20	25		*	*	µs
S/H aperture delay		50			*		ns
S/H aperture uncertainty		2				*	ns
TIMING							
Acquisition time (to 0.01% of final value for full scale step		5			*		µs
Throughput - serial mode			45			*	µs
- overlap mode			30			*	µs
OUTPUT - DIGITAL DATA							
Output codes - Unipolar			Straight binary				
- Bipolar			Offset binary				
Logic levels - Logic "0" (sink = 1.6mA)			+0.4			*	V
- Logic "1" (source = 500µA)	2.4			*			V
Leakage (data bits only) high-Z state	-5	0.1	+5	*	*	*	µA
POWER SUPPLY REQUIREMENTS							
Rated voltage - Analog (±Vcc)	14.25	15	15.75	*	*	*	VDC
- Digital (VDD)	4.75	5	5.25	*	*	*	VDC
Supply drain, +15V		18	25		*	*	mA
-15V		11	18		*	*	mA
+5V		1	2		*	*	mA
Power dissipation		.44	.66		*	*	W
TEMPERATURE RANGE							
Operating temperature range - JH, KH/JL, KL	0		70	*		*	°C
- AH, BH,AL, BL	-25		+85	*		*	°C
- RH, SH/RL, BL	-55		+125	*		*	°C
Storage temperature range	-65		+150	*		*	°C

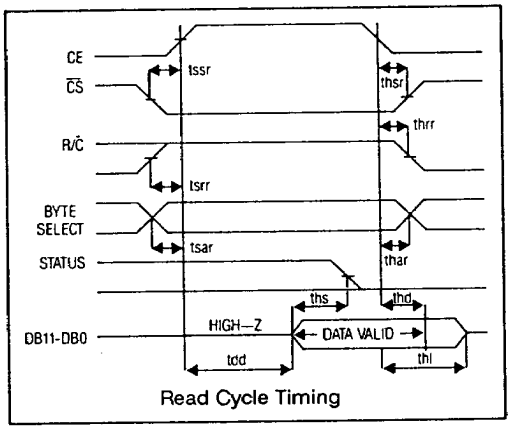
Notes:
1. Measured at the sample and hold output.
2. Measured with all input channels grounded.
3. The range of voltage on any input with respect to common over which accuracy and leakage current is guaranteed.
4. Applicable over full operating temperature range.
5. Adjustable to zero using external potentiometer or select on test resistor.

* Specification same as DAS862/863 J/A/R. No missing codes guaranteed over temperature.

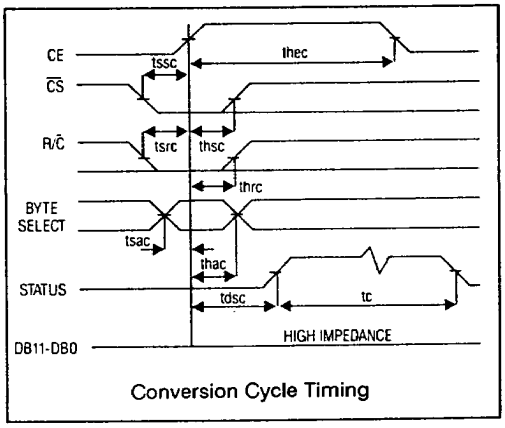
ANALOG TIMING SPECIFICATIONS

Parameter	Min	Typ	Max	Units
MULTIPLEXER				
Switching Time				
(between channels)		+15		µs
Settling time				
(10V step to 0.02%)		2.5		µs
Enable time ON		1	2	µs
OFF		0.25	0.5	µs
INSTRUMENTATION AMPLIFIER				
Settling time to 0.01%				
G = 1		5	12.5	µs
G = 10		3	7.5	µs
G = 100		4	7.5	µs
Slew rate	12	17		V/µs
S/H AMPLIFIER				
Acquisition time				
(10V step to 0.01%		5		µs
Aperture delay		50		ns
Hold mode settling time		1.5		µs
Slew rate		10		V/µs

Note: Specifications are at +25°C and measured at 50% level of transition.



Read Cycle Timing



Conversion Cycle Timing

DIGITAL TIMING SPECIFICATIONS

Symbol	Parameter	Min	Typ	Max	Units
CONVERT MODE					
tdsc	Status delay from CE		100	200	ns
thec	CE pulse width	50	30		ns
tssc	CS to CE setup	50	20		ns
thsc	CS low during CE high	50	20		ns
tsrc	R/C to CE setup	50	0		ns
thrc	R/C low during CE high	50	20		ns
tsac	Byte select to CE setup	0	0		ns
thac	Byte selected valid during CE high		50	20	ns
tc	Conversion time				
	12 bit cycle	15	20	25	µs
	8 bit cycle	10	13	17	µs
READ MODE					
tdd	Access time from CE		75	150	ns
thd	Data valid after CE low	25	35		ns
thi	Output float delay		100	150	ns
tssr	CS to CE setup		50	0	ns
tsrr	R/C to CE setup	0	0		ns
tsar	Byte select to CE setup	50	25		ns
thsr	CS valid after CE low	0	0		ns
thrr	R/C high after CE low	0	0		ns
thar	Byte select valid after CE low	50	25		ns
ths	Status delay after data valid	300	500	1000	ns

CE	CS	R/C	Data Mode	Byte Select	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

Figure 1 *Control Input Truth Table*

DAS862						DAS863				
MUX ADD3	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Selected	MUX ADD2	MUX ADD1	MUX ADD0	MUX Enable	Channel Pair Selected
X	X	X	X	L	none	X	X	X	L	none
L	L	L	L	H	0	L	L	L	H	0
L	L	L	H	H	1	L	L	H	H	1
L	L	H	L	H	2	L	H	L	H	2
L	L	H	H	H	3	L	H	H	H	3
L	H	L	L	H	4	H	L	L	H	4
L	H	L	H	H	5	H	L	H	H	5
L	H	H	L	H	6	H	H	L	H	6
L	H	H	H	H	7	H	H	H	H	7
H	L	L	L	H	8		-			
H	L	L	H	H	9		-			
H	L	H	L	H	10		-			
H	L	H	H	H	11		-			
H	H	L	L	H	12		-			
H	H	L	H	H	13		-			
H	H	H	L	H	14		-			
H	H	H	H	H	15		-			

Figure 2 *Channel Select Truth Table*

RANGE	-FS +1/2 LSB 000 TO 001 TRANSITION	+FS -1/2 LSB FFE TO FFF TRANSITION	1 LSB =
0 - 10V	+0.0012V	+9.9963V	2.44mV
±5V	-4.9988V	+4.9963V	2.44mV
±10V	-9.9976V	+9.9927V	4.88mV

Figure 3 *Code Transition Ranges*

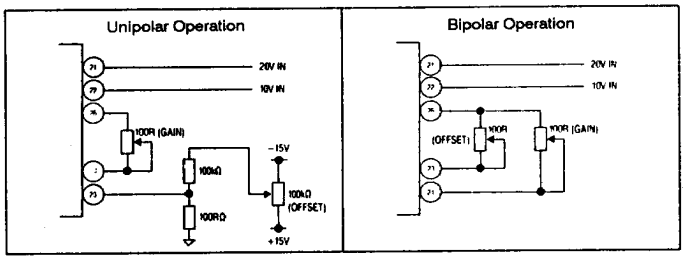


Figure 4 *Calibration*

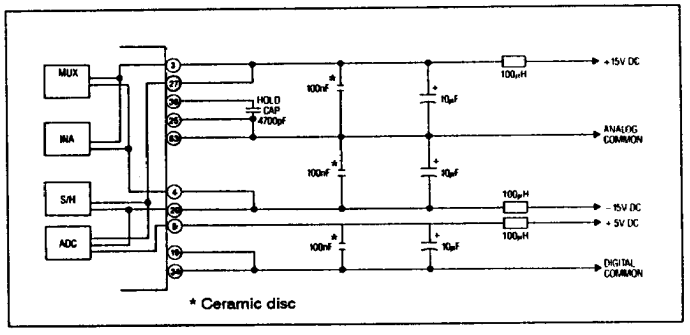
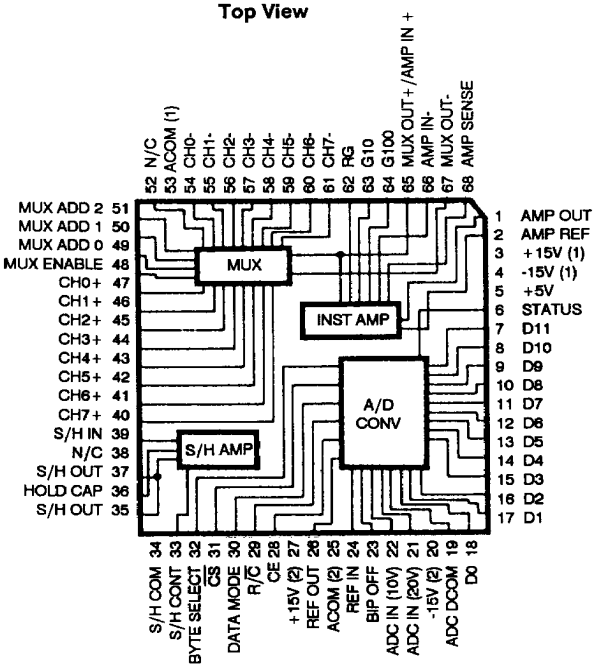


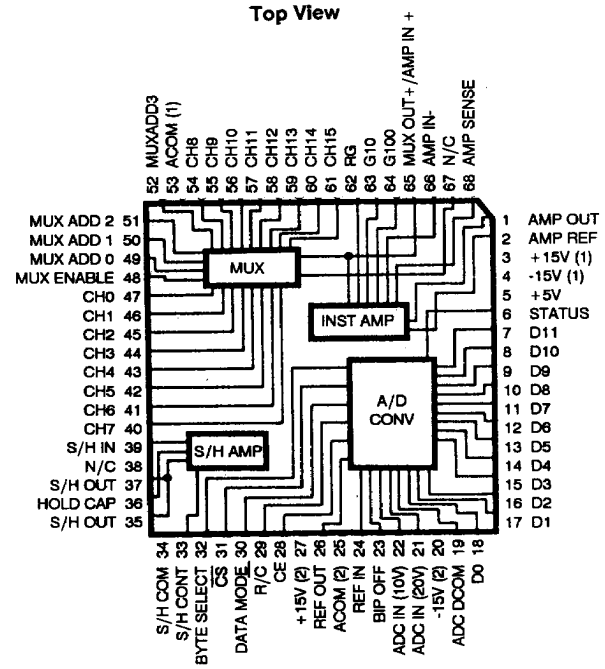
Figure 5 *Power Supply Connections and Recommended Decoupling*

PIN DESIGNATIONS

DAS863
Top View



DAS862
Top View



ORDERING INFORMATION

DAS862 16 Single Ended Inputs				DAS863 8 Differential Inputs			
Grade	68-pin Package LCC	68-pin Package PGA	Accuracy %FSR	Temp Range °C	Grade	68-pin Package LCC	68-pin Package PGA	Accuracy %FSR	Temp Range °C
J	L	H	±0.024	0 - 70	J	L	H	±0.024	0 - 70
K	L	H	±0.012	0 - 70	K	L	H	±0.012	0 - 70
A	L	H	±0.024	-25 +85	A	L	H	±0.024	-25 - +85
B	L	H	±0.012	-25 +85	A	L	H	±0.024	-25 - +85
R	L	H	±0.024	-55 +125	R	L	H	±0.024	-55 - +125
S	L	H	±0.012	-55 - +125	R	L	H	±0.024	-55 - +125

PIN FUNCTIONS

CH0 to CH15 - Pins 40 to 47
CH0 to CH7 (+, -) - Pins 54 to 61
Channel inputs
Analog inputs, 16 total, for single ended and differential operation. Inputs that are not used must be connected to analog common.

MUX out+/AMP in+ - Pin 65
Multiplexer high output
This is the multiplexer output on the DAS862. On the DAS863, it is the output of the positive selected inputs. It is connected internally to the positive input of the instrumentation amplifier.

MUX out - Pin 67
Multiplexer low output
This pin is used on the DAS863 only. It should be connected to the negative input of the instrumentation amplifier.

AMP in - Pin 66
Negative input of instrumentation amplifier
This should be connected to the analog common on the DAS862 and to the MUX OUT (Pin 67) on the DAS863.

AMP out - Pin 1
Output of instrumentation amplifier
This should be connected to the input of the sample/hold amplifier (Pin 39).

Amp Sense - Pin 68
Output sense line of instrumentation amplifier
Normally connected directly to A input (Pin 1).

AMP Ref - Pin 2
Reference for amplifier output
This pin will normally be connected to analog common. Care should be taken to minimize tracking and contact resistance to analog common to augment system accuracy.

S/H Out - Pin 35/37
Output of sample/hold amplifier
Two pins are provided to supply a guard ring around the hold capacitor pin. These pins should be connected to either ADC in (20V) or ADC in (10V) depending on the desired range.

Hold Cap - Pin 36
Connection for hold capacitor on sample/hold amplifier
The tracking to the hold capacitor should be as short as possible and have a guard ring set up using Pins 35 and 37.

ADC in (20V) - Pin 21
ADC in (10V) - Pin 22
Inputs to A/D converter
Should be connected to S/H amplifier. Use applicable pin for desired range.

RG, G10, G100 - Pins 62 - 64
Gain setting pins on instrumentation amplifier
Gain 1 - No connection.
Gain 10 - Connect G10 to RG.
Gain 100 - Connect G100 to RG.

Ref Out - Pin 26
10V reference voltage
Reference voltage for the A/D converter.

Ref In, BIP off - Pins 23, 24
Reference input and offset input to A/D converter
Connect trimming potentiometers (or select on test resistors) for unipolar or bipolar operation. Refer to Figure 4.

S/H in - Pin 39
Input to sample/hold amplifier
Connect to pin 1, amp out.

MUX Enable - Pin 48
Multiple enable/disable
Logic "1" on this pin will enable a selected channel on the internal multiplexer. Logic "0" deselects all channels.

MUX ADD 0 to MUX ADD 3 - Pins 49 to 52
Address inputs for channel selection
These address lines select a specific channel as shown in Figure 2.

S/H Control - Pin 33
Track/hold control on S/H amplifier
Logic "1" holds an analog value for conversion by the A/D converter. This line may be controlled by the status (Pin 6) of the converter to simplify external timing control.

S/H Common - Pin 34
Reference for S/H logic control
Connect to digital common.

D0 to D11 - Pins 7 - 18
Tri-state digital outputs
The 12 or 8 bit result of a conversion that is available as output on these pins. D0 is LSB and D11 is MSB.

Status - Pin 6
Status of A/D converter
During a conversion cycle, this output is at logic "1". It may be used to directly control the sample/hold amplifier.

CE - Pin 28
Chip enable
The input must be at Logic "1" to initiate a conversion or read output data. Refer Figure 1.

CS - Pin 31
Chip select
Input must be at Logic "0" to initiate a conversion or read output data. Refer Figure 1.

R/C - Pin 29
Read/convert
Data can be read when this pin is at logic "1" or a conversion can be initiated when this pin is at logic "0". This pin is usually connected to the R/W control line of a microprocessor based system. Refer Figure 1.

Data Mode - Pin 30
Select 12 or 8 bit data
Logic "1" - All 12 output data bits are enabled simultaneously.
Logic "0" - MSBs and LSBs are controlled by byte select, Pin 32.

Byte Select - Pin 32
Byte address, short cycle
Byte select at logic "0" enables the 8 MSBs when reading output data. Byte select at logic "1" enables the 4 LSBs. 4 LSBs can be connected to four of the MSB lines for interconnection to an 8-bit bus. In start convert mode, logic "0" enables a 12-bit conversion, while logic "1" will short cycle the conversion to 8 bits. Refer Figure 1.

+15V (1) +15V (2) - Pins 3, 27
Power supply
Connect to +15V supply using decoupling techniques as shown in Figure 5.

-15V (1) -15V (2) - Pins 4, 20
Power Supply
Connect to -15V supply using decoupling techniques as shown in Figure 5.

A COM (1), A COM (2) - Pins 53, 25
Analog common
A common (including a digital common) should be connected together at one point close to the device.

+5V - Pin 5
Logic power supply
Connect to +5V digital supply line using decoupling technique shown in Figure 5.

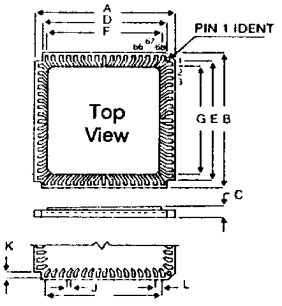
ADC DCOM - Pin 19
Reference for A/D converter control lines
Should be connected to S/H common at one point close to device.

N/C - Pin 38
No internal connection

MECHANICAL OUTLINE

Leadless Chip Carrier

L Package

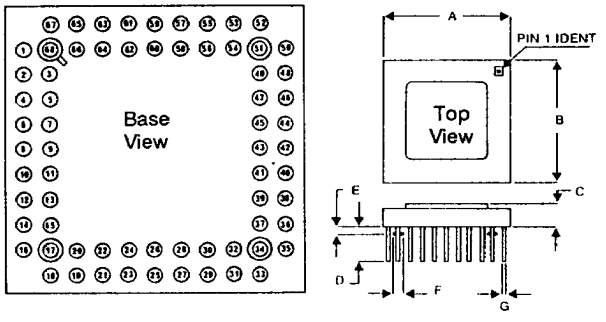


	Inches		Millimeters	
Dim	Min	Max	Min	Max
A	.945	.965	24.003	24.511
B	.945	.965	24.003	24.511
C	.076	.094	1.934	2.388
D	.841	.859	21.361	21.819
E	.841	.859	21.361	21.819
F	.755	.785	19.177	19.939
G	.755	.785	19.177	19.939
H	.800	Basic	20.320	Basic
J	.027	.033	.686	.838
K	.045	Basic	1.143	Basic
L	.050	Basic	1.270	Basic

Terminations: Gold plated nickel on refractory metallization.
Case: White ceramic with gold plated nickel lid.
Hermeticity: Gross leak test.
Weight: 4.2. grams (0.15 oz.)

Pin Grid Array

H Package



Terminations: Gold plated KOVAR.
Case: Black ceramic with gold plated nickel lid.
Hermeticity: Gross leak test.
Weight: 9 gms (0.32 oz.)

	Inches		Millimeters	
Dim	Min	Max	Min	Max
A	1.087	1.109	27.610	28.169
B	1.087	1.109	27.610	28.169
C	.095	.120	2.413	3.048
D	.162	.198	4.115	5.029
E	.045	.055	1.143	1.397
F	.045	.055	1.143	1.397
G	.016	.020	.406	.508
H	.100	Basic	2.540	Basic
J	.100	Basic	2.540	Basic

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