

PowerMOS transistor

Logic level FET

BUK581-100A**GENERAL DESCRIPTION**

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mount applications.

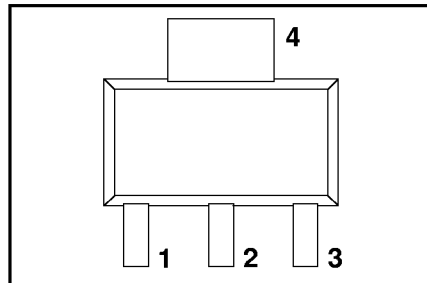
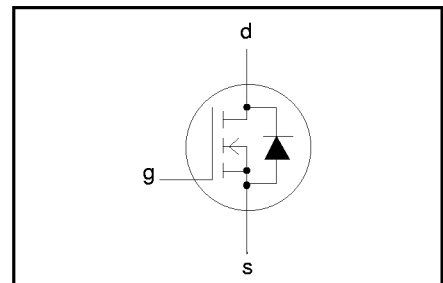
The device is intended for use in automotive and general purpose switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	0.9	A
P_{tot}	Total power dissipation	1.5	W
T_j	Junction temperature	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5\text{ V}$	0.90	Ω

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION**SYMBOL****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	$T_{amb} = 25\text{ °C}$	-	0.9	A
I_D	Drain current (DC)	$T_{amb} = 100\text{ °C}$	-	0.6	A
I_{DM}	Drain current (pulse peak value)	$T_{amb} = 25\text{ °C}$	-	3.6	A
P_{tot}	Total power dissipation	$T_{amb} = 25\text{ °C}$	-	1.5	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\text{ j-b}}$	From junction to board ¹	Mounted on any PCB	-	50	-	K/W
$R_{th\text{ j-amb}}$	From junction to ambient	Mounted on PCB of Fig.17	-	-	85	K/W

¹ Temperature measured 1-3 mm from tab.

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STATIC CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 0.1\text{ mA}$	1.0	1.5	2.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V};$ $V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	1	10	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 15\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 0.9\text{ A}$	-	0.51	0.90	Ω

DYNAMIC CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 0.9\text{ A}$	1	1.8	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	180	300	pF
C_{oss}	Output capacitance		-	45	60	pF
C_{rss}	Feedback capacitance		-	16	25	pF
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 3\text{ A};$ $V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ $R_{gen} = 50\text{ }\Omega$	-	6	10	ns
t_r	Turn-on rise time		-	45	55	ns
t_{doff}	Turn-off delay time		-	15	25	ns
t_f	Turn-off fall time		-	20	30	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	0.9	A
I_{DRM}	Pulsed reverse drain current	-	-	-	3.6	A
V_{SD}	Diode forward voltage	$I_F = 0.9\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.1	V
t_{rr}	Reverse recovery time	$I_F = 0.9\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	40	-	ns
Q_{rr}	Reverse recovery charge		-	100	-	nC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 0.9\text{ A}; V_{DD} \leq 25\text{ V};$ $V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega; T_{amb} = 25\text{ }^{\circ}\text{C}$	-	-	10	mJ

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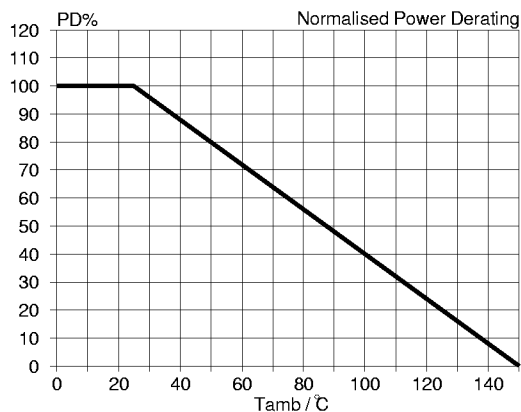


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ C} = f(T_{amb})$

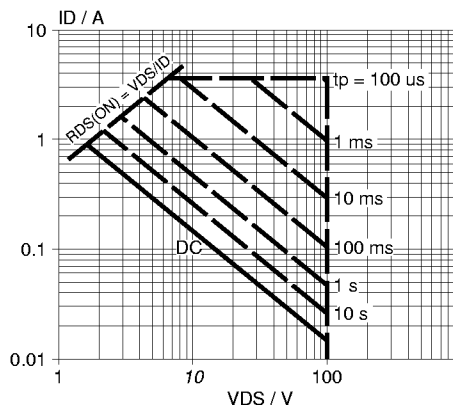


Fig.4. Safe operating area $T_{amb} = 25\ ^\circ C$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

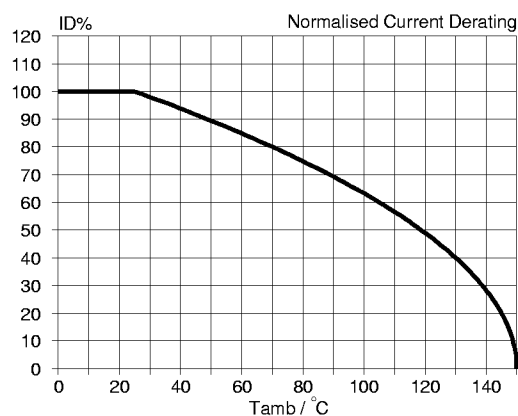


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ C} = f(T_{amb})$; conditions: $V_{GS} \geq 5\ V$

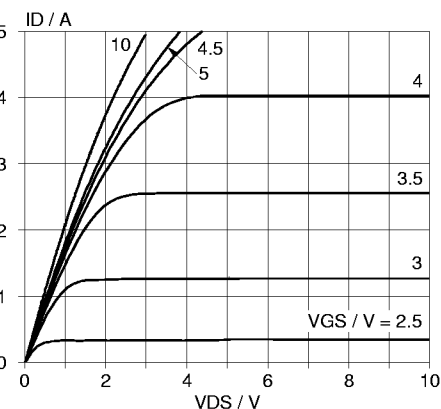


Fig.5. Typical output characteristics, $T_J = 25\ ^\circ C$.
 $I_D = f(V_{DS})$; parameter V_{GS}

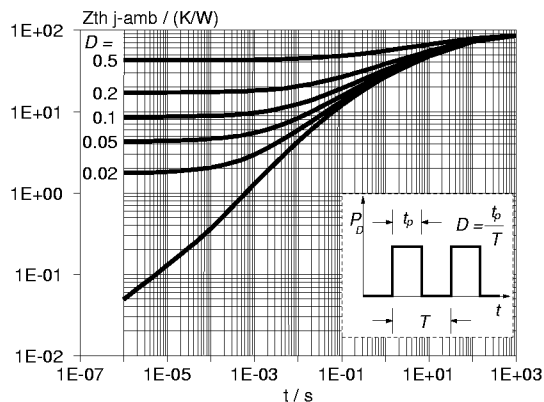


Fig.3. Transient thermal impedance.
 $Z_{th\ j-amb} = f(t)$; parameter $D = t_p / T$

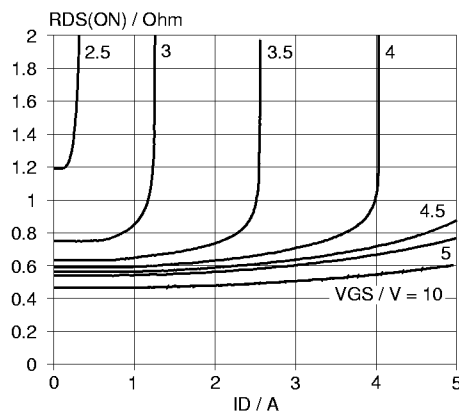


Fig.6. Typical on-state resistance, $T_J = 25\ ^\circ C$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

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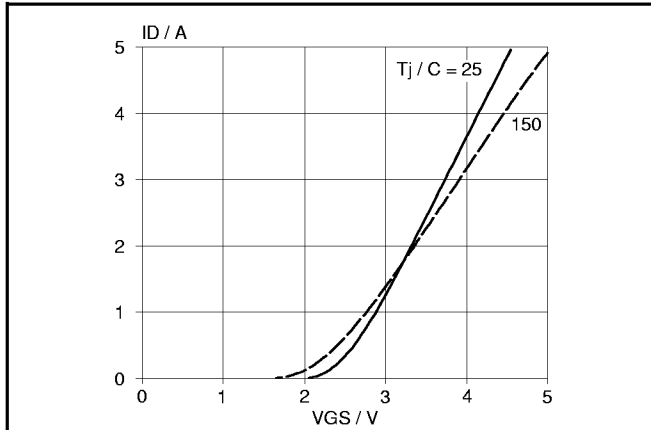


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

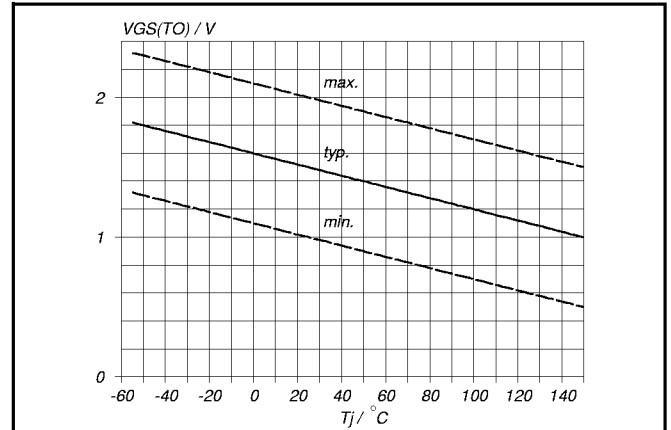


Fig.10. Gate threshold voltage.
 $V_{GS(TH)} = f(T_j)$; conditions: $I_D = 0.1\text{ mA}$; $V_{DS} = V_{GS}$

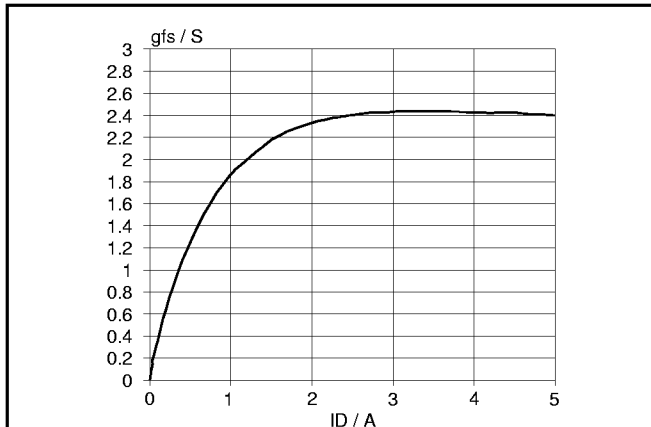


Fig.8. Typical transconductance, $T_j = 25\text{ °C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

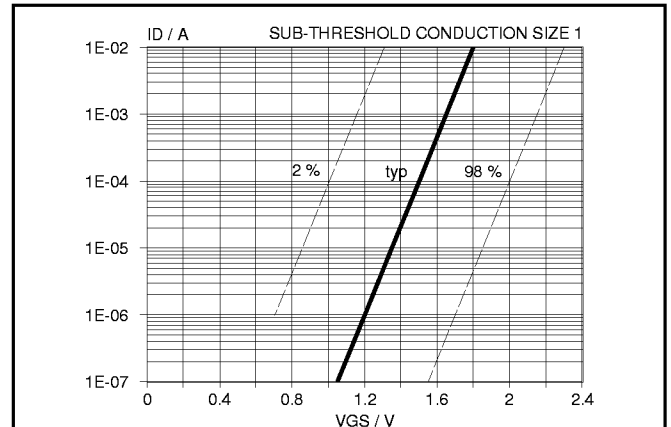


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25\text{ °C}$; $V_{DS} = V_{GS}$

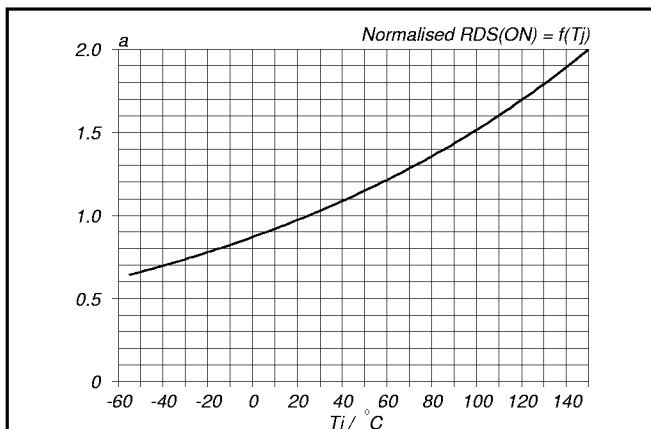


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ °C}} = f(T_j)$; $I_D = 0.9\text{ A}$; $V_{GS} = 5\text{ V}$

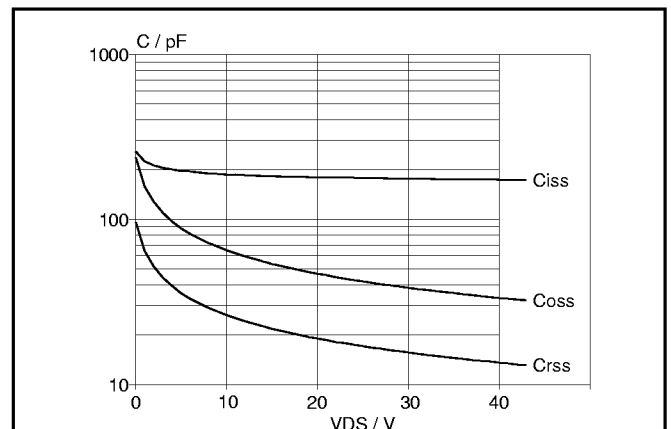


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

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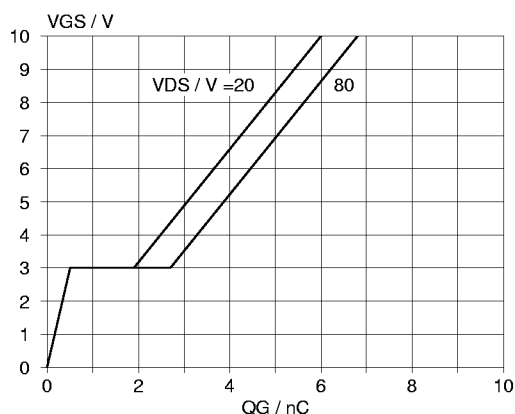


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 0.9 \text{ A}$; parameter V_{DS}

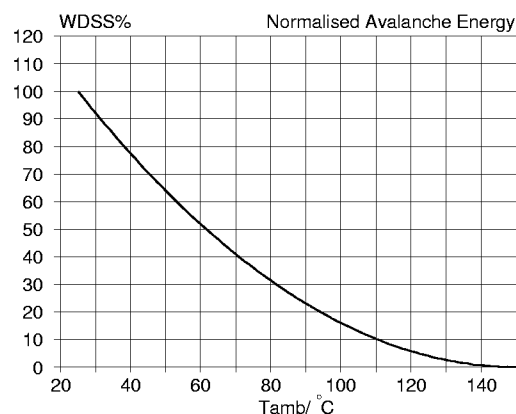


Fig. 15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{amb})$; conditions: $I_D = 0.9 \text{ A}$

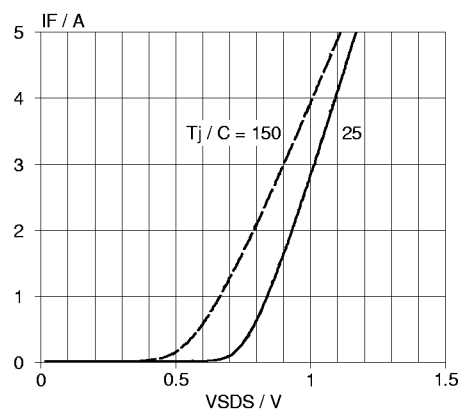


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0 \text{ V}$; parameter T_j

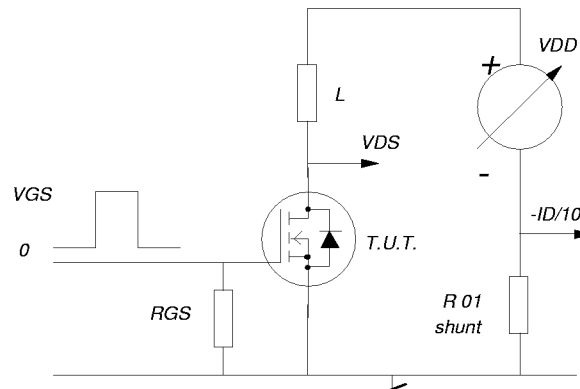
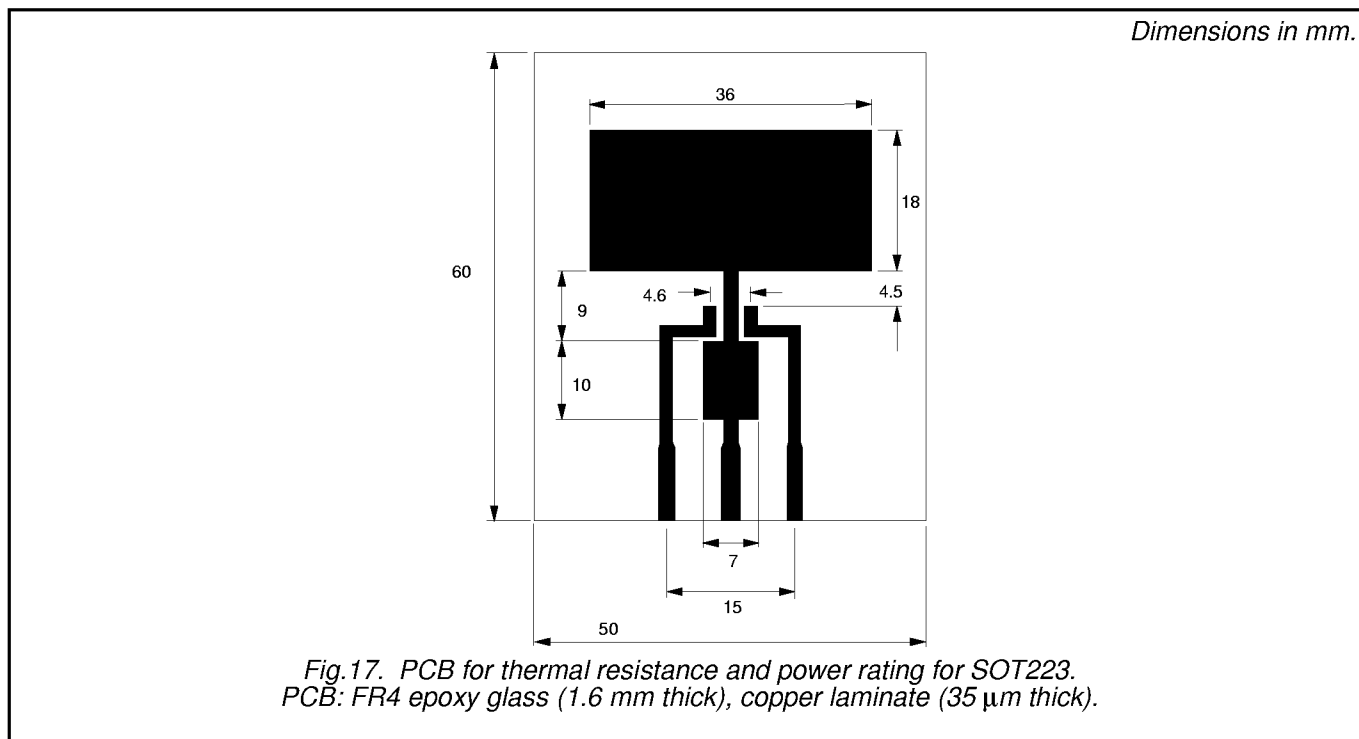


Fig. 16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

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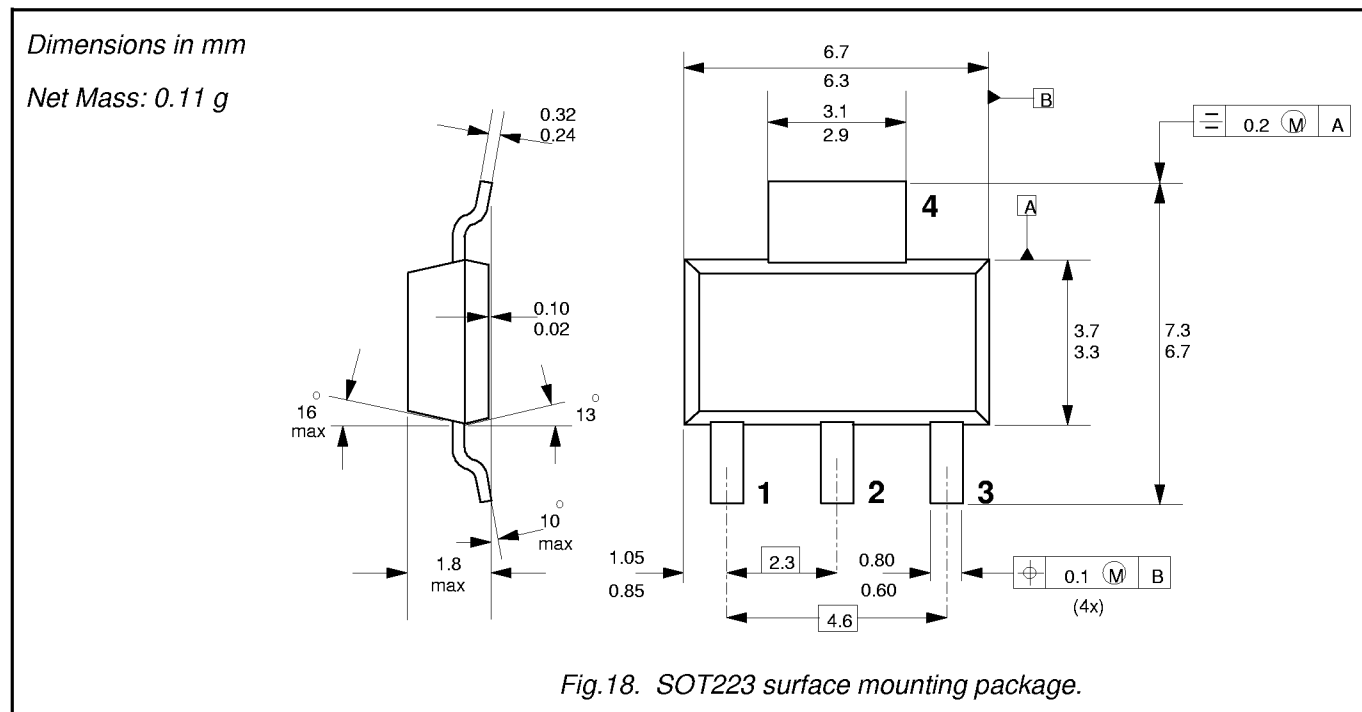
BUK581-100A

PRINTED CIRCUIT BOARD

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MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".