Silicon n-channel dual gate MOS-FETs

BF901; BF901R

FEATURES

- Intended for low voltage operation
- Short channel transistor with high ratio $|Y_{fs}|:C_{is}$
- Low noise gain-controlled amplifier to 1 GHz
- BF901R has reverse pinning.

DESCRIPTION

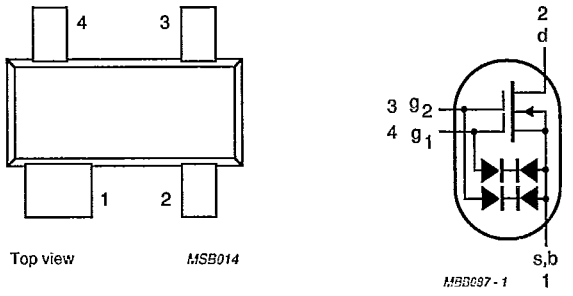
Enhancement type field-effect transistors in plastic microminiature SOT143 and SOT143R envelopes, with source and substrate interconnected. They are intended for UHF and VHF applications, such as television tuners and professional communications equipment especially suited for low voltage operation. These MOS-FET tetrodes are protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

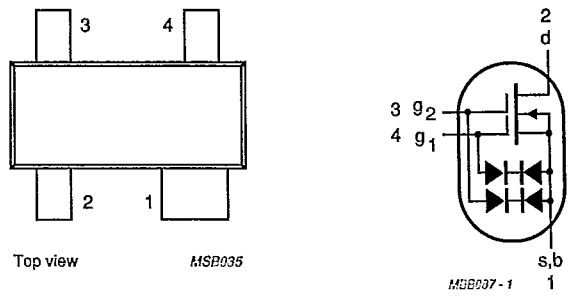
QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage	–	12	V
I_D	drain current	–	30	mA
P_{tot}	total power dissipation	–	200	mW
T_j	junction temperature	–	150	°C
$\|Y_{fs}\|$	transfer admittance	28	35	mS
C_{ig1-s}	input capacitance at gate 1	2.35	2.75	pF
C_{rs}	feedback capacitance	25	–	fF
F	noise figure at 800 MHz	1.7	–	dB



Marking code: MO1.

Fig.1 Simplified outline (SOT143) and symbol.



Marking code: MO2.

Fig.2 Simplified outline (SOT143R) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	12	V
V_{D-G2}	drain-gate 2 voltage		–	6	V
I_D	DC drain current		–	30	mA
$\pm I_{G1-S}$	gate 1-source current		–	10	mA
$\pm I_{G2-S}$	gate 2-source current		–	10	mA
P_{tot}	total power dissipation				
	BF901	up to T_{amb} = 50 °C (note 1)	–	200	mW
	BF901R	up to T_{amb} = 40 °C (note 1)	–	200	mW
T_{stg}	storage temperature		–65	150	°C
T_j	junction temperature		–	150	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	thermal resistance from junction to ambient (note 1)	
	BF901	500 K/W
	BF901R	550 K/W

Note

1. Device mounted on an FR4 printboard.

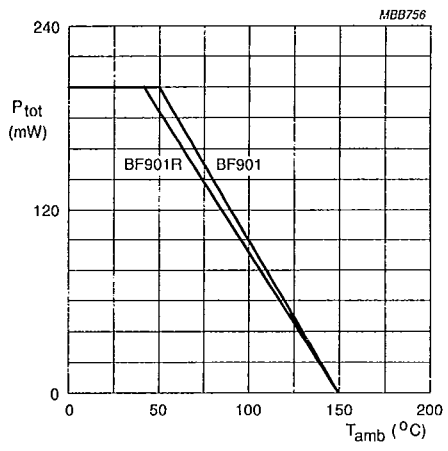


Fig.3 Power derating curve.

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STATIC CHARACTERISTICS

T_j = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$\pm I_{G1\text{-}SS}$	gate 1 cut-off current	$\pm V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S} = V_{DS} = 0$	–	50	nA
$\pm I_{G2\text{-}SS}$	gate 2 cut-off current	$\pm V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S} = V_{DS} = 0$	–	50	nA
$\pm V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$\pm I_{G1\text{-}SS}$ = 10 mA; $V_{G2\text{-}S} = V_{DS} = 0$	6	20	V
$\pm V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$\pm I_{G2\text{-}SS}$ = 10 mA; $V_{G1\text{-}S} = V_{DS} = 0$	6	20	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	I_D = 20 µA; V_{DS} = 8 V; $V_{G2\text{-}S}$ = 4 V	0	0.7	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	I_D = 20 µA; V_{DS} = 8 V; $V_{G1\text{-}S} = 0$	0.3	1	V
I_{DSX}	drain-source current	V_{DS} = 4 V; $V_{G1\text{-}S}$ = 1.1 V; $V_{G2\text{-}S}$ = 3.4 V	2	18	mA

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): I_D = 14 mA; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert Y_{fs}\rvert$	transfer admittance	pulsed; T_j = 25 °C	25	28	35	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	2.35	2.75	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	1.2	–	pF
C_{os}	output capacitance	f = 1 MHz	–	1.4	–	pF
C_{rs}	feedback capacitance	f = 1 MHz	–	25	–	fF
F	noise figure	f = 200 MHz; G_s = 2 mS; $B_s = B_{sopt.}$	–	0.7	–	dB
		f = 800 MHz; G_s = 3.3 mS; $B_s = B_{sopt.}$	–	1.7	–	dB