T-46-07-11

June 1992

74BCT374
Octal D Flip-Flop with TRI-STATE® Outputs

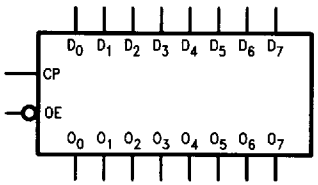
General Description

The 'BCT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed 4000V minimum ESD protection
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

Logic Symbols



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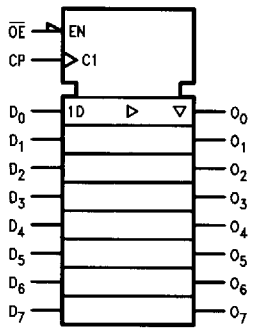
IEEE/IEC



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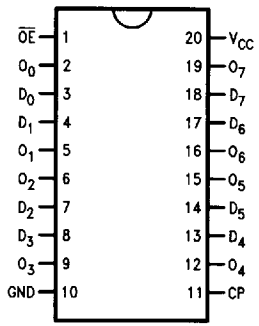
Connection Diagram

Pin Assignment for DIP and SOIC



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Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

9000-3486

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

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Functional Description

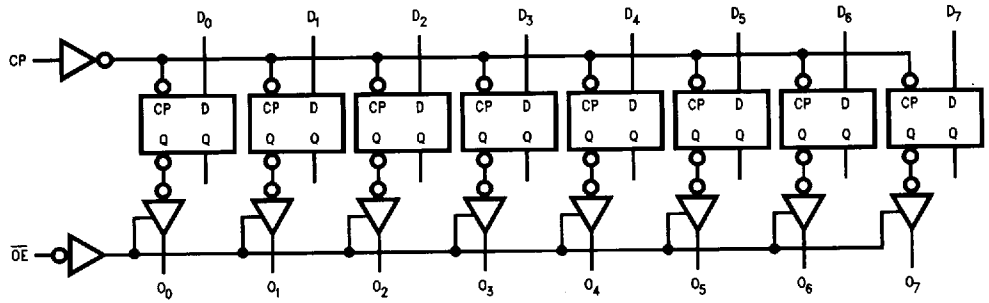
The 'BCT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Internal Register	Output
D_n	CP	$\overline{OE}$		O_n
H	⌐	L	H	H
L	⌐	L	L	L
X	X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in the Disable or Power-Off State	−0.5V to +5.5V
in the High State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−250	μA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		6	9	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		40	50	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		6	9	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74BCT $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	70	130		70		MHz
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0 2.0	5.4 4.3	9.1 8.8	2.0 2.0	10.6 10.0	ns
t_{PZH} t_{PZL}	Output Enable Time	1.0 1.0	8.0 9.0	13.0 13.0	1.0 1.0	13.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time	1.0 1.0	4.2 4.2	6.8 6.8	1.0 1.0	6.8 6.8	ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.75		0.75	ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.60		0.60	ns
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			2.5		2.5	ns
t_{PV} (Note 2)	Device to Device Skew			4.0		4.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

AC Operating Requirements

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Symbol	Parameter	74BCT $T_A = +25°C$, $V_{CC} = +5.0V$		74BCT $T_A, V_{CC} = Com$		Units
		Min	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	8.5 8.5		8.5 8.5		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0 0		0 0		
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	4.0 11.5		4.0 11.5		ns

Extended AC Electrical Characteristics

Symbol	Parameter	74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 50$ pF, 8 Outputs Switching (Note 3)		74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 250$ pF, 1 Output Switching (Note 4)		74BCT $T_A = Com$, $V_{CC} = Com$, $C_L = 250$ pF, 8 Outputs Switching (Notes 3, 4)		Units
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0 2.0	10.2 10.2	3.0 3.0	12.0 12.0	4.0 4.0	15.0 15.0	ns
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output				1.5			ns
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output				1.0			ns
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output				5.0			ns
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output				7.0			ns

Extended AC Electrical Characteristics (Continued)

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}).

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device.

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.).

Note 4: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

Capacitance

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Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	V_{CC} = 5.0V
C_{OUT}	Output Pin Capacitance	9.0	pF	V_{CC} = 5.0V

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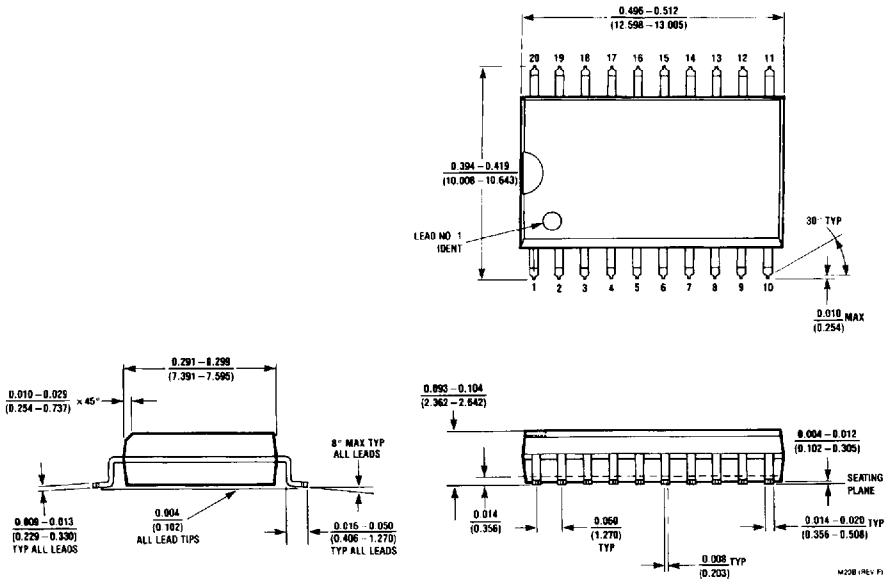
Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:

74BCT 374 P C QR

- 74BCT: Temperature Range Family — 74BCT = Commercial
- 374: Device Type
- P: Package Code — P = Plastic DIP; S = Small Outline (SOIC)
- C: Temperature Range — C = Commercial (0°C to +70°C)
- QR: Special Variations — X = Devices shipped in 13" reels; QR = Commercial grade device with burn-in

Physical Dimensions inches (millimeters)



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

Lit # 114865

Physical Dimensions inches (millimeters) (Continued)

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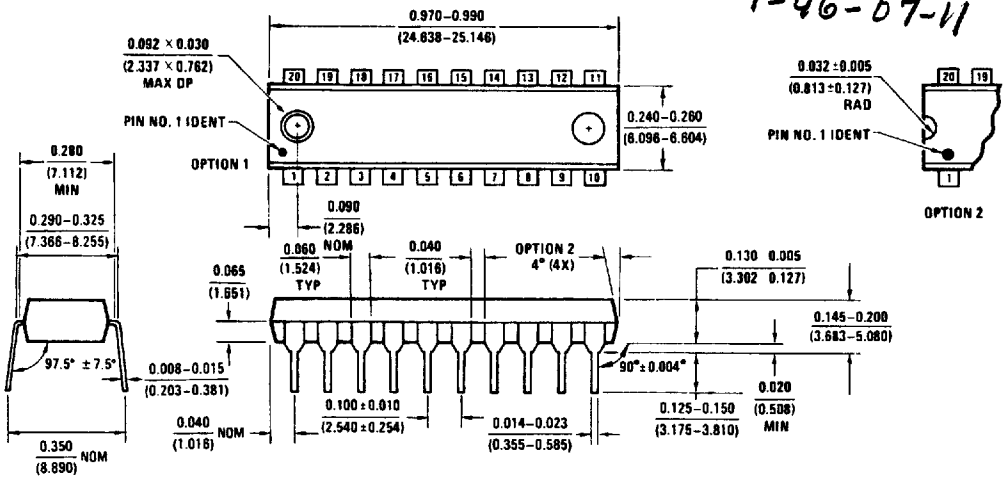

N20B (REV A)

20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

NATIONAL SEMICOND (LOGIC) 49E D

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