NEC

MOS INTEGRATED CIRCUIT

μPD78076Y, 78078Y

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78076Y and 78078Y add the I²C bus control function to the μPD78076 and 78078, and are suitable for application in AV products.

Besides a high-speed, high-performance CPU, these microcontrollers have internal ROM, RAM, I/O ports, 8-bit resolution A/D converter, 8-bit resolution D/A converter, timer, serial interface, real-time output port, interrupt control, and various other peripheral hardware.

A one-time PROM version and an EPROM version (common name: μPD78P078Y), both of which can operate in the same power supply voltage range as the mask ROM version, and various development tools are also available.

The details of the functions are described in the following user's manuals. Be sure to read them before designing.

μPD78078, 78078Y Subseries User's Manual: U10641E

78K/0 Series User's Manual – Instructions: U12326E

FEATURES

- Internal high-capacity ROM and RAM

Item / Part Number	Program Memory (ROM)	Data Memory			Package
		Internal High-Speed RAM	Internal Buffer RAM	Internal Expansion RAM	
μPD78076Y	48 Kbytes	1024 bytes	32 bytes	1024 bytes	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78078Y	60 Kbytes				100-pin plastic LQFP[Note] (14 × 14 mm, resin thickness 1.40 mm)

Note Under development

- External memory expansion space: 64 Kbytes
- Minimum instruction execution time can be changed from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 88 (N-ch open-drain: 8)
- 8-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- Serial interface: 3 channels
  - 3-wire serial I/O, 2-wire serial I/O, and I²C bus mode: 1 channel
  - 3-wire serial I/O mode: 1 channel
  - 3-wire serial I/O and UART mode: 1 channel
- Timer: 7 channels
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Cellular phones, cordless telephones, AV equipment, etc.

Document No. U10605EJ3V0DS00 (3rd edition)
Date Published November 1997 N
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

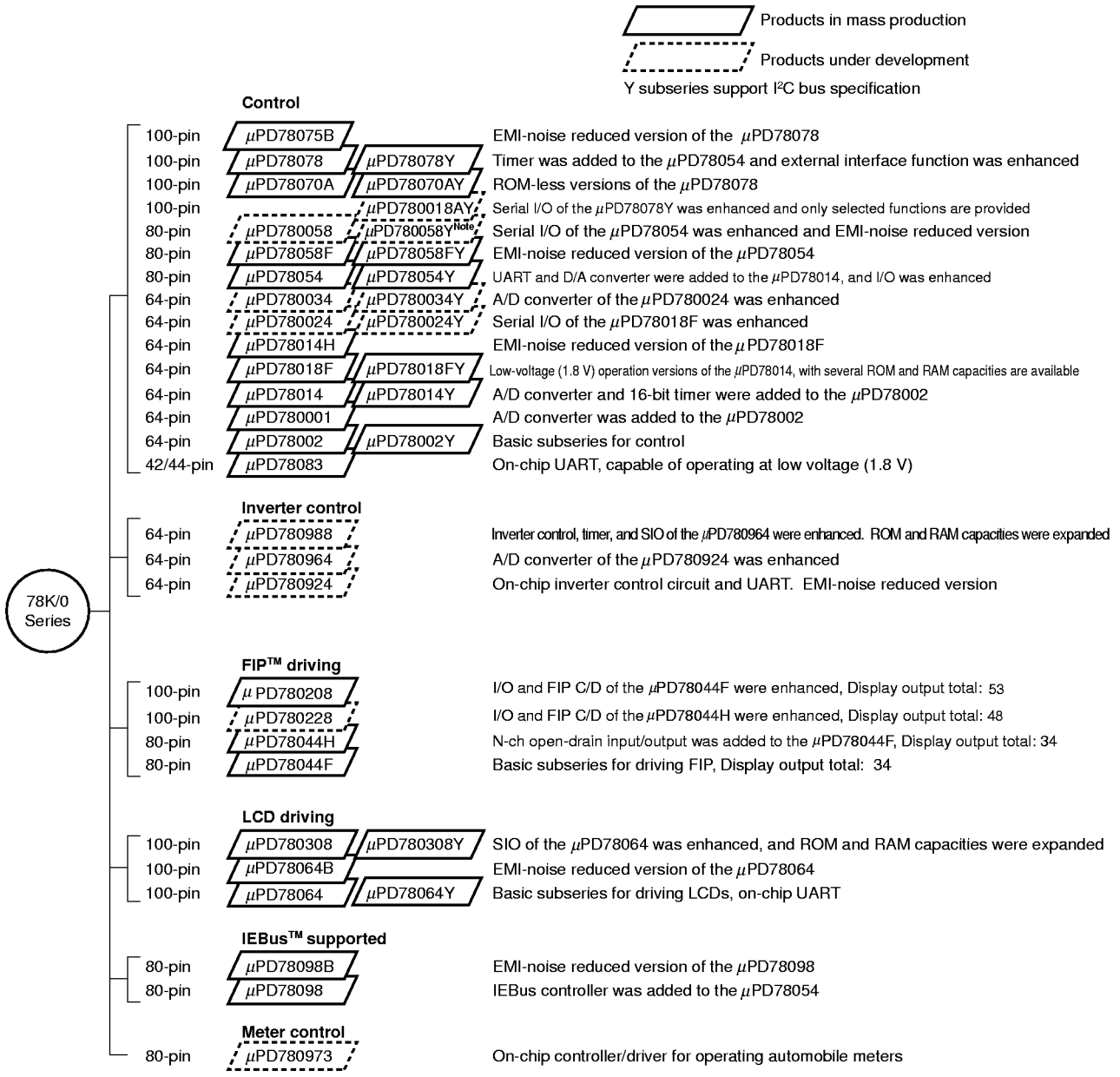
Part Number	Package
μPD78076YGF-×××-3BA	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78076YGC-×××-8EU[Note]	100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness 1.40 mm)
μPD78078YGF-×××-3BA	100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78078YGC-×××-8EU[Note]	100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness 1.40 mm)

Note Under development

Remark ××× indicates the ROM code suffix.

★ 78K/0 SERIES DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Note Under development

The major functional differences among the Y subseries are shown below.

Subseries Name \ Function		ROM Capacity	Serial Interface	I/O	V_{DD} MIN. Value
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I²C : 1 ch	88	1.8 V
	μPD78070AY	—	3-wire with automatic transmit/receive function : 1 ch 3-wire/UART : 1 ch	61	2.7 V
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function : 1 ch Time division 3-wire : 1 ch I²C bus (supports Multimaster) : 1 ch	88	
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I²C : 1 ch 3-wire with automatic transmit/receive function : 1 ch 3-wire/time division UART : 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I²C : 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K	3-wire with automatic transmit/receive function : 1 ch 3-wire/UART : 1 ch		2.0 V
	μPD780034Y	8 K to 32 K	UART : 1 ch	51	1.8 V
	μPD780024Y		3-wire : 1 ch I²C bus (supports Multimaster) : 1 ch		
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I²C/SBI/I²C : 1 ch 3-wire with automatic transmit/receive function : 1 ch	53	
	μPD78014Y	8 K to 32K	3-wire/2-wire/SBI/I²C : 1 ch 3-wire with automatic transmit/receive function : 1 ch		2.7 V
	μPD78002Y	8 K to 16 K	3-wire/2-wire/SBI/I²C : 1 ch		
LCD driving	μPD780308Y	48 K to 60 K	3-wire/2-wire/I²C : 1 ch 3-wire/time division UART : 1 ch 3-wire : 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I²C : 1 ch 3-wire/UART : 1 ch		

Remark Functions except serial interface are common to subseries without Y suffix.

OVERVIEW OF FUNCTION

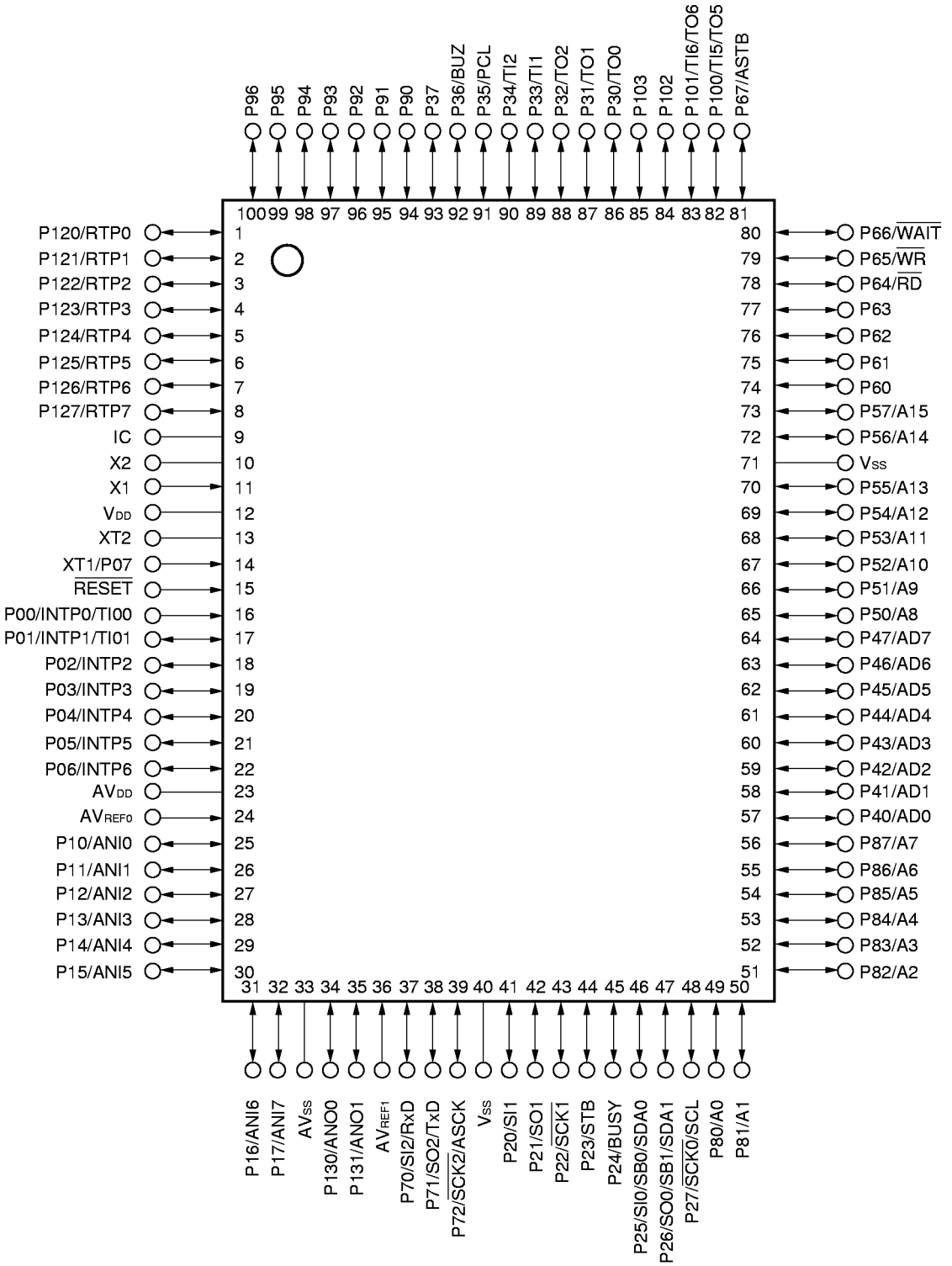
Item \ Part Number		μPD78076Y	μPD78078Y
Internal memory	ROM	48 Kbytes	60 Kbytes
	High-speed RAM	1024 bytes	
	Buffer RAM	32 bytes	
	Expansion RAM	1024 bytes	
Memory space		64 Kbytes	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution		On-chip minimum instruction execution time variable function	
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0-MHz operation)	
	When subsystem clock selected	122 μs (at 32.768-kHz operation)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total : 88 • CMOS input : 2 • CMOS I/O : 78 • N-ch open-drain I/O : 8	
A/D converter		• 8-bit resolution x 8 channels	
D/A converter		• 8-bit resolution x 2 channels	
Serial interface		• 3-wire serial I/O/2-wire serial I/O/I²C bus mode selectable : 1 channel • 3-wire serial I/O mode (up to 32-byte automatic data transmit/receive function is provided) : 1 channel • 3-wire serial I/O/UART mode selectable : 1 channel	
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 4 channels • Watch timer : 1 channel • Watchdog timer : 1 channel	
Timer output		5 (14-bit PWM output × 1, 8-bit PWM output × 2)	
Clock output		• 19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (@ 5.0-MHz operation with main system clock) • 32.768 kHz (@ 32.768-kHz operation with subsystem clock)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (@ 5.0-MHz operation with main system clock)	
Vectored interrupt sources	Maskable	Internal: 15, External: 7	
	Non-maskable	Internal: 1	
	Software	1	
Test input		Internal: 1, External: 1	
Supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		• 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm) • 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness 1.40 mm) Note	

Note Under development

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)**
  μPD78076YGF-×××-3BA, 78078YGF-×××-3BA

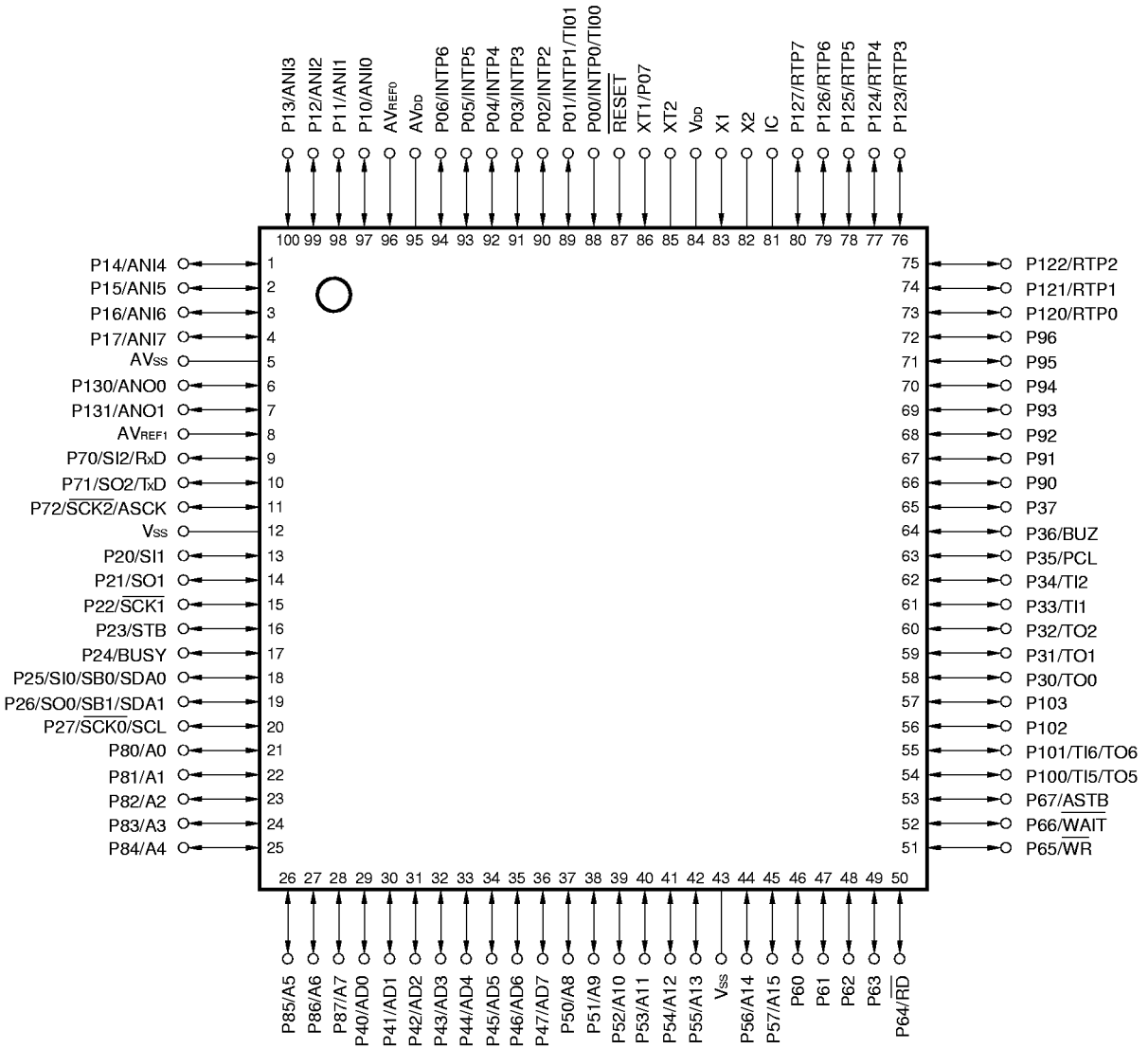


Cautions 1. Connect IC (internally connected) pin directly to VSS.

2. Connect AVDD pin to VDD.

3. Connect AVSS pin to VSS.

- **100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness 1.40 mm)**
  μPD78076YGC-8EU[Note], 78078YGC-8EU[Note]



Note Under development

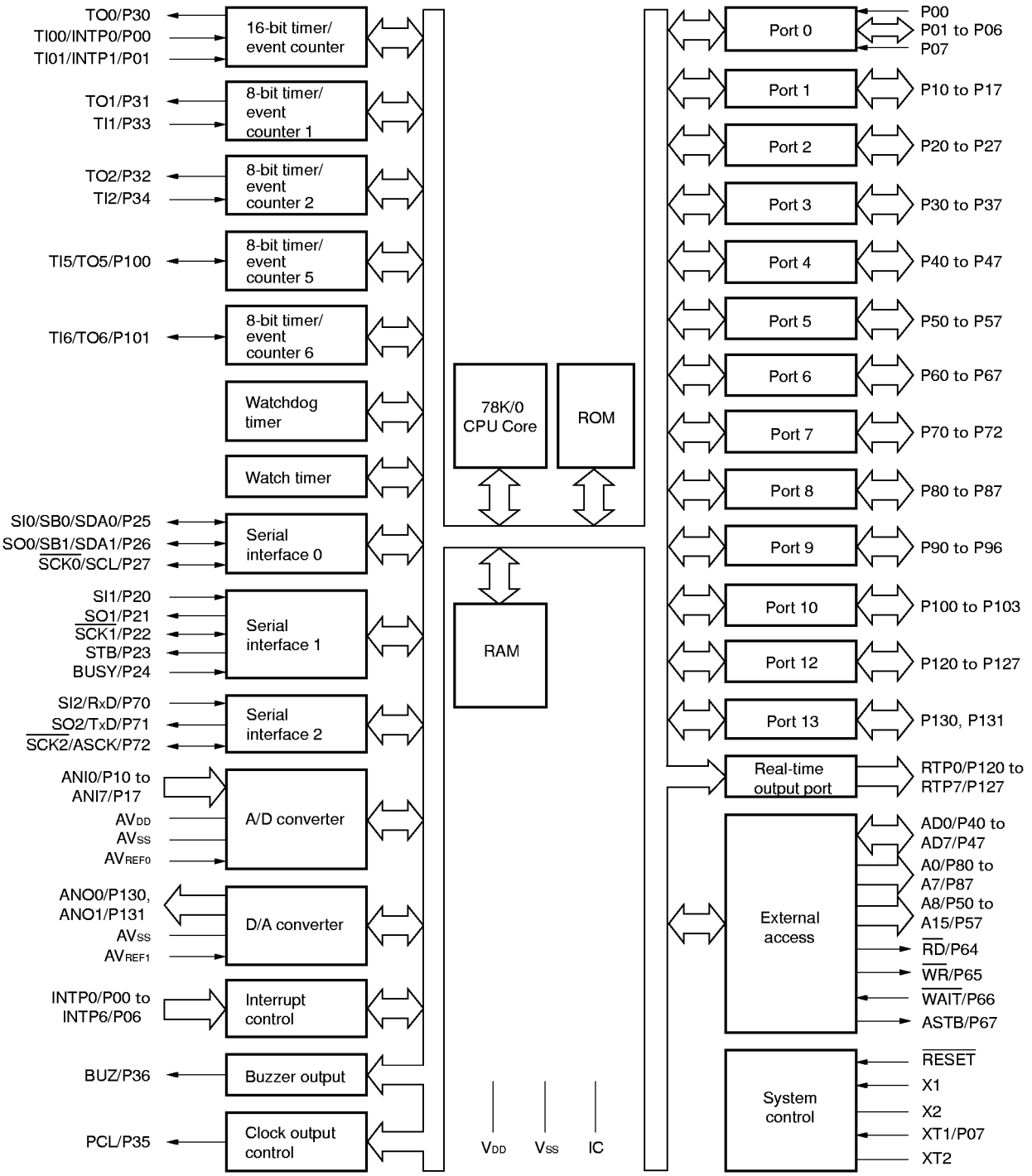
Cautions 1. Connect IC (internally connected) pin directly to VSS.

2. Connect AVDD pin to VDD.

3. Connect AVSS pin to VSS.

A0 to A15	:	Address Bus	P120 to P127	:	Port12
AD0 to AD7	:	Address/Data Bus	P130, P131	:	Port13
ANI0 to ANI7	:	Analog Input	PCL	:	Programmable Clock
ANO0, ANO1	:	Analog Output	$\overline{RD}$	:	Read Strobe
ASCK	:	Asynchronous Serial Clock	$\overline{RESET}$	:	Reset
ASTB	:	Address Strobe	RTP0 to RTP7	:	Real-Time Output Port
AV_{DD}	:	Analog Power Supply	RxD	:	Receive Data
AV_{REF0}, AV_{REF1}	:	Analog Reference Voltage	SB0, SB1	:	Serial Bus
AV_{SS}	:	Analog Ground	$\overline{SCK0}$ to $\overline{SCK2}$	:	Serial Clock
BUSY	:	Busy	SCL	:	Serial Clock
BUZ	:	Buzzer Clock	SDA0, SDA1	:	Serial Data
IC	:	Internally Connected	SI0 to SI2	:	Serial Input
INTP0 to INTP6	:	Interrupt from Peripherals	SO0 to SO2	:	Serial Output
P00 to P07	:	Port0	STB	:	Strobe
P10 to P17	:	Port1	TI00, TI01	:	Timer Input
P20 to P27	:	Port2	TI1, TI2, TI5, TI6	:	Timer Input
P30 to P37	:	Port3	TO0 to TO2, TO5, TO6	:	Timer Output
P40 to P47	:	Port4	TxD	:	Transmit Data
P50 to P57	:	Port5	V_{DD}	:	Power Supply
P60 to P67	:	Port6	V_{SS}	:	Ground
P70 to P72	:	Port7	$\overline{WAIT}$	:	Wait
P80 to P87	:	Port8	$\overline{WR}$	:	Write Strobe
P90 to P96	:	Port9	X1, X2	:	Crystal (Main System Clock)
P100 to P103	:	Port10	XT1, XT2	:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM capacity depends on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 8-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.[Note 2]		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK0}}$/SCL
P30	Input/ output	Port 3 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/ output	Port 4 8-bit input/output port Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be used by means of software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P07/XT1 pins as an input port, set to 1 bit 6 (FRC) of the processor clock control register (PCC). (Do not use the on-chip feedback resistor of the subsystem clock oscillator.)

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, set port 1 to the input mode. At this time, on-chip pull-up resistor is automatically disconnected.

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P50 to P57	Input/ output	Port 5 8-bit input/output port LEDs can be driven directly. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	A8 to A15
P60	Input/ output	Port 6 8-bit input/ output port Input/output can be specified bit-wise.	N-ch open-drain input/output port. An on-chip pull-up resistor can be specified by mask option. LEDs can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, an on-chip pull-up resistor can be used by means of software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/ output	Port 7 3-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P80 to P87	Input/ output	Port 8 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	A0 to A7
P90	Input/ output	Port 9 7-bit input/output port Input/output can be specified bit-wise.	N-ch open-drain input/output port. An on-chip pull-up resistor can be specified by mask option. LEDs can be driven directly.	Input	—
P91					
P92					
P93					
P94			When used as an input port, an on-chip pull-up resistor can be used by means of software.		
P95					
P96					
P100	Input/ output	Port 10 4-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	TI5/TO5
P101					TI6/TO6
P102, P103					—
P120 to P127	Input/ output	Port 12 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	RTP0 to RTP7
P130, P131	Input/ output	Port 13 2-bit input/output port Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.		Input	ANO0, ANO1

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input	Input	P25/SB0/SDA0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output	Input	P26/SB1/SDA1
SO1				P21
SO2				P71/TxD
SB0	Input/ output	Serial interface serial data input/output	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input/	Serial interface serial clock input/output	Input	P27/SCL
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
RxD	Input	Asynchronous serial interface serial data input	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TI5		External count clock input to 8-bit timer (TM5)		P100/TO5
TI6		External count clock input to 8-bit timer (TM6)		P101/TO6
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
TO5		8-bit timer (TM5) output (also used for 8-bit PWM output)		P100/TI5
TO6		8-bit timer (TM6) output (also used for 8-bit PWM output)		P101/TI6
PCL	Output	Clock output (for main system clock, subsystem clock trimming)	Input	P35
BUZ	Output	Buzzer output	Input	P36

3.2 Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
RTP0 to RTP7	Output	Real-time output port from which data is output in synchronization with a trigger	Input	P120 to P127
AD0 to AD7	Input/ output	Low-order address/data bus at external memory expansion	Input	P40 to P47
A0 to A7	Output	Low-order address bus at external memory expansion	Input	P80 to P87
A8 to A15	Output	High-order address bus at external memory expansion	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output	Input	P64
$\overline{WR}$		External memory write operation strobe signal output		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ASTB	Output	Strobe output which externally latches the address information to ports 4, 5, and 8 to access external memory	Input	P67
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input	—	—
AV_{REF1}	Input	D/A converter reference voltage input	—	—
AV_{DD}	—	A/D converter analog power supply. Connect to V_{DD}.	—	—
AV_{SS}	—	A/D converter and D/A converter ground potential. Connect to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Crystal resonator connection for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Crystal resonator connection for subsystem clock oscillation	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{SS}	—	Ground potential	—	—
IC	—	Internally connected. Connect directly to V_{SS}.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits (1/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	Input/output	Independently connect to V_{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connected to V_{DD}.
P10/ANI0 to P17/ANI7	11	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/output	Independently connect to V_{DD} via a resistor.
P50/A8 to P57/A15	5-A	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P60 to P63	13-B	Input/output	Independently connect to V_{DD} via a resistor.
P64/$\overline{RD}$	5-A	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 3-1. Types of Pin Input/Output Circuits (2/2)

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection for Unused Pins
P70/SI2/RxD	8-A	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P80/A0 to P87/A7	5-A		
P90 to P93	13-B	Input/output	Independently connect to V_{DD} via a resistor.
P94 to P96	5-A	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102, P103	5-A		
P120/RTP0 to P127/RTP7			
P130/ANO0, P131/ANO1	12-A	Input/output	Independently connect to V_{SS} via a resistor.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
IC			Connect directly to V_{SS}.

Figure 3-1. Pin Input/Output Circuits (1/2)

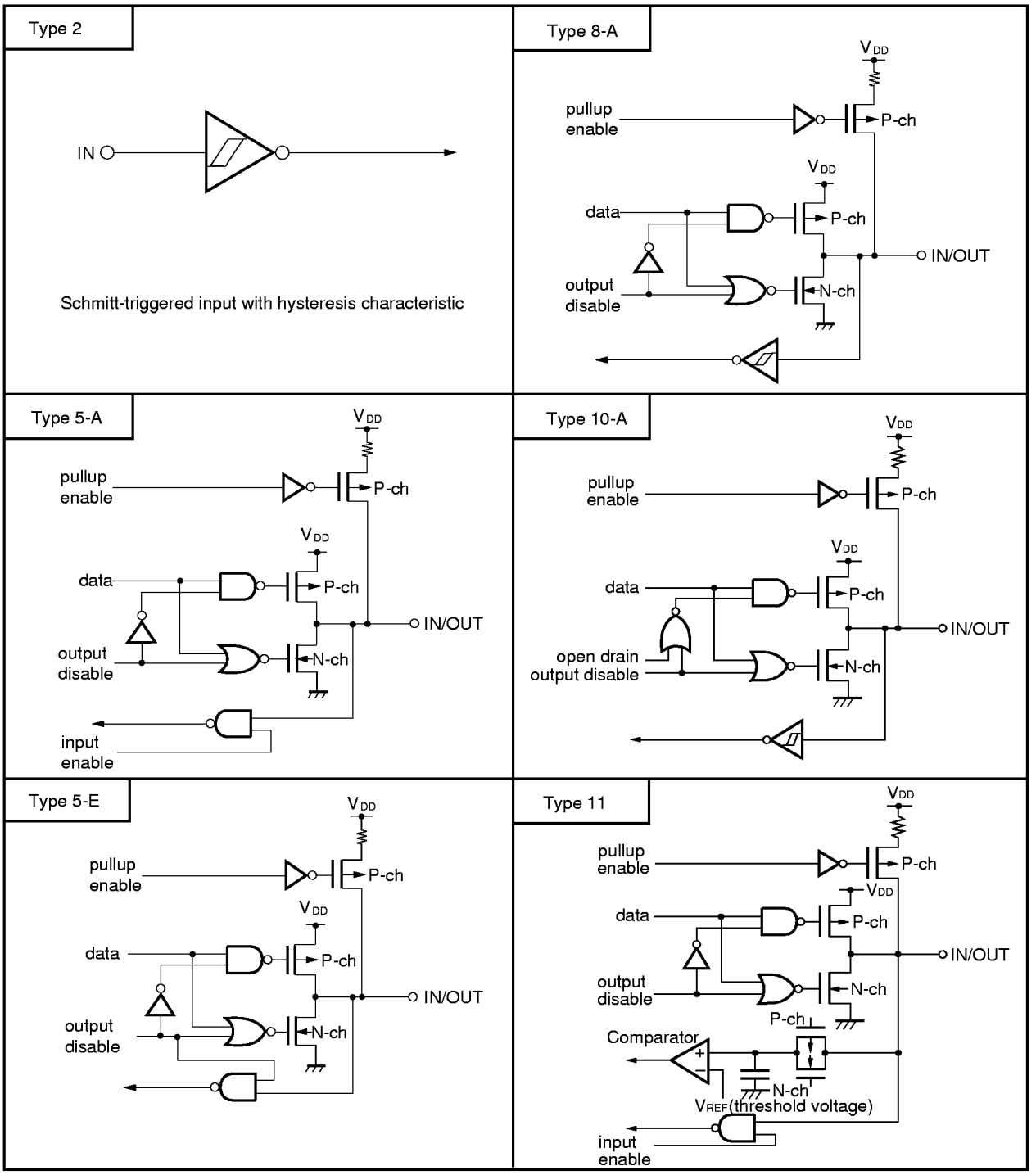
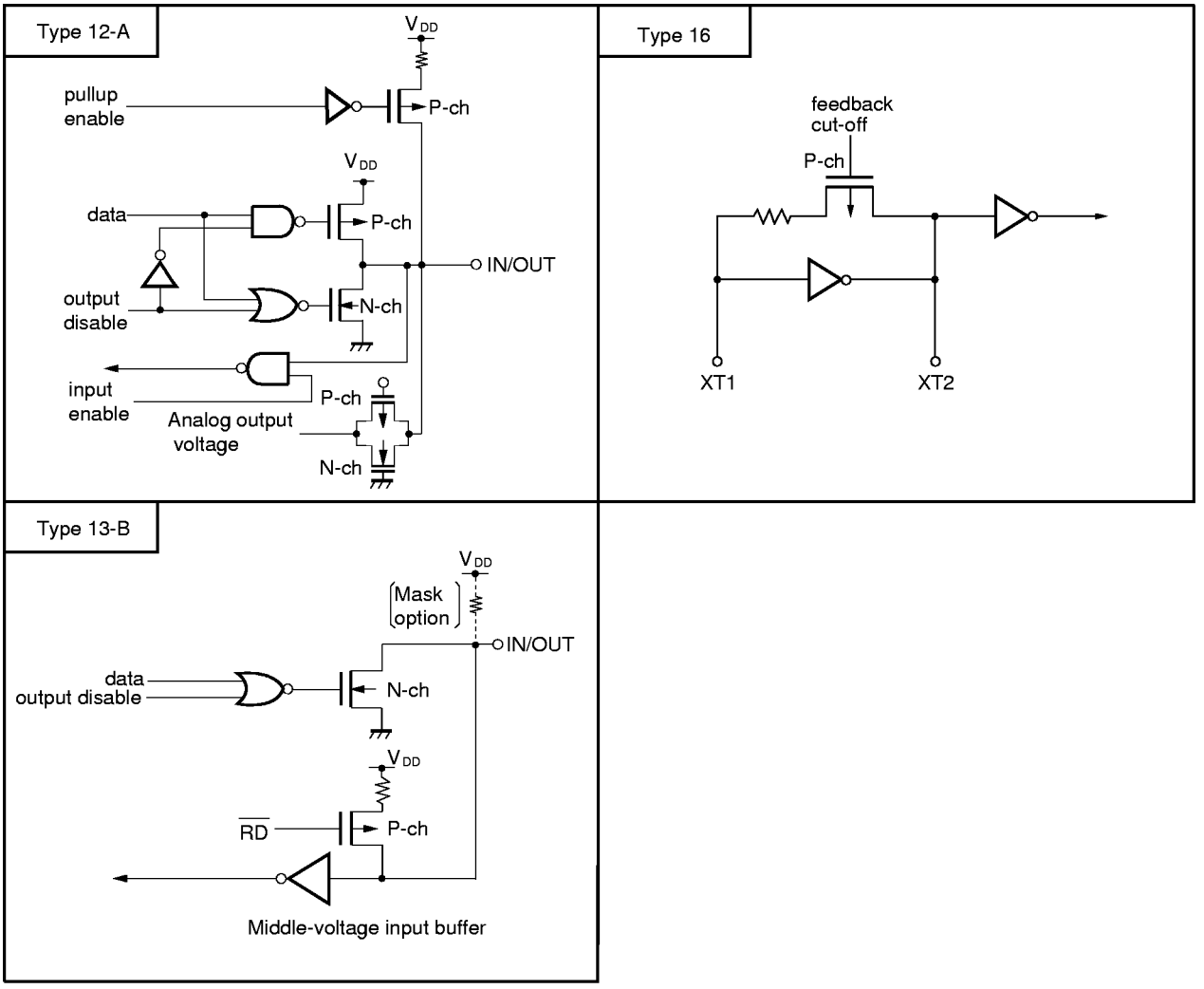


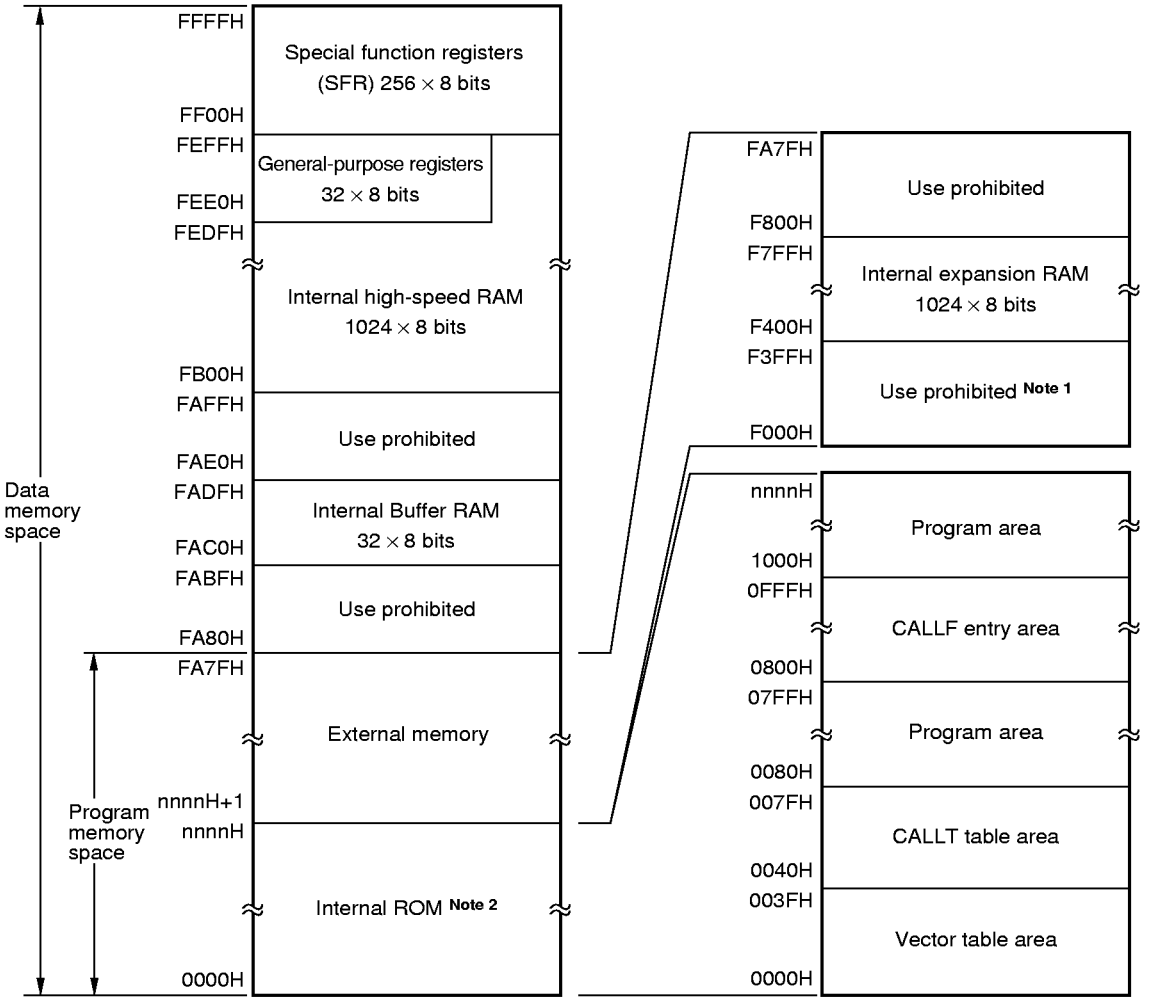
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

The memory map of the μPD78076Y and 78078Y is shown in Figure 4-1.

Figure 4-1. Memory Map



Notes 1. If external device expansion functions are to be employed for the μPD78078Y, set the size of the internal ROM to 56 Kbytes or below using the memory size switching register (IMS).

2. The internal ROM capacity depends on the product. (See the following table.)

Part Number	Internal ROM Last Address nnnnH
μPD78076Y	BFFFH
μPD78078Y	EFFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Input/output ports are classified into three types.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01 to P06, Port 1 to 5, P64 to P67, Port 7, Port 8, P94 to P96, Port 10, Port 12, Port 13) : 78
- N-ch open-drain input/output (P60 to P63, P90 to P93) : 8

Total : 88

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P00, P07	Input only.
	P01 to P06	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 1	P10 to P17	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 2	P20 to P27	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 3	P30 to P37	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 4	P40 to P47	Input/output port. Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be used by means of software. The test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software. LEDs can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. An on-chip pull-up resistor can be used by mask option. LEDs can be driven directly.
	P64 to P67	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 7	P70 to P72	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 8	P80 to P87	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 9	P90 to P93	N-ch open-drain input/output port. Input/output can be specified bit-wise. An on-chip pull-up resistor can be used by mask option. LEDs can be driven directly.
	P94 to P96	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 10	P100 to P103	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 12	P120 to P127	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.
Port 13	P130, P131	Input/output port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be used by means of software.

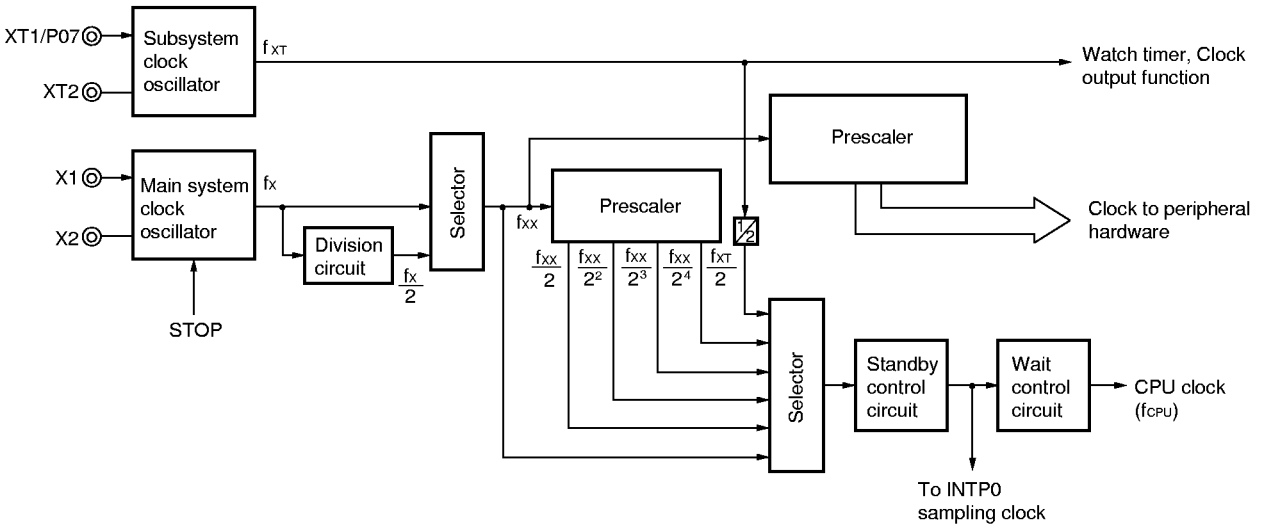
5.2 Clock Generator

There are two kinds of clock generators: main system and subsystem clock generators.

It is possible to change the minimum instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock frequency of 5.0 MHz)
- 122 μs (at subsystem clock frequency of 32.768 kHz)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

There are the following seven timer/event counter channels:

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 4 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Operations of Timer/Event Counters

		16-bit Timer/Event Counter	8-bit Timer/Event Counters 1, 2	8-bit Timer/Event Counters 5, 6	Watch Timer	Watchdog Timer
Operation mode	Interval timer	1 channel	2 channels	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	2 channels	—	—
Function	Timer output	1 output	2 outputs	2 outputs	—	—
	PWM output	1 output	—	2 outputs	—	—
	Pulse width measurement	2 inputs	—	—	—	—
	Square wave output	1 output	2 outputs	2 outputs	—	—
	One-shot pulse output	1 output	—	—	—	—
	Interrupt request	2	2	2	1	1
	Test input	—	—	—	1 input	—

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

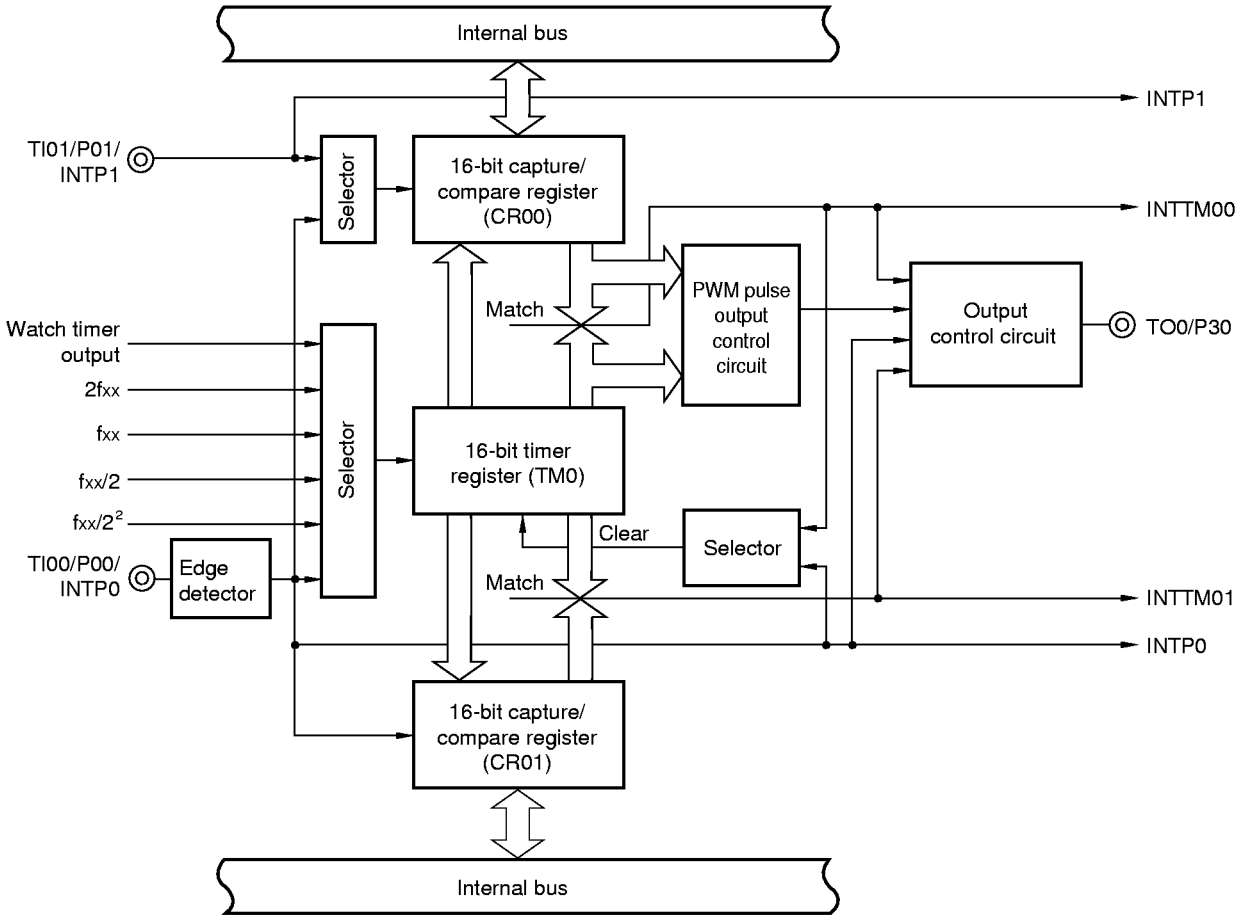


Figure 5-3. 8-Bit Timer/Event Counters 1, 2 Block Diagram

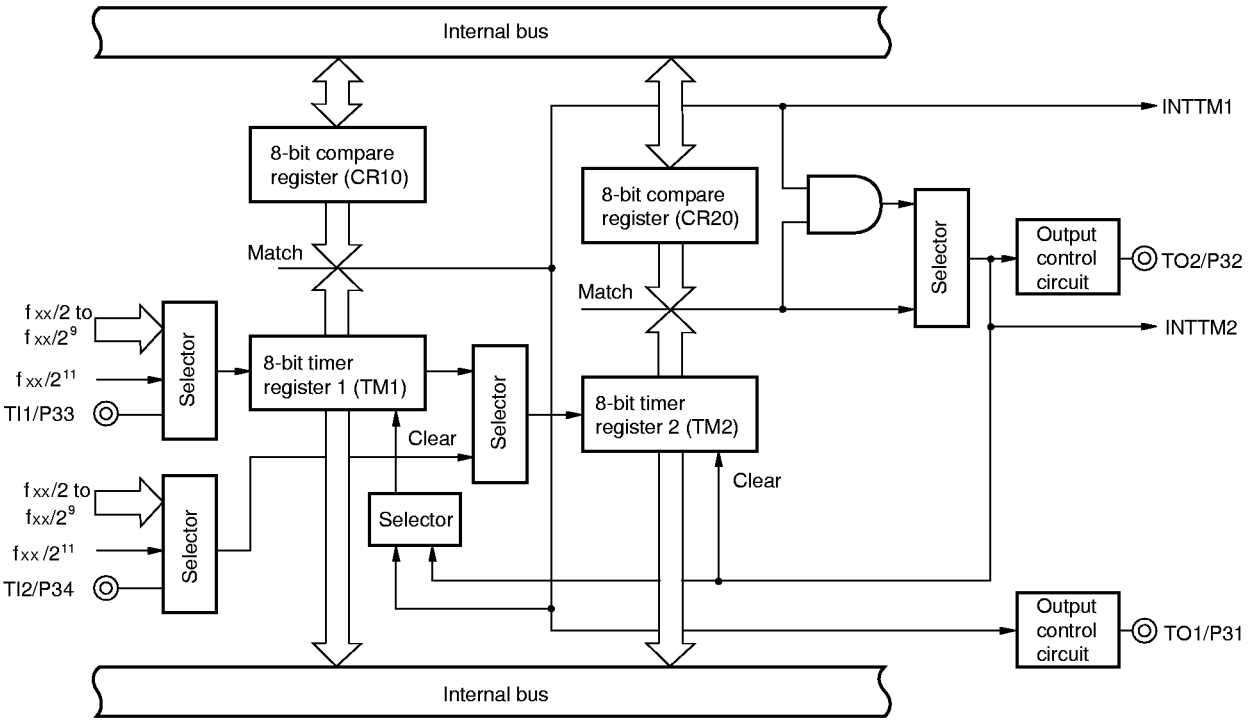
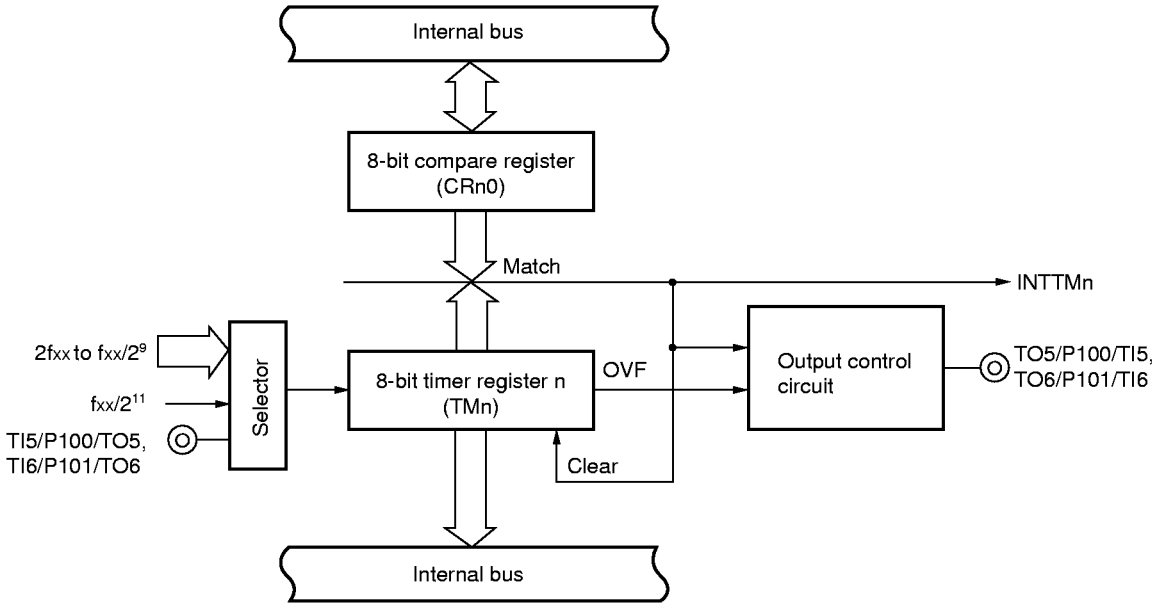


Figure 5-4. 8-Bit Timer/Event Counters 5, 6 Block Diagram



n = 5, 6

Figure 5-5. Watch Timer Block Diagram

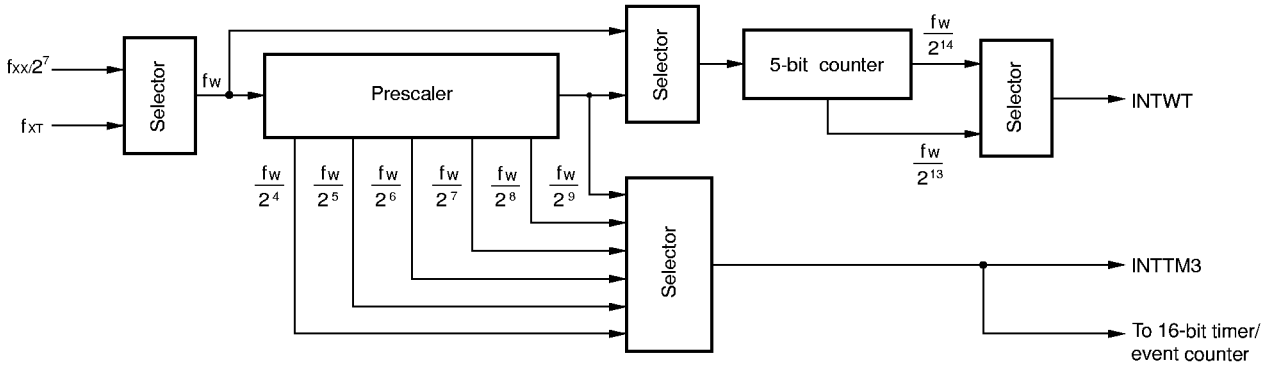
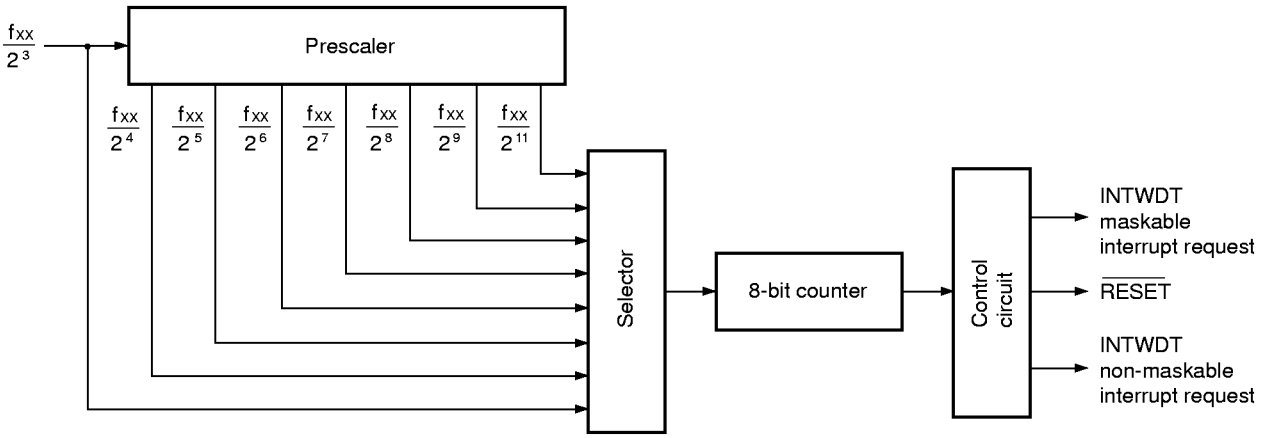


Figure 5-6. Watchdog Timer Block Diagram

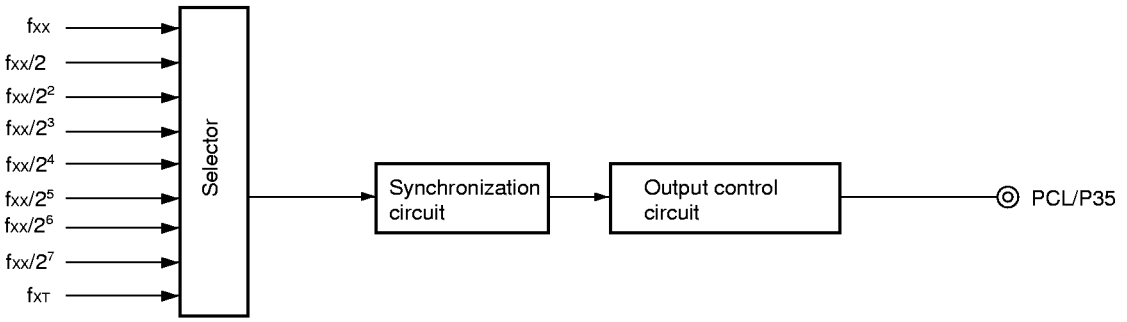


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (at main system clock frequency of 5.0 MHz)
- 32.768 kHz (at subsystem clock frequency of 32.768 kHz)

Figure 5-7. Clock Output Control Circuit Block Diagram

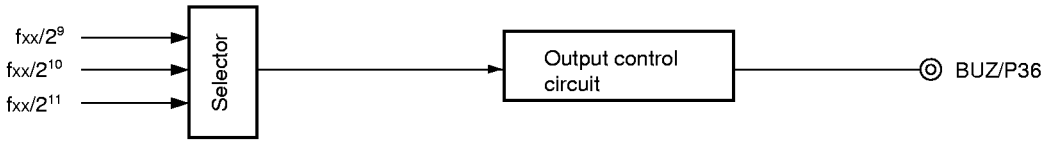


5.5 Buzzer Output Control Circuit

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (at main system clock frequency of 5.0 MHz)

Figure 5-8. Buzzer Output Control Circuit Block Diagram



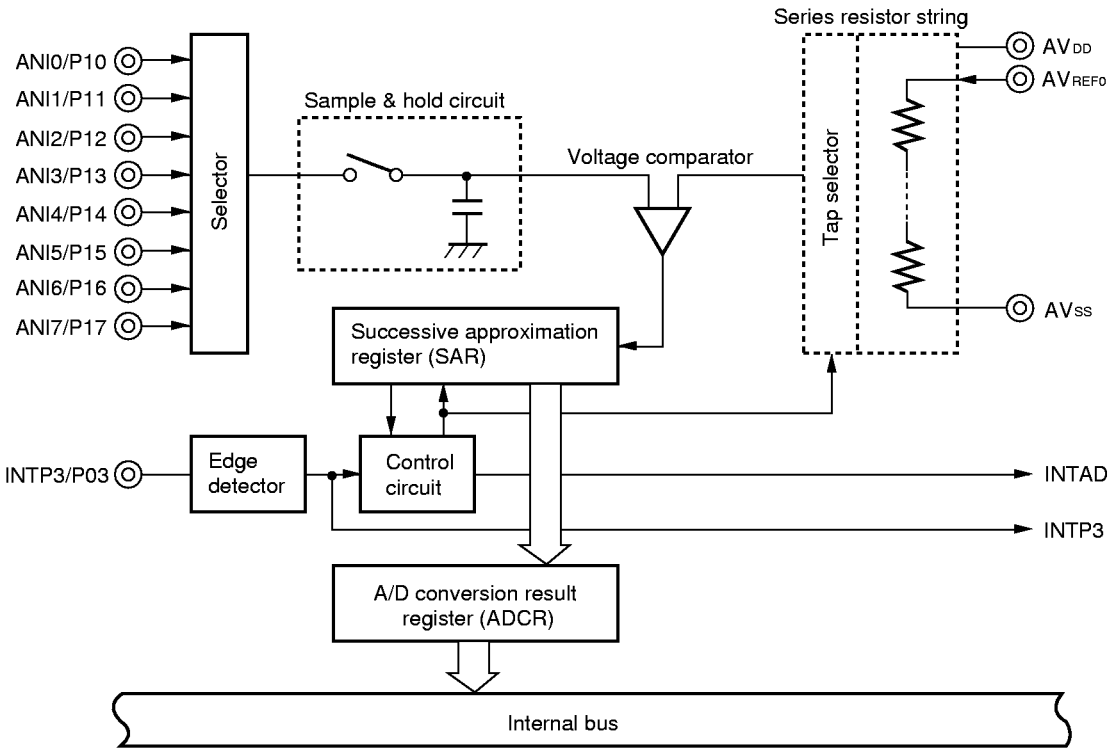
5.6 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

Figure 5-9. A/D Converter Block Diagram

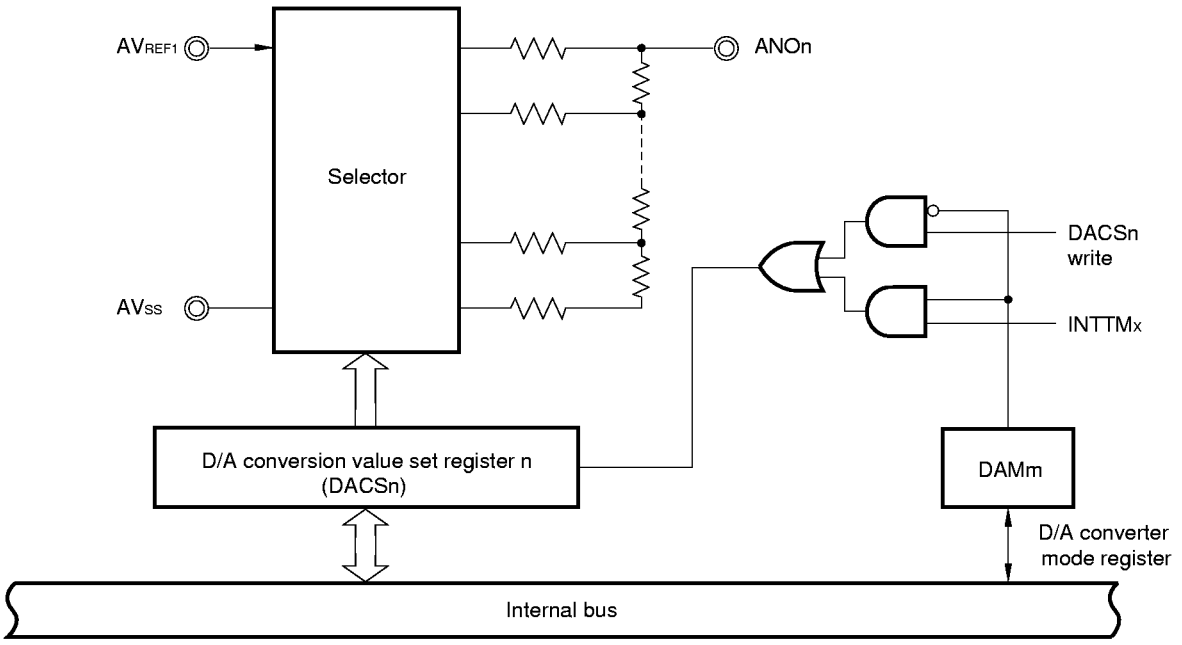


5.7 D/A Converter

The D/A converter consists of two 8-bit resolution channels.

The conversion method is the R-2R resistor ladder method.

Figure 5-10. D/A Converter Block Diagram



n = 0, 1
m = 4, 5
x = 1, 2

5.8 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interfaces

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	√ (MSB/LSB first switching possible)	√ (MSB/LSB first switching possible)	√ (MSB/LSB first switching possible)
3-wire serial I/O mode with automatic data transmit/ receive function	—	√ (MSB/LSB first switching possible)	—
2-wire serial I/O mode	√ (MSB first)	—	—
I²C bus mode	√ (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	(On-chip dedicated baud rate generator)

Figure 5-11. Serial Interface Channel 0 Block Diagram

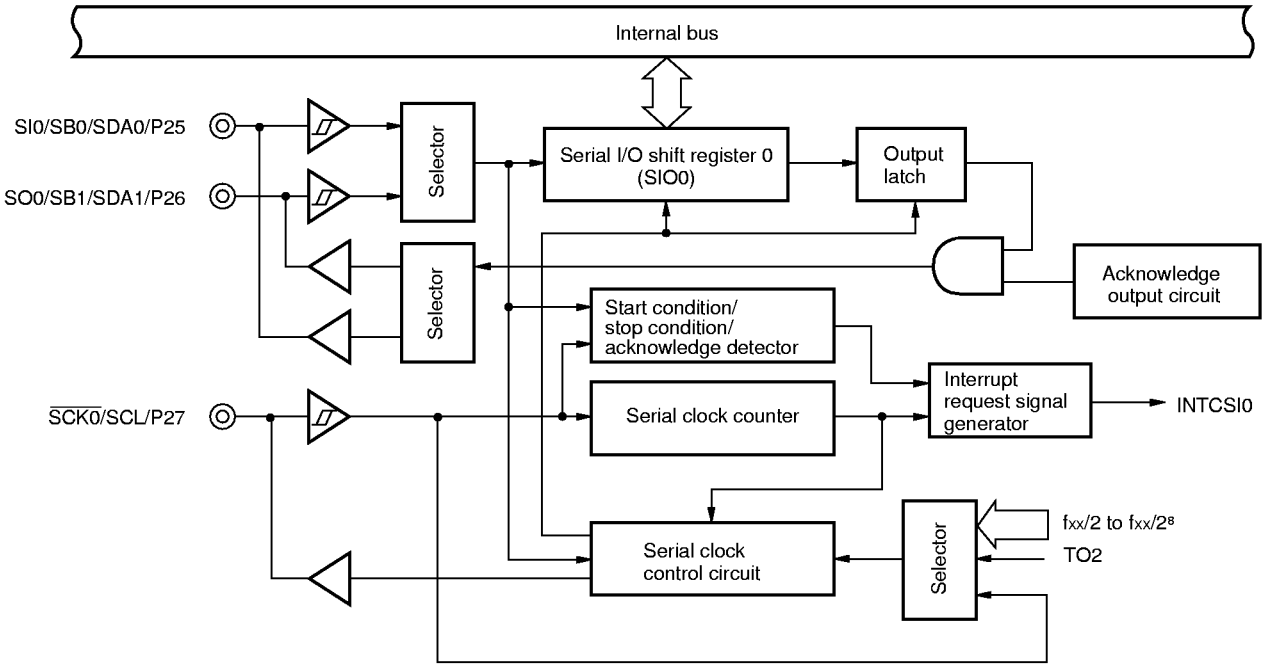


Figure 5-12. Serial Interface Channel 1 Block Diagram

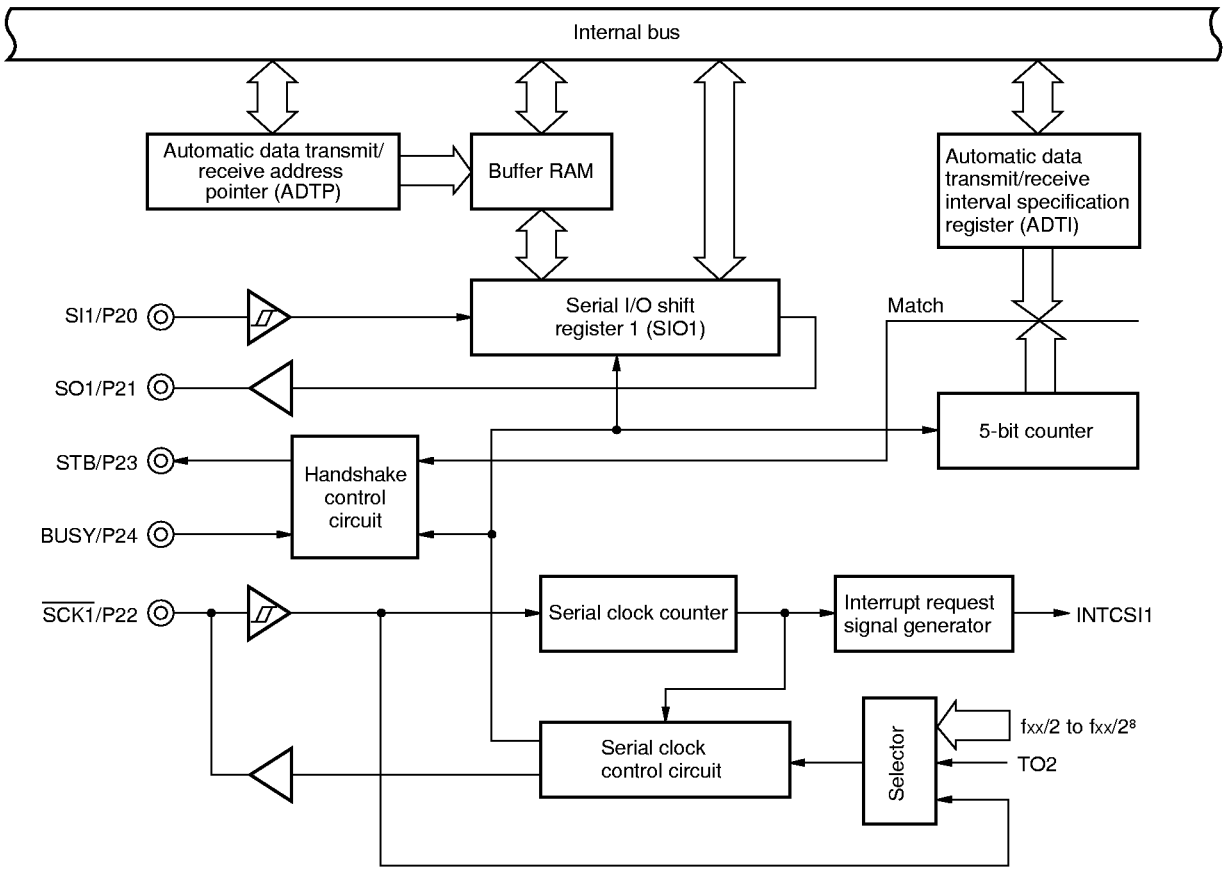
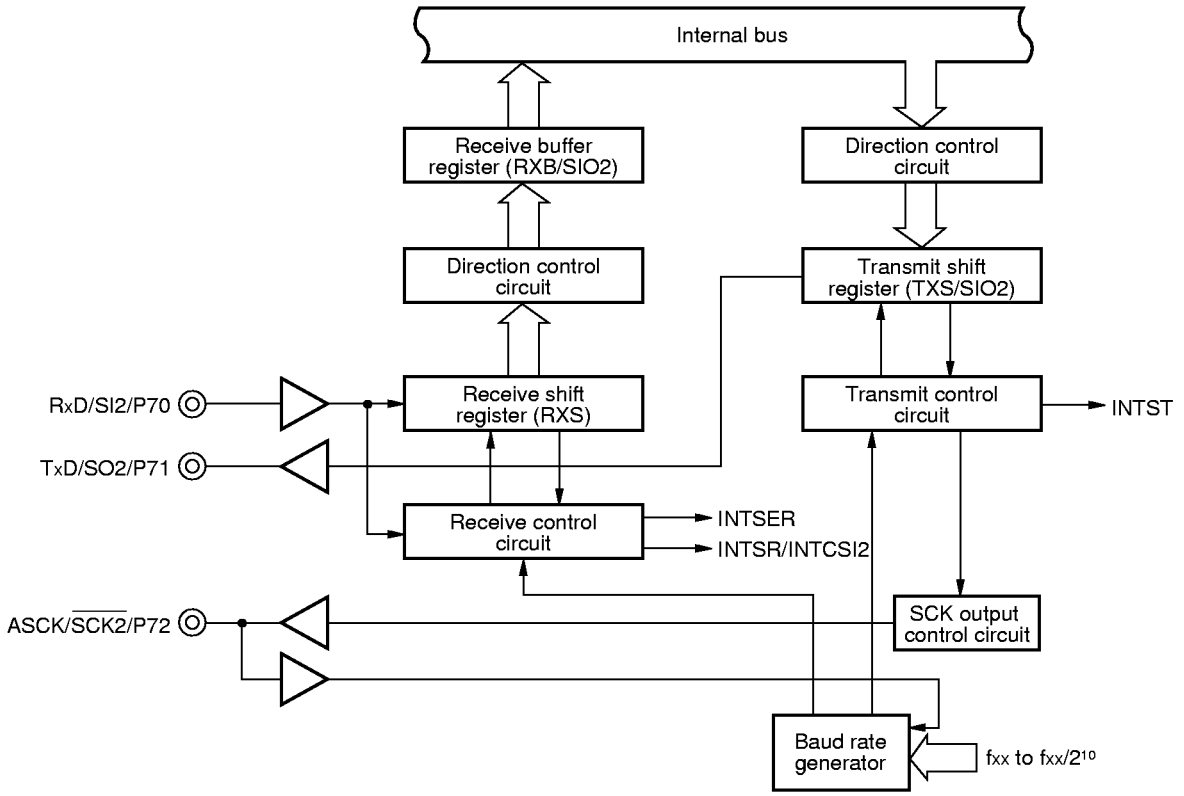


Figure 5-13. Serial Interface Channel 2 Block Diagram

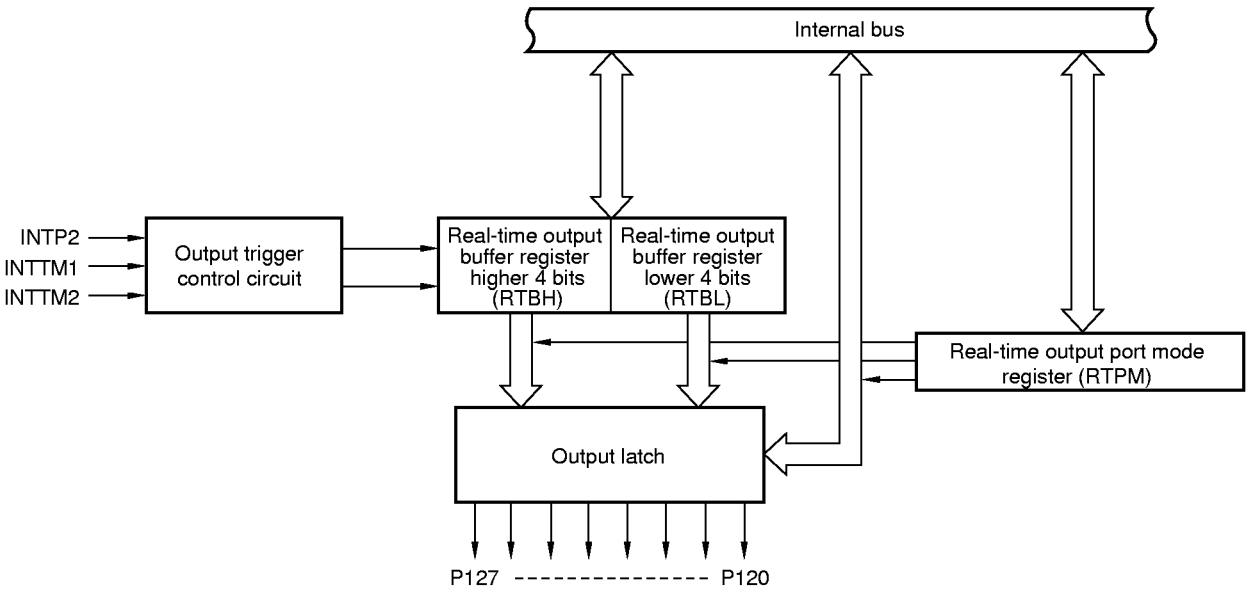


5.9 Real-time Output Port

Data set previously in the real-time output buffer is transferred to the output latch by hardware concurrently with timer interrupt request or external interrupt request generation in order to output to off-chip. This is a real-time output function. Pins used to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motor, etc.

Figure 5-14. Real-time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

A total of 24 interrupt sources are provided, divided into the following three types.

- Non-maskable interrupt : 1
- Maskable interrupt : 22
- Software interrupt : 1

Table 6-1. List of Interrupt Sources

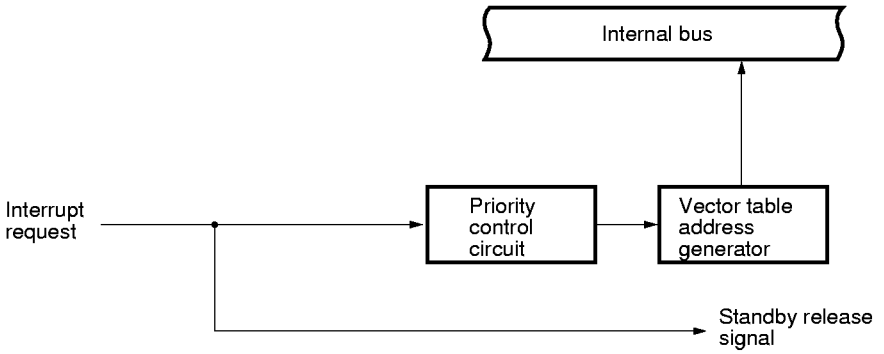
Interrupt Type	Default Priority [Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type [Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (When the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (When the interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	Completion of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	Completion of serial interface channel 1 transfer		0016H	
	10	INTSER	Occurrence of serial interface channel 2 UART reception error		0018H	
	11	INTSR	Completion of serial interface channel 2 UART reception		001AH	
		INTCSI2	Completion of serial interface channel 2 3-wire transfer			
	12	INTST	Completion of serial interface channel 2 UART transmission		001CH	
	13	INTTM3	Reference interval signal from watch timer		001EH	
	14	INTTM00	Generation of matching signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of matching signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of matching signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of matching signal of 8-bit timer/event counter 2		0026H	
	18	INTAD	Completion of A/D conversion		0028H	
	19	INTTM5	Generation of matching signal of 8-bit timer/event counter 5		002AH	
	20	INTTM6	Generation of matching signal of 8-bit timer/event counter 6		002CH	
Software	—	BRK	Execution of BRK instruction	—	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 20 is the lowest order.

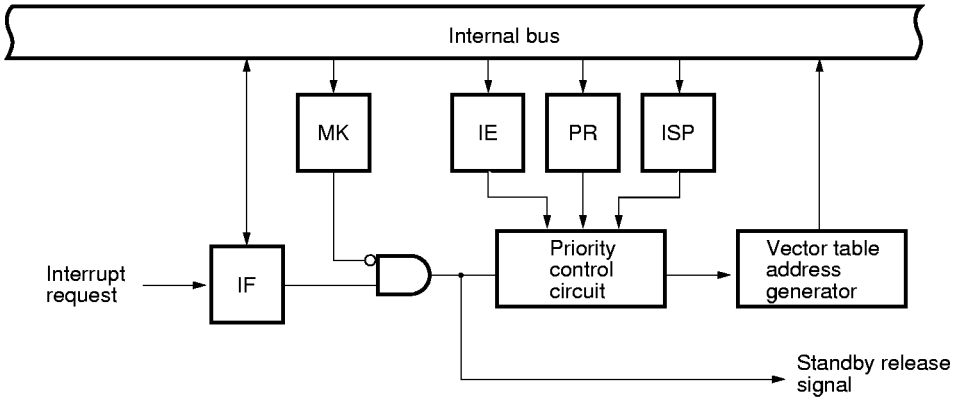
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

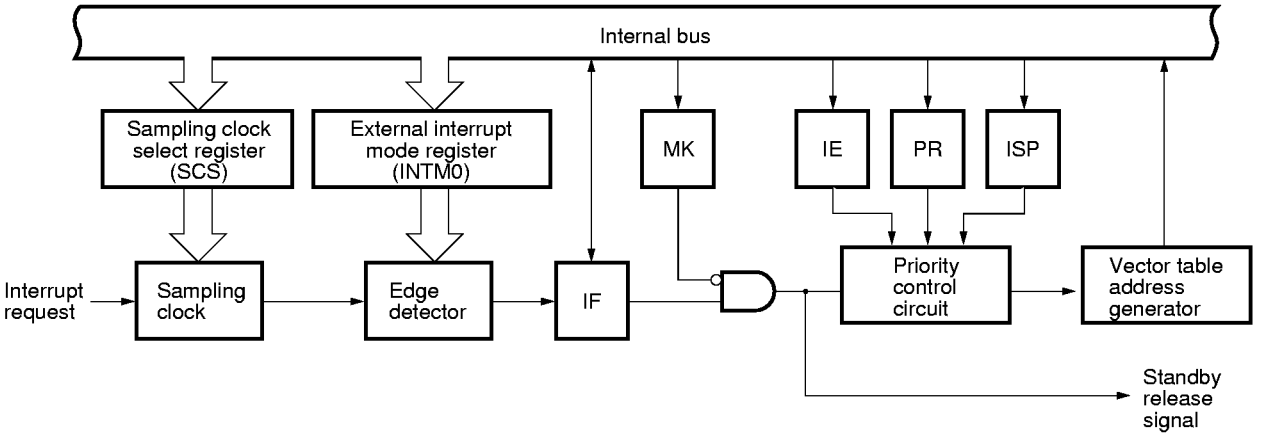
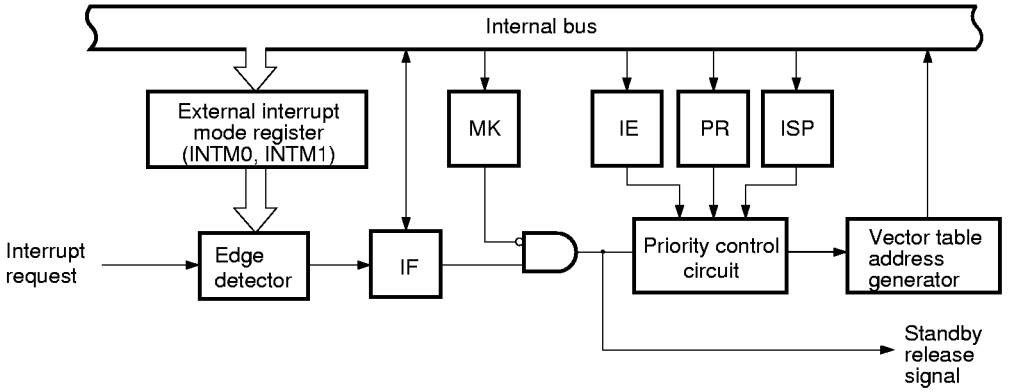
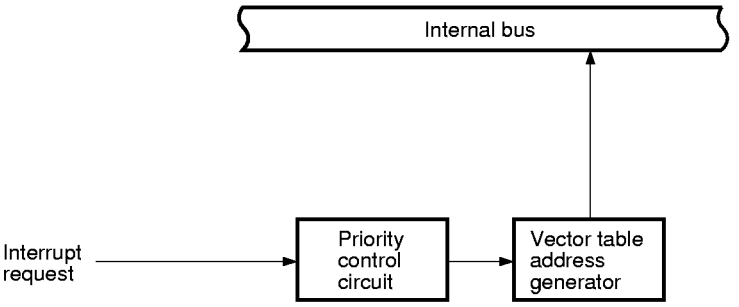


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
E : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

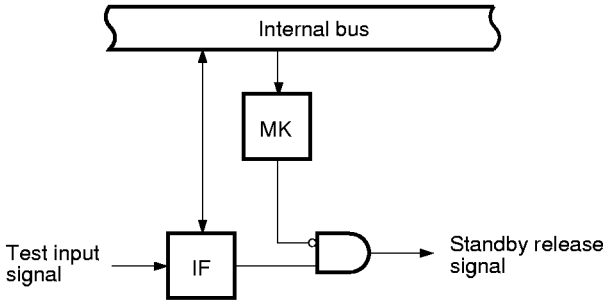
6.2 Test Functions

Table 6-2 shows the two test functions available.

Table 6-2. Test Input Factors

Test Input Factor		Internal/ External
Name	Trigger	
INTWT	Overflow of watch timer	Internal
INTPT4	Detection of falling edge of port 4	External

Figure 6-2. Basic Configuration of Test Function



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR.

External devices connection uses ports 4 to 6 and port 8.

The external device expansion function has the following two modes:

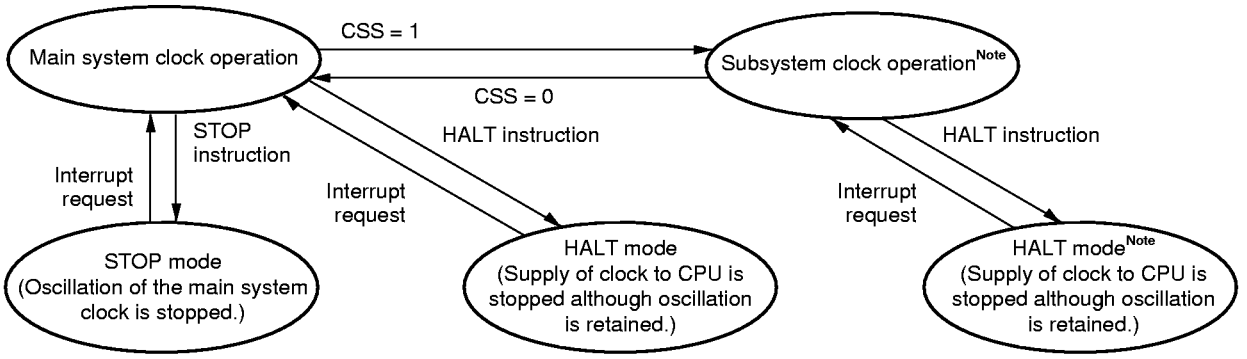
- Separate bus mode : External devices are connected by using an independent address bus and data bus. Because an external latch circuit is not necessary, this mode is effective for reducing the number of components and the mounting area on a printed wiring board.
- Multiplexed bus mode : External devices are connected by using a time-division multiplexed address/data bus. This mode can reduce the number of ports used when external devices are connected.

8. STANDBY FUNCTION

The standby function is designed to reduce current consumption. It has the following two modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode : In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used for extremely small power consumption.

Figure 8-1. Standby Function



Note Current consumption can be reduced by shutting off the main system clock.
If the CPU is operating on the subsystem clock, shut off the main system clock by setting MCC (bit 7 in the processor clock control register (PCC)). In this case, a STOP instruction cannot be used.

Caution When switching on the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to provide enough time for oscillation stabilization with the program first.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

1st Operand \ 2nd Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			−0.3 to +7.0	V
	AV_{DD}			−0.3 to V_{DD} + 0.3	V
	AV_{REF0}			−0.3 to V_{DD} + 0.3	V
	AV_{REF1}			−0.3 to V_{DD} + 0.3	V
	AV_{SS}			−0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63, P90 to P93	N-ch open-drain	−0.3 to +16	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} − 0.3 to AV_{REF0} + 0.3	V
Output leakage current, high	I_{OH}	Per pin		−10	mA
		Total for P30 to P37, P56, P57, P60 to P67, P90 to P96, P100 to P103, P120 to P127		−15	mA
		Total for P01 to P06, P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P80 to P87, P130, P131		−15	mA
Output leakage current, low	I_{OL} Note	Per pin	Peak value	30	mA
			r.m.s.	15	mA
		Total for P50 to P55	Peak value	100	mA
			r.m.s.	70	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			r.m.s.	70	mA
		Total for P30 to P37, P64 to P67, P90 to P96, P100 to P103, P120 to P127	Peak value	100	mA
			r.m.s.	70	mA
		Total for P20 to P27, P40 to P47, P80 to P87	Peak value	50	mA
			r.m.s.	20	mA
		Total for P01 to P06, P10 to P17, P70 to P72, P130, P131	Peak value	50	mA
			r.m.s	20	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note The r.m.s. (root mean square) should be calculated as follows: [r.m.s.] = [Peak value] × $\sqrt{\text{duty}}$

Caution Product quality may suffer if the absolute maximum ratings are exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

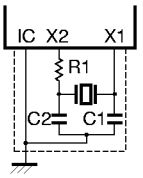
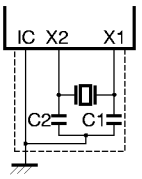
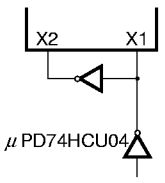
Remark The characteristics of an alternate function pin are the same as those of port pins unless otherwise specified.

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131			15	pF
			P60 to P63, P90 to P93			20	pF

Remark The characteristics of an alternate function pin are the same as those of port pins unless otherwise specified.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		5.0	MHz
		X1 input high/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC CHARACTERISTICS** for instruction execution time.

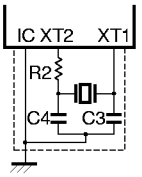
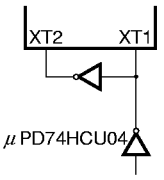
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should always be the same as that of V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC CHARACTERISTICS** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should always be the same as that of Vss.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillator is designed to be a circuit with a low amplification level, for low power consumption more prone to malfunction due to noise than that of the main system clock. Therefore, when using the subsystem clock, take special cautions for wiring methods.

RECOMMENDED OSCILLATOR CONSTANT

MAIN SYSTEM CLOCK : CERAMIC RESONATOR (T_A = –45 to +85°C)

Manufacturer	Part Number	Frequency	Recommended Circuit Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
TDK	CCR1000K2	1.00 MHz	150	150	0	2.0	5.5	Surface mount type
	CCR4.0MC3	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor Surface mount type
	FCR4.0MC5	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor Insertion type
	CCR5.00MC3	5.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor Surface mount type
	FCR5.00MC5	5.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor Insertion type
Murata Mfg. Corporation	CSB1000J	1.00 MHz	100	100	5.6	2.2	5.5	Insertion type
	CSA2.00MG040	2.00 MHz	100	100	0	1.9	5.5	Insertion type
	CST2.00MG040	2.00 MHz	On-chip	On-chip	0	1.9	5.5	On-chip capacitor Insertion type
	CSA4.00MG	4.00 MHz	30	30	0	1.8	5.5	Insertion type
	CST4.00MGW	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor Insertion type
	CSA5.00MG	5.00 MHz	30	30	0	2.0	5.5	Insertion type
	CST5.00MGW	5.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor Insertion type

MAIN SYSTEM CLOCK : CERAMIC RESONATOR (T_A = –20 to +80°C)

Manufacturer	Part Number	Frequency	Recommended Circuit Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Kyocera Corporation	KBR-1000F	1.00 MHz	150	150	0	2.3	5.5	Insertion type
	KBR-2.0MS	2.00 MHz	82	82	0	2.4	5.5	Insertion type
	PBRC4.00A	4.00 MHz	33	33	0	2.4	5.5	Surface mount type
	PBRC4.00B	4.00 MHz	On-chip	On-chip	0	2.4	5.5	On-chip capacitor Surface mount type
	KBR-4.00MSA	4.00 MHz	33	33	0	2.4	5.5	Insertion type
	KBR-4.00MKS	4.00 MHz	On-chip	On-chip	0	2.4	5.5	On-chip capacitor Insertion type
	PBRC5.00A	5.00 MHz	33	33	0	1.8	5.5	Surface mount type
	PBRC5.00B	5.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor Surface mount type
	KBR-5.00MSA	5.00 MHz	33	33	0	1.8	5.5	Insertion type
	KBR-5.00MKS	5.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor Insertion type

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. The oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1 of 3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63, P90 to P93 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			Note	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P60 to P63, P90 to P93 (N-ch open-drain)	4.5 V≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			2.7 V≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
			Note	0		0.1V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P50 to P57, P60 to P63, P90 to P93	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain, at pulled-up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note For use of P07/XT1 pin as P07, use an inverter to input the reverse phase of P07 to the XT2 pin.

Remark The characteristics of an alternate function pin are the same as those of port pins unless otherwise specified.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2 of 3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63, P90 to P93			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63, P90 to P93			–3 Note 1	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60 to P63, P90 to P93		20	40	90	kΩ
Software pull-up resistor Note 2	R_2	V_{IN} = 0 V, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	4.5 V ≤ V_{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ

Notes 1. When the pull-up resistors are not connected to P60 to P63 and P90 to P93 (specified by mask option), a low-level input leakage current of –200 μA (MAX.) flows only for 1.5 clocks (without wait) after a read instruction has been executed to port 6 (P6), port mode register 6 (PM6), port 9 (P9), or port mode register 9 (PM9).

At times other than this 1.5-clock interval, a –3 μA (MAX.) current flows.

2. A software pull-up resistor can be used only in the range of V_{DD} = 2.7 to 5.5 V.

Remark The characteristics of an alternate function pin are the same as those of port pins unless otherwise specified.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (3 of 3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current Note 1	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ±10% Note 5		4.5	13.5	mA
			V_{DD} = 3.0 V ±10% Note 6		0.7	2.1	mA
			V_{DD} = 2.0 V ±10% Note 6		0.4	1.2	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ±10% Note 5		8.0	24.0	mA
			V_{DD} = 3.0 V ±10% Note 6		0.9	2.7	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ±10%		1.4	4.2	mA
			V_{DD} = 3.0 V ±10%		0.5	1.5	mA
			V_{DD} = 2.0 V ±10%		280	840	μA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ±10%		1.6	4.8	mA
			V_{DD} = 3.0 V ±10%		0.65	1.95	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode Note 4	V_{DD} = 5.0 V ±10%		60	120	μA
			V_{DD} = 3.0 V ±10%		32	64	μA
			V_{DD} = 2.0 V ±10%		24	48	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode Note 4	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	15	μA
			V_{DD} = 2.0 V ±10%		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is used	V_{DD} = 5.0 V ±10%		1	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
			V_{DD} = 2.0 V ±10%		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA
			V_{DD} = 2.0 V ±10%		0.05	10	μA

Notes 1. Refers to the current flowing to the V_{DD} pin. The current flowing to the A/D converter, D/A converter, and ports is not included.

2. Operation with main system clock $f_{XX} = f_X/2$ (when oscillation mode select register (OSMS) is set to 00H)

3. Operation with main system clock $f_{XX} = f_X$ (when oscillation mode select register (OSMS) is set to 01H)

4. When the main system clock operation is halted

5. Operating in high-speed mode (when the processor clock control register (PCC) is set to 00H).

6. Operating in low-speed mode (when the processor clock control register (PCC) is set to 04H).

Remark The characteristics of an alternate function pin are the same as those of port pins unless otherwise specified.

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ Note 1	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
					2.0		64	μs
			$f_{XX} = f_X$ Note 2	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
				2.7 V ≤ V_{DD} < 3.5 V	0.8		32	μs
		Operating on subsystem clock			40 Note 3	122	125	μs
TI00 input high/ low-level width	t_{TIH00}, t_{TIL00}	3.5 V ≤ V_{DD} ≤ 5.5 V			$2/f_{sam}$ + 0.1 Note 4			μs
		2.7 V ≤ V_{DD} < 3.5 V			$2/f_{sam}$ + 0.2 Note 4			μs
					$2/f_{sam}$ + 0.5 Note 4			μs
TI01 input high/ low-level width	t_{TIH01}, t_{TIL01}	V_{DD} = 2.7 to 5.5 V			10			μs
					20			μs
TI1, TI2, TI5, TI6 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V			0		4	MHz
					0		275	kHz
TI1, TI2, TI5, TI6 input high/ low-level width	t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 to 5.5 V			100			ns
					1.8			μs
Interrupt request input high/low-level width	t_{INTH}, t_{INTL}	INTP0		3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$ + 0.1 Note 4			μs
				2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$ + 0.2 Note 4			μs
					$2/f_{sam}$ + 0.5 Note 4			μs
		INTP1 to INTP6, KR0 to KR7		V_{DD} = 2.7 to 5.5 V	10			μs
					20			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V			10			μs
					20			μs

Notes 1. When oscillation mode select register (OSMS) is set to 00H

2. When oscillation mode select register (OSMS) is set to 01H

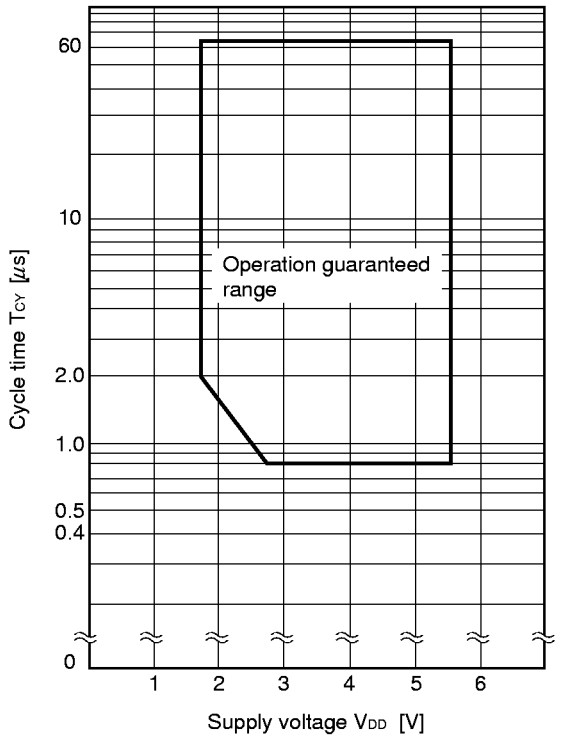
3. The value when using external clock. When using crystal resonator, it is 114 μs (MIN.).

4. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible from $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, and $f_{XX}/128$ (when N = 0 to 4).

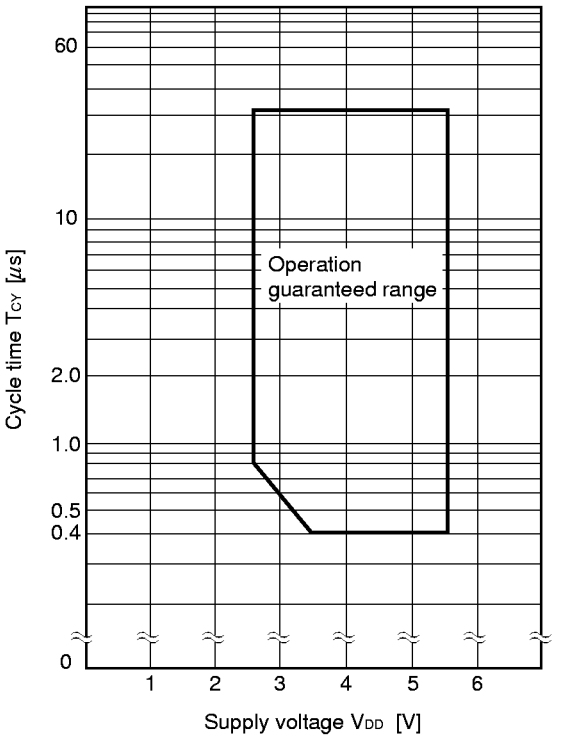
Remarks 1. f_{XX} : Main system clock frequency (f_X or $f_X/2$)

2. f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD} (At $f_{XX} = f_X/2$ main system clock operation)



T_{CY} vs V_{DD} (At $f_{XX} = f_X$ main system clock operation)



(2) Read/Write Operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to + 85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY} - 50$		ns
Address setup time	t_{ADS}		$0.85t_{CY} - 50$		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85 + 2n)t_{CY} - 80$	ns
	t_{ADD2}			$(4 + 2n)t_{CY} - 100$	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY} - 100$	ns
	t_{RDD2}			$(2.85 + 2n)t_{CY} - 100$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2 + 2n)t_{CY} - 60$		ns
	t_{RDL2}		$(2.85 + 2n)t_{CY} - 60$		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.85t_{CY} - 50$	ns
	t_{RDWT2}			$2t_{CY} - 60$	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{CY} - 60$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15 + 2n)t_{CY}$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85 + 2n)t_{CY} - 100$		ns
Write data hold time	t_{WDH}	Load resistance ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL}		$(2.85 + 2n)t_{CY} - 60$		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY} + 20$		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ at external fetch	t_{RDAST}		$0.85t_{CY} - 10$	$1.15t_{CY} + 20$	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t_{RDADH}		$0.85t_{CY} - 50$	$1.15t_{CY} + 50$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY} - 20$	$1.15t_{CY} + 40$	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$1.15t_{CY} + 40$	$3.15t_{CY} + 40$	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$1.15t_{CY} + 30$	$3.15t_{CY} + 30$	ns

Remarks 1. MCS: Bit 0 of the oscillation mode select register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to + 85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 80		ns
Address setup time	t_{ADS}		t_{CY} – 80		ns
Address hold time	t_{ADH}		0.4t_{CY} – 10		ns
Data input time from address	t_{ADD1}			(3 + 2n)t_{CY} – 160	ns
	t_{ADD2}			(4 + 2n)t_{CY} – 200	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(1.4 + 2n)t_{CY} – 70	ns
	t_{RDD2}			(2.4 + 2n)t_{CY} – 70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4 + 2n)t_{CY} – 20		ns
	t_{RDL2}		(2.4 + 2n)t_{CY} – 20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			t_{CY} – 100	ns
	t_{RDWT2}			2t_{CY} – 100	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			2t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		(2.4 + 2n)t_{CY}–60		ns
Write data hold time	t_{WDH}	Load resistance ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.4 + 2n)t_{CY} – 20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		0.4t_{CY} – 30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		1.4t_{CY} – 30		ns
ASTB↑ delay time from $\overline{RD}$↑ at external fetch	t_{RDAST}		t_{CY} –10	t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ at external fetch	t_{RDADH}		t_{CY} – 80	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		0.4t_{CY} – 30		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		0	60	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		t_{CY} – 60	t_{CY} + 60	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY} + 120	ns

Remarks 1. MCS: Bit 0 of the oscillation mode select register (OSMS)

2. PCC2 to PCC0: Bits 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF **Note**			300	ns

Note C is the load capacitance of SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}			400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF **Note**	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK0}$ rise/fall time	t_{R2}, t_{F2}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the load capacitance of the SO0 output line.

(iii) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
			2.0 V ≤ V_{DD} < 2.7 V	3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH3}		V_{DD} = 2.7 to 5.5 V	$t_{KCY3}/2 - 160$			ns
				$t_{KCY3}/2 - 190$			ns
$\overline{SCK0}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 5.5 V	$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}			0		300	ns

Note R and C are the load resistance and load capacitance of the SCK0, SB0, and SB1 output lines, respectively.

(iv) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH4}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{SCK0}$ low-level width	t_{KL4}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
						800	ns
$\overline{SCK0}$ rise/fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines, respectively.

(v) I²C bus mode (SCL... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	2.7 V ≤ V_{DD} ≤ 5.5 V	10			μs
			2.0 V ≤ V_{DD} < 2.7 V	20			μs
				30			μs
SCL high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	t_{KCY5} – 160			ns
				t_{KCY5} – 190			ns
SCL low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	t_{KCY5} – 50			ns
				t_{KCY5} – 100			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK5}		2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} < 2.7 V	300			ns
				400			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI5}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO5}		4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL ↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}		V_{DD} = 2.0 to 5.5 V	400			ns
				500			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0, and SDA1 output lines, respectively.

(vi) I²C bus mode (SCL... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY6}			1000			ns
SCL high/low-level width	t_{KH6}, t_{KL6}	V_{DD} = 2.0 to 5.5 V		400			ns
				600			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK6}	V_{DD} = 2.0 to 5.5 V		200			ns
				300			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI6}			0			ns
SDA0, SDA1 output delay time from SCL↓	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL ↑	t_{KSB}			200			ns
SCL↓ from SDA0, SDA1↓	t_{SBK}	V_{DD} = 2.0 to 5.5 V		400			ns
				500			ns
SDA0, SDA1 high-level width	t_{SBH}	V_{DD} = 2.0 to 5.5 V		500			ns
				800			
SCL rise/fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines, respectively.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 5.5 V	$t_{KCY7}/2 - 50$			ns
			$t_{KCY7}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF [Note]			300	ns

Note C is the load capacitance of the SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}			400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF [Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise/fall time	t_{R8}, t_{F8}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	$t_{KCY9}/2 - 50$			ns
			$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO9}	C = 100 pF **Note**			300	ns
STB↑ from $\overline{SCK1}$↑	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} ≤ 5.5 V	$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
		2.0 V ≤ V_{DD} < 2.7 V	$t_{KCY9} - 60$		$t_{KCY9} + 60$	ns
			$t_{KCY9} - 90$		$t_{KCY9} + 90$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
$\overline{SCK1}$↓ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note C is the load capacitance of the SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1600			ns
			2400			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO10}	C = 100 pF Note, V_{DD} = 2.0 to 5.5 V			300	ns
					500	ns
$\overline{SCK1}$ rise/fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the load capacitance of the SO1 output line.

(c) Serial Interface Channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 5.5 V	$t_{KCY11}/2 - 50$			ns
			$t_{KCY11}/2 - 100$			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100 pF Note			300	ns

Note C is the load capacitance of SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK2}$ high/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK12}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI12}			400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO12}	C = 100 pF Note	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK2}$ rise/fall time	t_{R12}, t_{F12}	V_{DD} = 4.5 to 5.5 V When not using external device expansion function				1000	ns
						160	ns

Note C is the load capacitance of the SO2 output line.

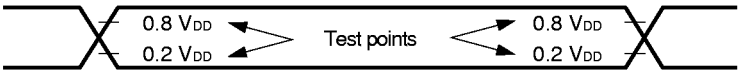
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
		2.0 V ≤ V_{DD} < 2.7 V			19531	bps
					9766	bps

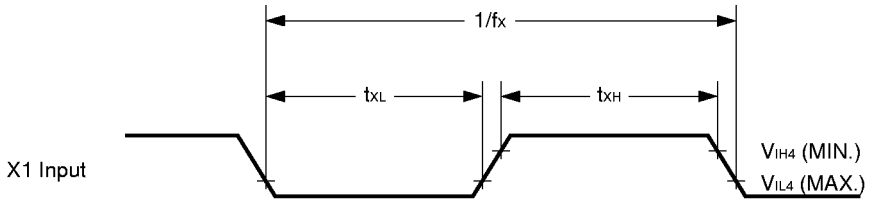
(iv) UART mode (External clock input)

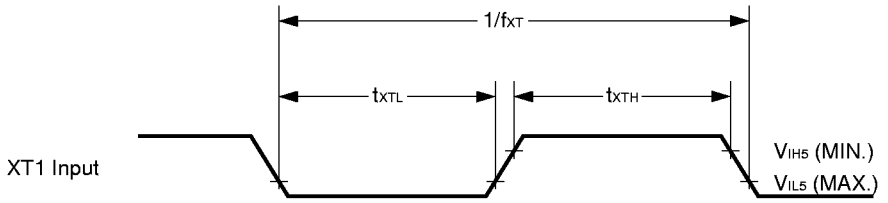
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
ASCK high/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1600			ns
			2400			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
		2.0 V ≤ V_{DD} < 2.7 V			9766	bps
					6510	bps
ASCK rise/fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 5.5 V When not using external device expansion function			1000	ns
					160	ns

AC Timing Test Points (excluding X1, XT1 Inputs)

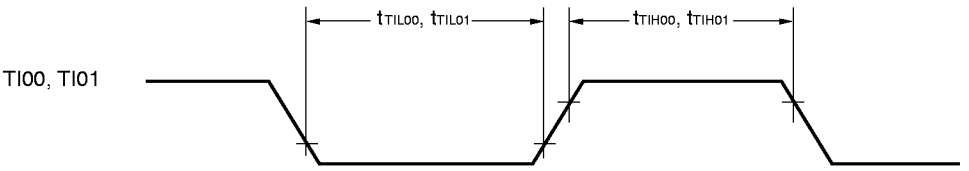


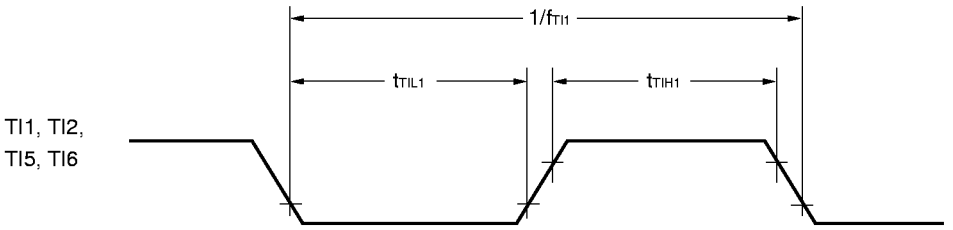
Clock Timing





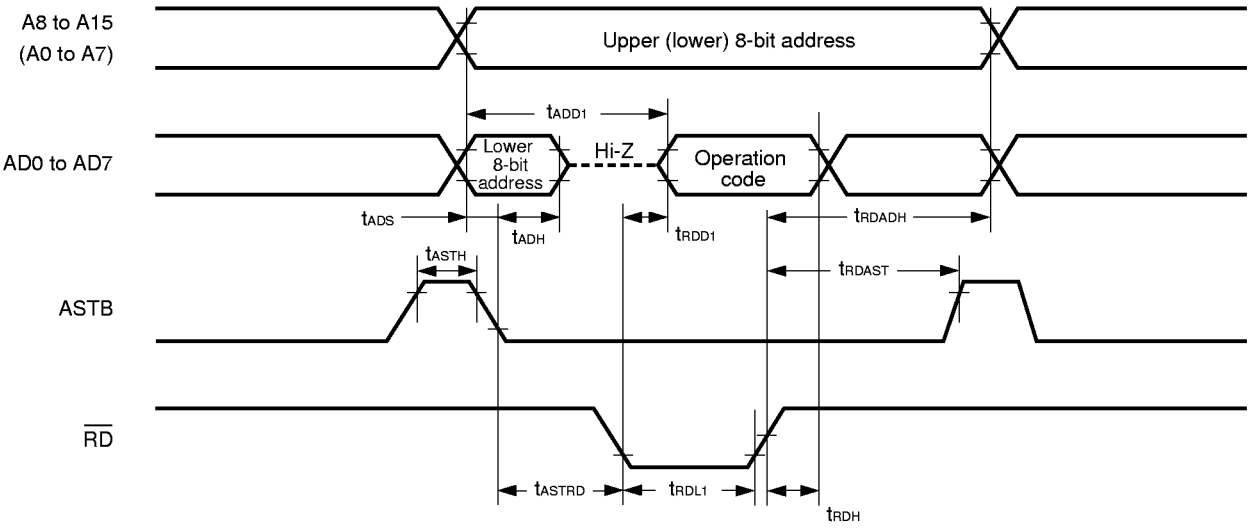
TI Timing





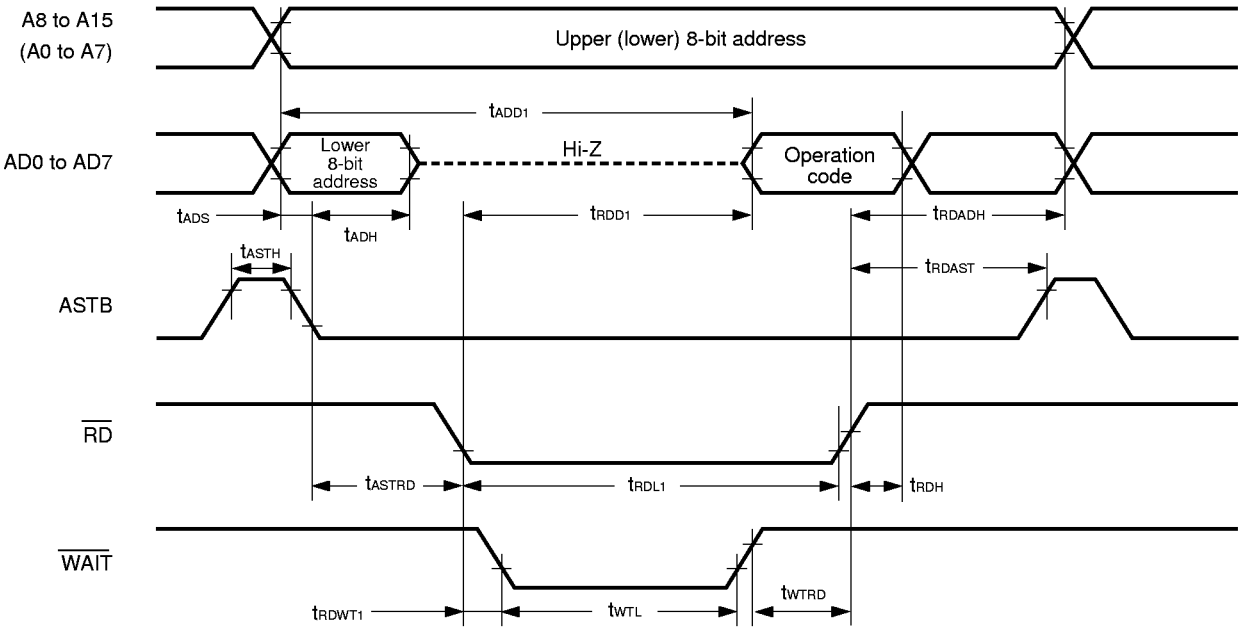
Read/Write Operation

External fetch (no wait) :



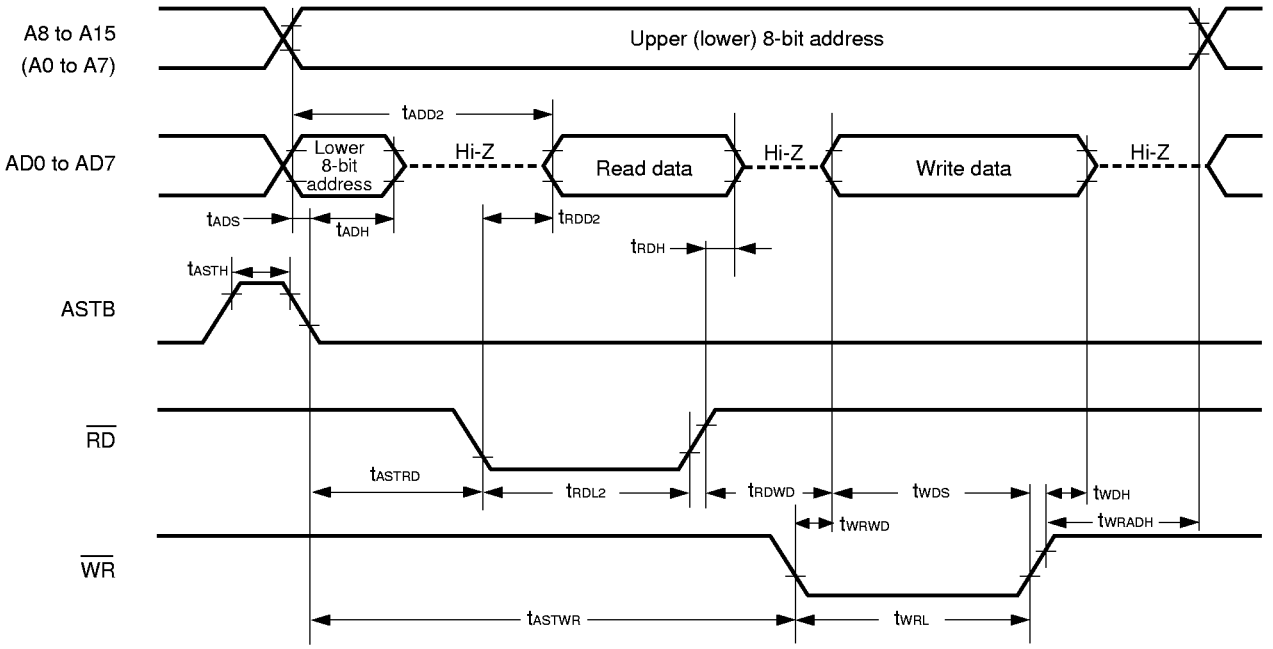
Remark ( ) is valid only in the separate bus mode.

External fetch (wait insertion) :



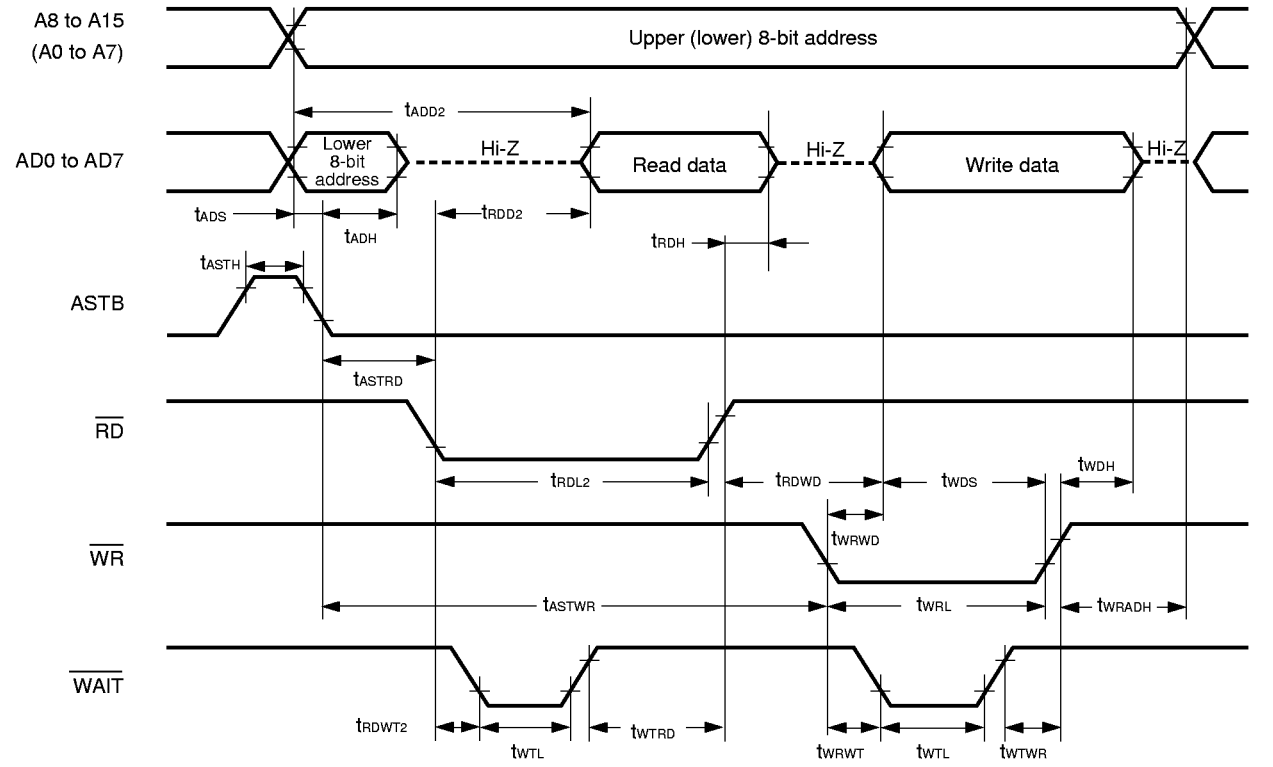
Remark ( ) is valid only in the separate bus mode.

External data access (no wait) :



Remark ( ) is valid only in the separate bus mode.

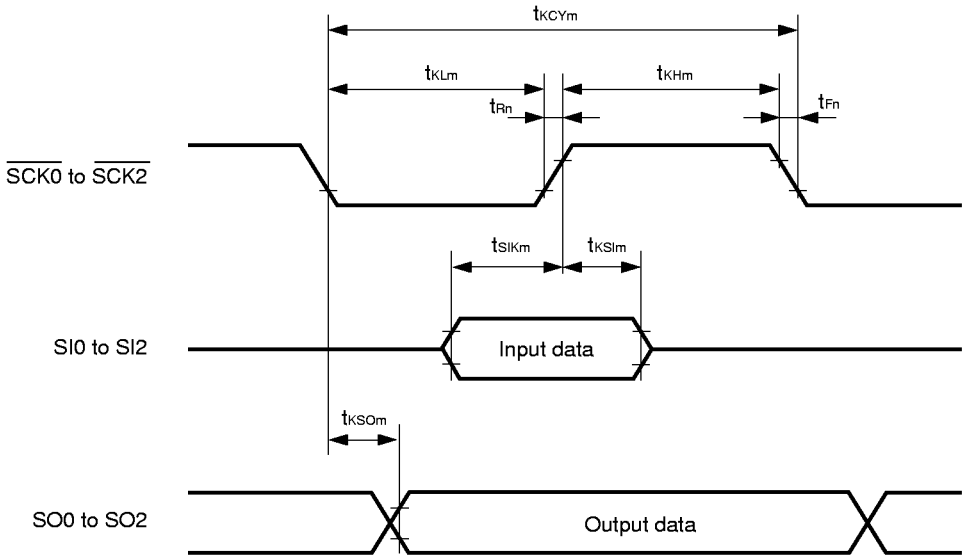
External data access (wait insertion) :



Remark ( ) is valid only in the separate bus mode.

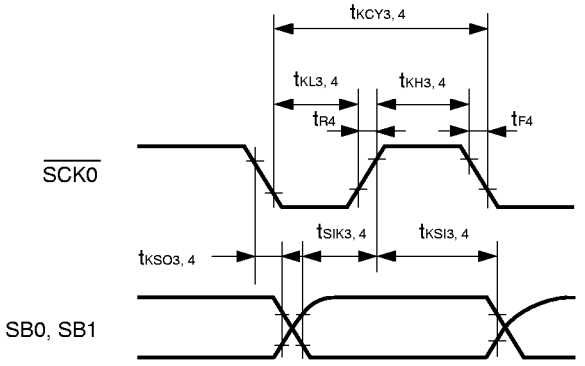
Serial Transfer Timing

3-wire serial I/O mode :

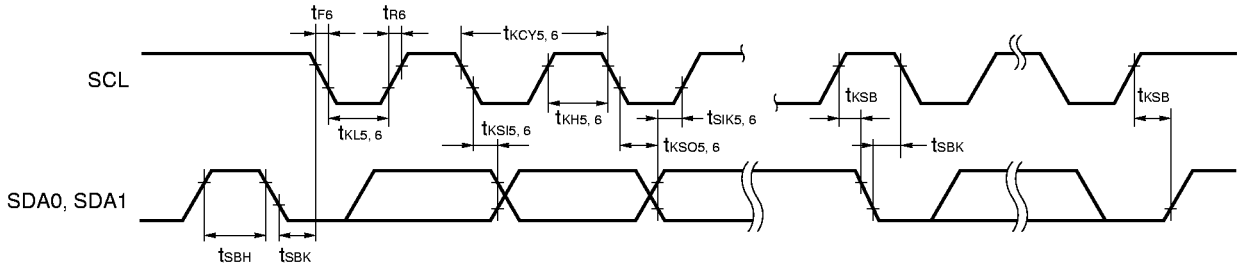


m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

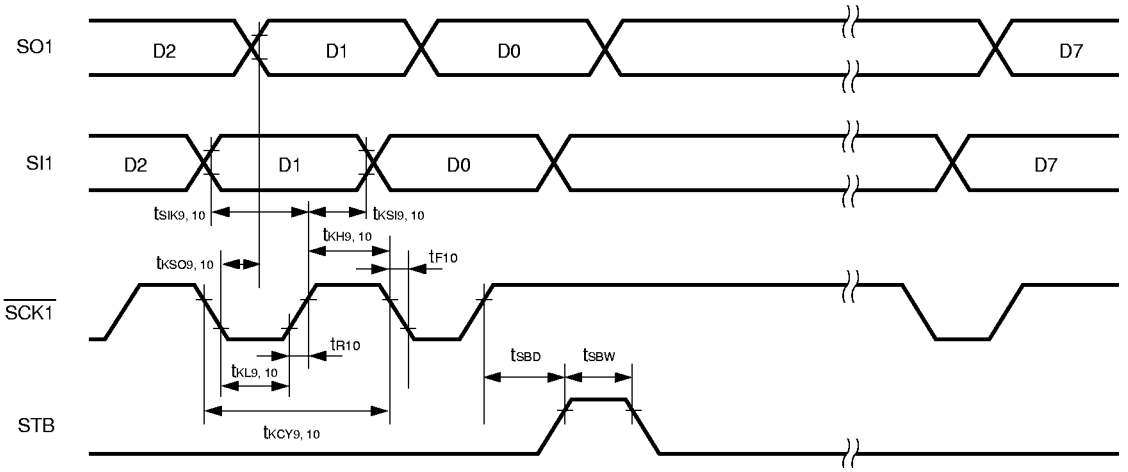
2-wire serial I/O mode :



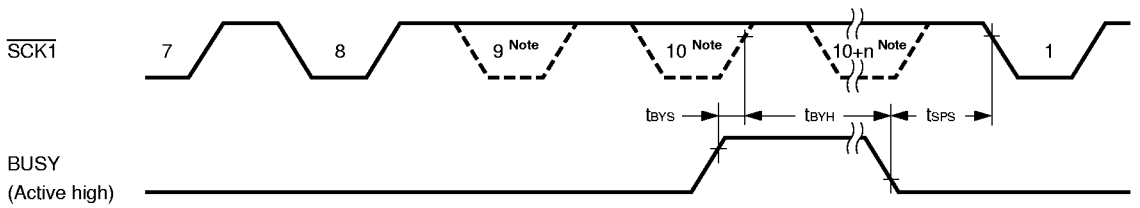
I²C bus mode :



3-wire serial I/O mode with automatic transmit/receive function :

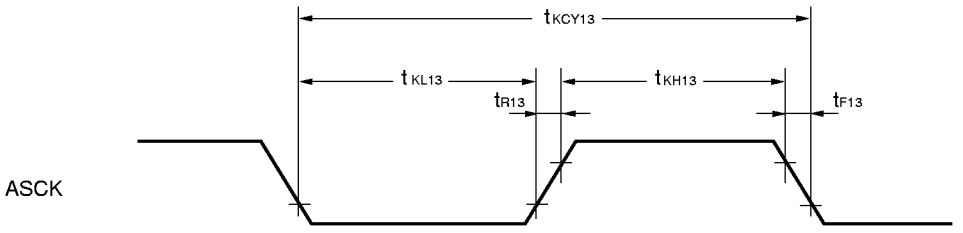


3-wire serial I/O mode with automatic transmit/receive function (busy processing) :



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART mode (external clock input) :



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error Note		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			0.6	%
		1.8 V ≤ AV_{REF0} < 2.7 V			1.4	%
Conversion time	t_{CONV}	2.0 V ≤ AV_{DD} ≤ 5.5 V	19.1		200	μs
		1.8 V ≤ AV_{DD} < 2.0 V	38.2		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		1.8		AV_{DD}	V
Resistance between AV_{REF0} and AV_{SS}	R_{AIREF0}		4	14		kΩ

Note Excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Remarks 1. f_{XX}: Main system clock frequency (f_X or f_X/2)

2. f_X: Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error		R = 2 MΩ Note 1				1.2	%
		R = 4 MΩ Note 1				0.8	%
		R = 10 MΩ Note 1				0.6	%
Settling time		Note C=30pF	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			1.8 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_O	**Note 2**			10		kΩ
Analog reference voltage	AV_{REF1}			1.8		V_{DD}	V
Resistance between AV_{REF1} and AV_{SS}	R_{AIREF1}	DACS0, DACS1 = 55H Note 2		4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance, respectively.

2. Value for one D/A converter channel

Remark DACS0, DACS1: D/A Conversion value setting registers 0, 1.

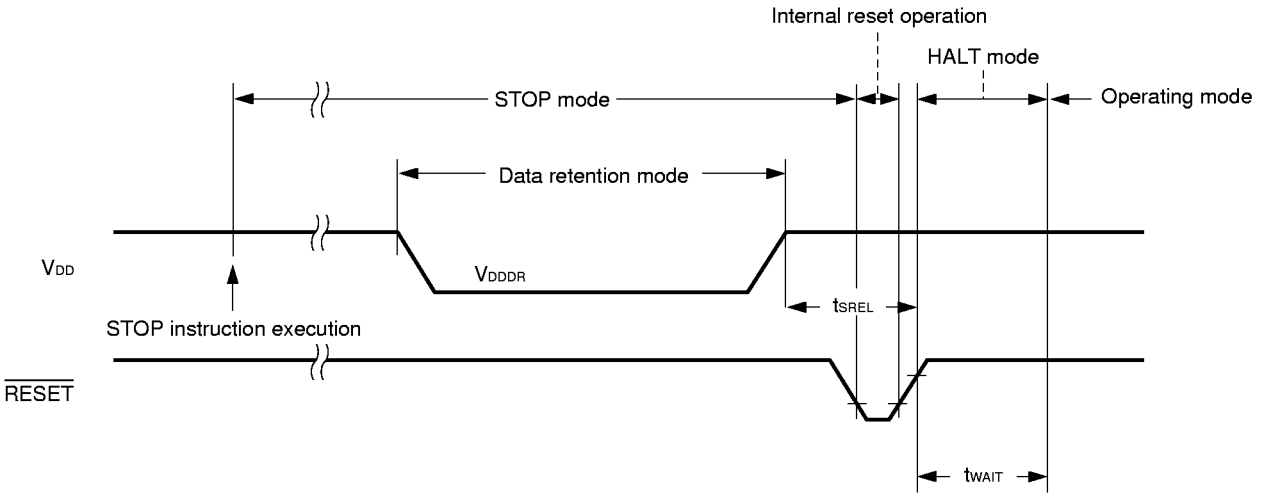
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stop and feedback resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		**Note**		ms

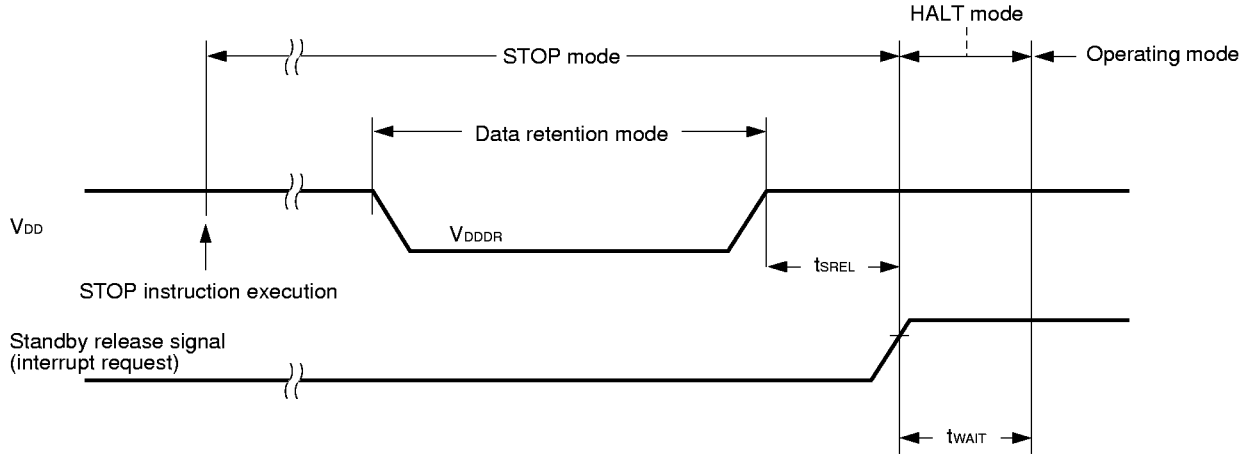
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection is possible from 2^{12}/fxx and 2^{14}/fxx to 2^{17}/fxx.

Remark fxx: Main system clock frequency (fx or fx/2)
fx: Main system clock oscillation frequency

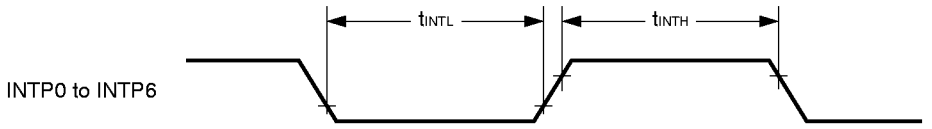
Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)



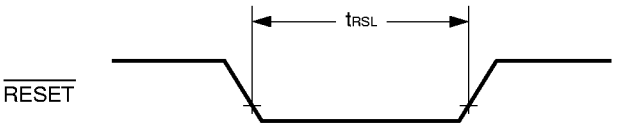
Data Retention Timing (Standby release signal: STOP mode release by interrupt request signal)



Interrupt Request Input Timing

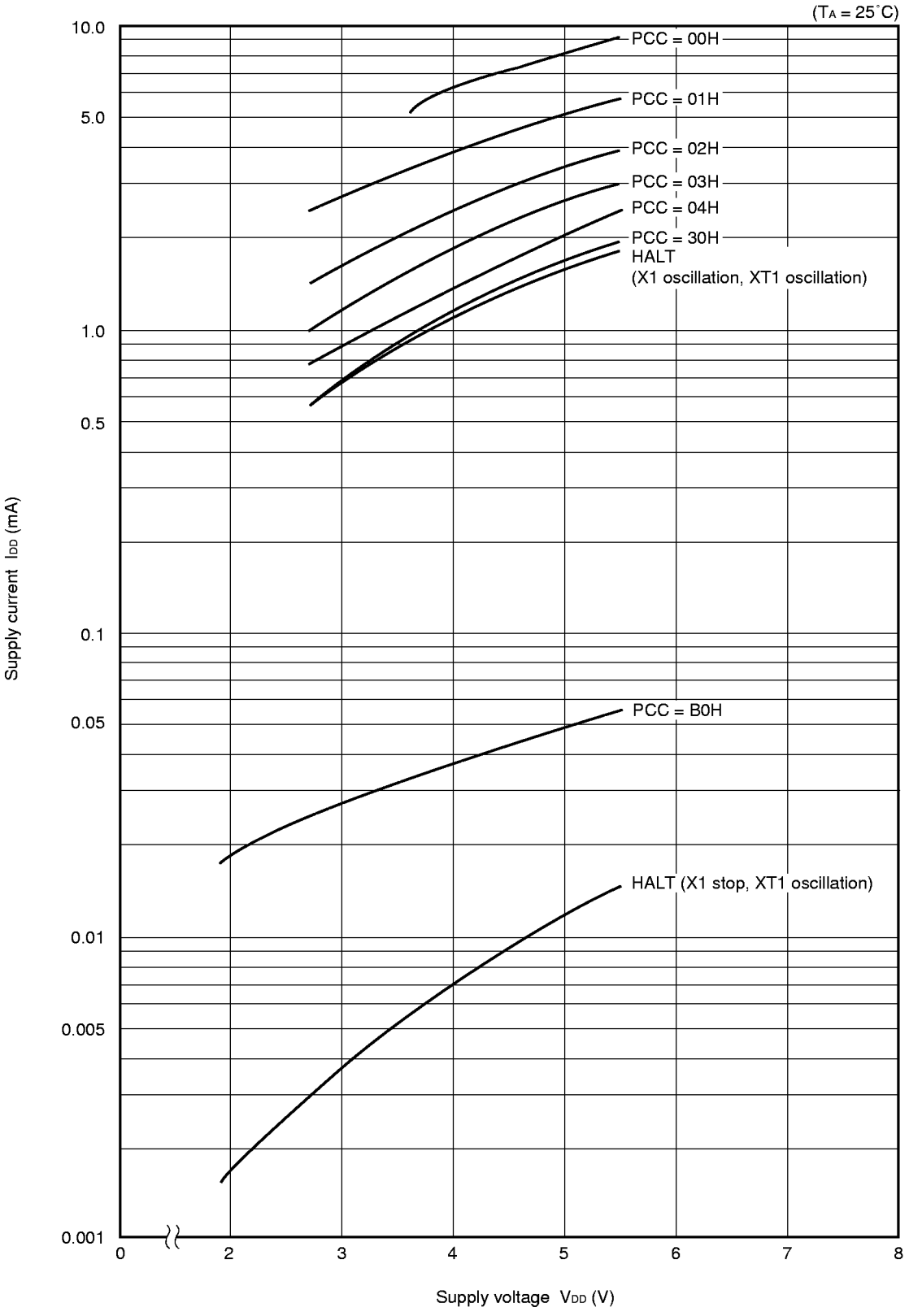


$\overline{\text{RESET}}$ Input Timing

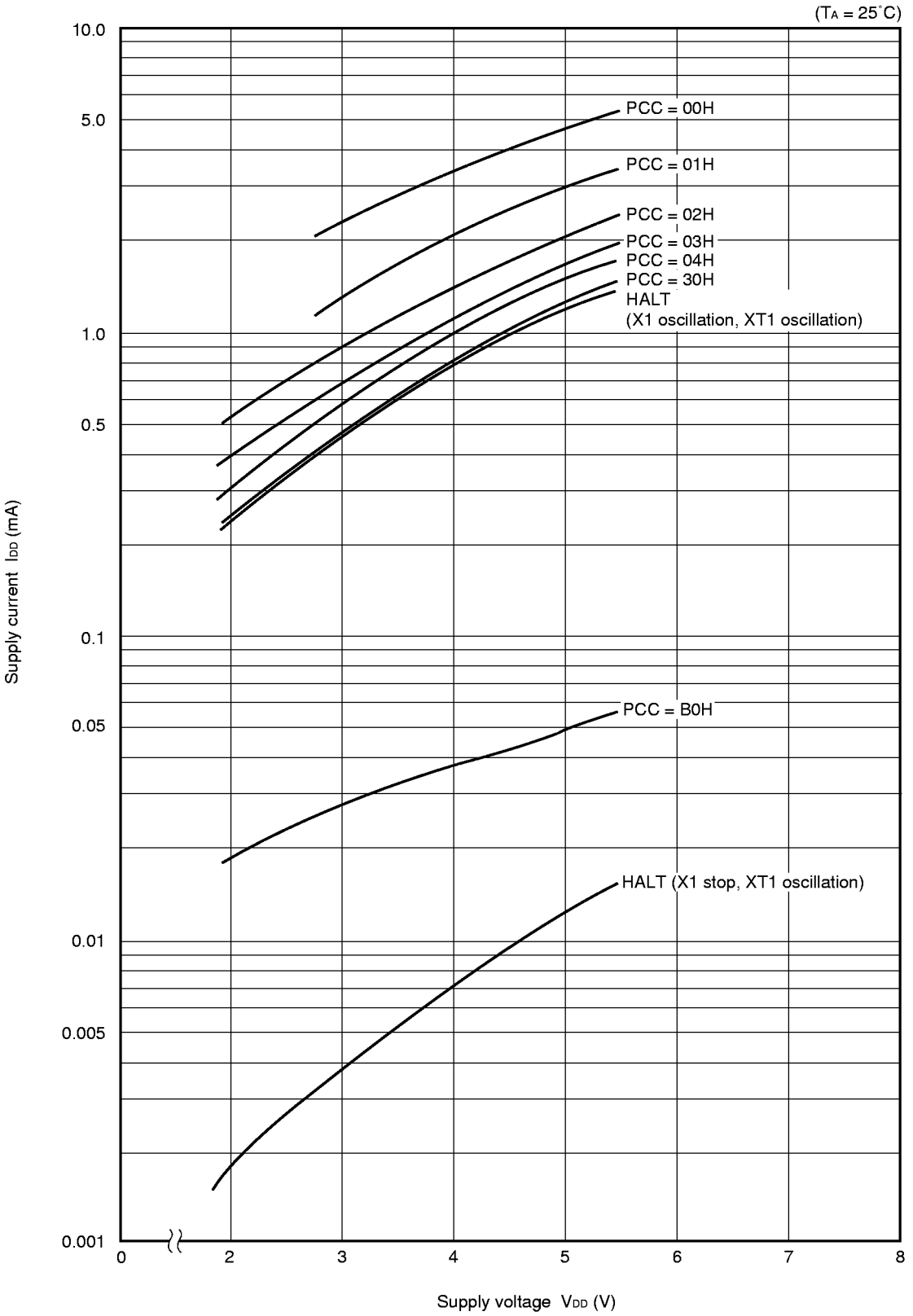


12. CHARACTERISTIC CURVES (REFERENCE VALUE)

I_{DD} vs V_{DD} (fx = fxx = 5.0 MHz)

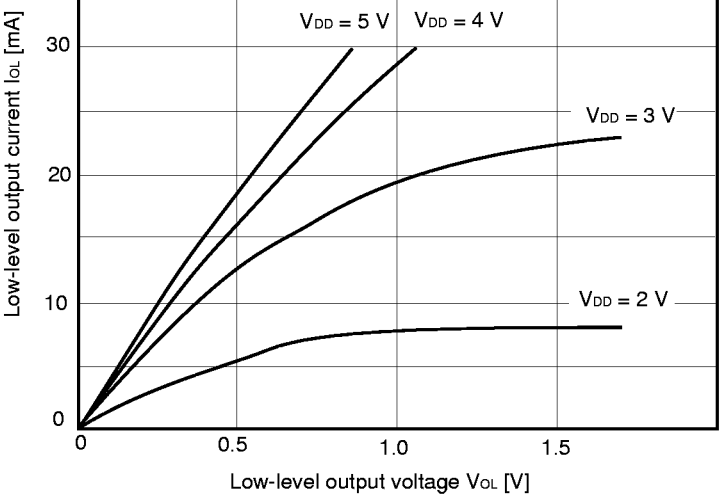


I_{DD} vs V_{DD} (fx = 5.0 MHz, fxx = 2.5 MHz)



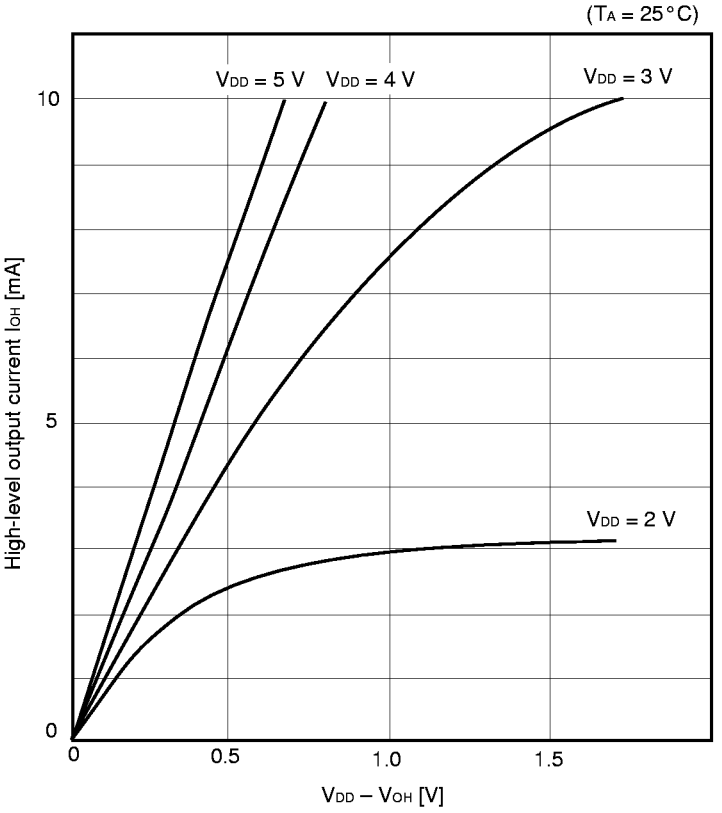
I_{OL} vs V_{OL} (Port 0)

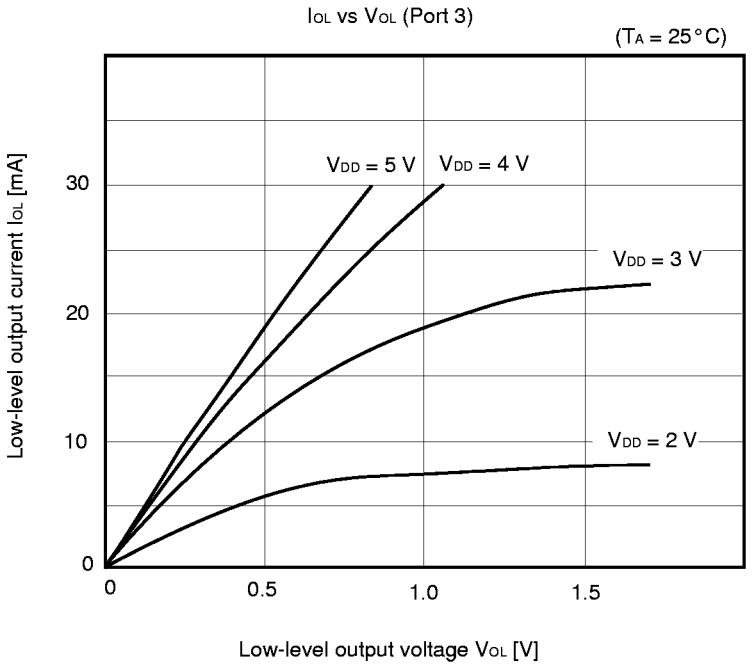
(T_A = 25°C)

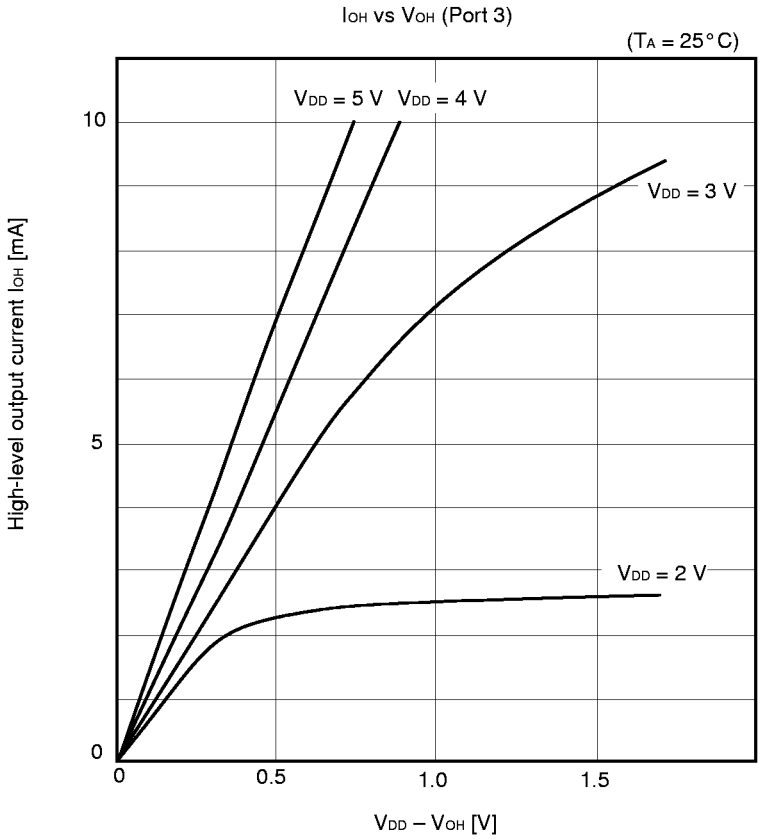


I_{OH} vs V_{OH} (Port 0)

(T_A = 25°C)

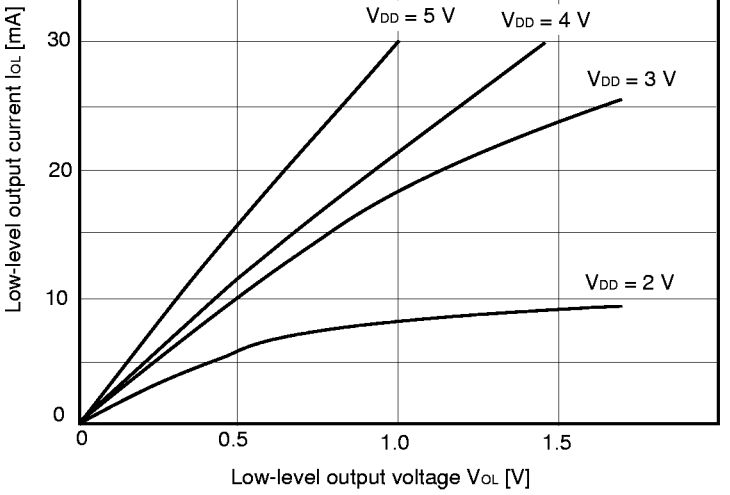



IOL vs VOL (Port 3)
(TA = 25°C)
VDD = 5 V
VDD = 4 V
VDD = 3 V
VDD = 2 V
Low-level output current IOL [mA]
30
20
10
0
0
0.5
1.0
1.5
Low-level output voltage VOL [V]


IOH vs VOH (Port 3)
(TA = 25°C)
VDD = 5 V
VDD = 4 V
VDD = 3 V
VDD = 2 V
High-level output current IOH [mA]
10
5
0
0
0.5
1.0
1.5
VDD – VOH [V]

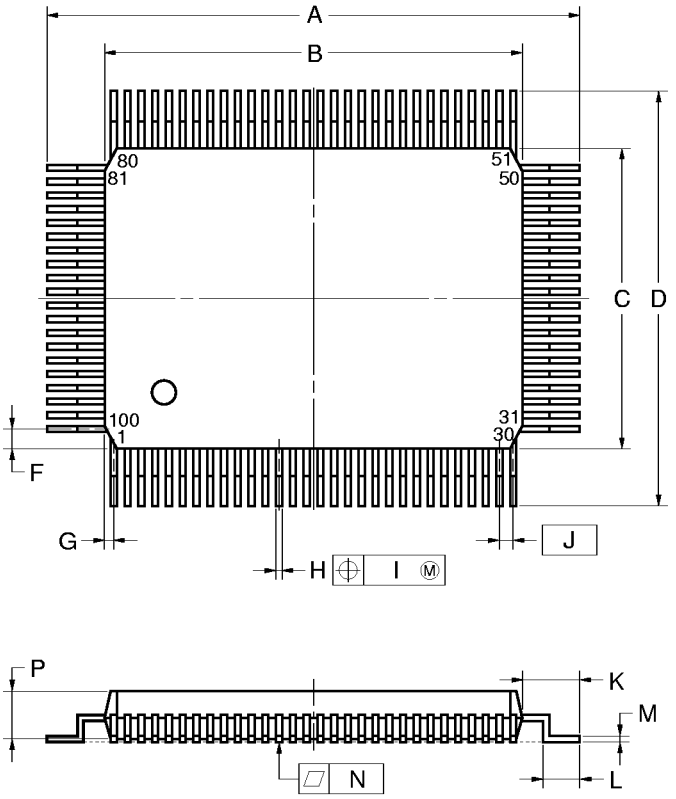
I_{OL} vs V_{OL} (Port 6)

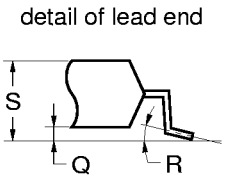
(T_A = 25°C)



13. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14x20)





NOTE

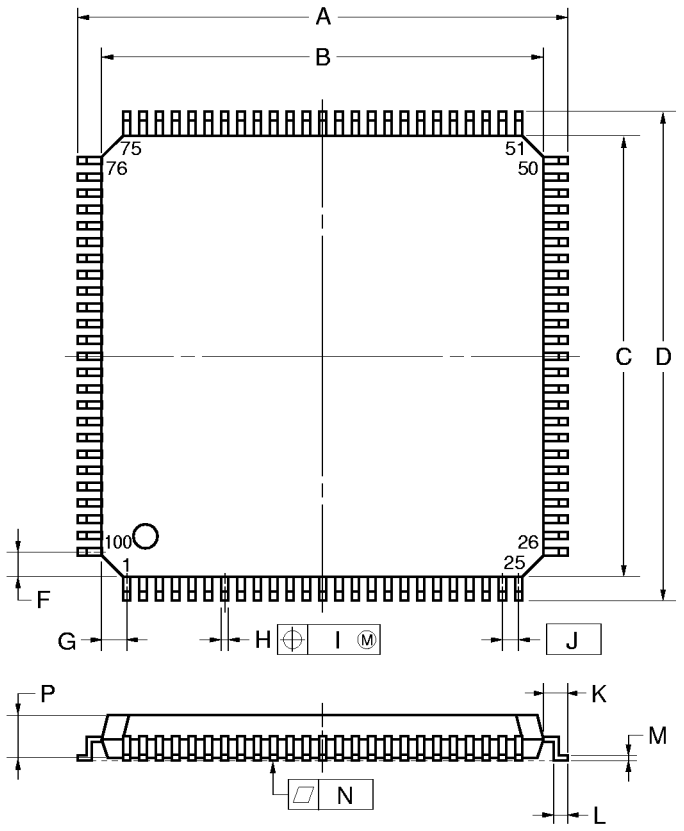
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

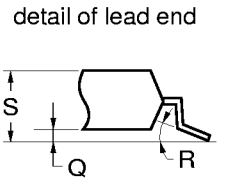
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

Remark The external dimensions and material of the ES version are the same as that of the mass-produced version.

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)





NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

Remark The external dimensions and material of the ES version are the same as that of the mass-produced version.

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78076Y and 78078Y should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, consult an NEC sales personnel.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD78076YGF-×××-3BA : 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)
μPD78078YGF-×××-3BA : 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: three or less.	IR35-00-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: three or less.	VP15-00-3
Wave soldering	Soldering bath temperature: 260°C max., Duration: 10 sec. max., Number of times: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per pin row)	—

Cautions 1. Use of more than one soldering method should be avoided (except in the case of partial heating).

2. The soldering conditions for the μPD78076YGC-xxx-8EU and μPD78078YGC-xxx-8EU are undefined, since they are still under development.

★ APPENDIX A. DEVELOPMENT TOOLS

The following tools are available for system development using the μPD78076Y and 78078Y.
Also refer to **(5) Cautions when Using Development Tools**.

(1) Language Processing Software

RA78K/0	Assembler package common to the 78K/0 Series
CC78K/0	C compiler package common to the 78K/0 Series
DF78078	Device file common to the μPD78078 Subseries
CC78K/0–L	C compiler library source file common to the 78K/0 Series

(2) PROM Writing Tools

PG-1500	PROM programmer
PA-78P078GF PA-78P078GC PA-78P078KL-T	Programmer adapters connected to the PG-1500
PG-1500 controller	PG-1500 control program

(3) Debugging Tools

- **In-circuit emulator (when IE-78K0-NS is used)**

IE-78K0-NS[Note]	In-circuit emulator common to the 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for the IE-78K0-NS
IE-70000-98-IF-C[Note]	Interface adapter when using the PC-9800 series (except for notebook computers) as the host machine
IE-70000-CD-IF[Note]	PC card and interface cable when using the PC-9800 series notebook computers as the host machine
IE-70000-PC-IF-C[Note]	Interface adapter when using IBM PC/AT™ and its compatibles as the host machine
IE-78078-NS-EM1[Note]	Emulation board to common to the μPD78078 Subseries
NP-100GC	Emulation probe for 100-pin plastic QFP (GC-8EU type)
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC and the target system board on which 100-pin plastic QFP (GC-8EU type) can be mounted
EV-9200GF-100	Socket mounted on the target system board for 100-pin plastic QFP (GF-3BA type)
ID78K0-NS[Note]	Integrated debugger for the IE-78K0-NS
SM78K0	System simulator common to the 78K/0 Series
DF78078	Device file common to the μPD78078 Subseries

Note Under development

- **In-circuit Emulator (when IE-78001-R-A is used)**

IE-78001-R-A[Note]	In-circuit emulator common to the 78K/0 Series
IE-70000-98-IF-B IE-70000-98-IF-C[Note]	Interface adapter when using the PC-9800 series (except for notebook computers) as the host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C[Note]	Interface adapter and cable when using IBM PC/AT and its compatibles as the host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as the host machine
IE-78078-NS-EM1[Note] IE-78078-R-EM	Emulation board common to the μPD78078 Subseries
IE-78K0-R-EX1[Note]	Emulation probe conversion board that is necessary when using the IE-78078-NS-EM1 on the IE-78001-R-A
EP-78064GC-R	Emulation probe for 100-pin plastic QFP (GC-8EU type)
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the EP-78064GC-R and the target system board on which 100-pin plastic QFP (GC-8EU type) can be mounted
EV-9200GF-100	Socket mounted on the target system board for 100-pin plastic QFP (GF-3BA type)
ID78K0	Integrated debugger for the IE-78001-R-A
SM78K0	System simulator common to the 78K/0 Series
DF78078	Device file common to the μPD78078 Subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for the 78K/0 Series
MX78K0	OS for the 78K/0 Series

(5) Cautions when Using Development Tools

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF78078.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 or DF78078.
- The NP-100GC and NP-100GF are products of Naito Densei Machidaseisakusho Co., Ltd. (044-822-3813). Contact an NEC distributor about purchasing.
- The TGC-100SDW is a product of TOKYO ELETECH CORPORATION.
  Refer to: Daimaru Kogyo, Ltd. Tokyo Electronic Components Division (03-3820-7112)
  Osaka Electronic Components Division (06-244-6672)
- Refer to **78K/0 Series Selection Guide (U11126E)** about third-party development tools.
- The host machine and the OS applied to each software are shown below.

Software \ Host Machine [OS]	PC PC-9800 series [Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√Note	√
CC78K/0	√Note	√
PG-1500 controller	√Note	–
ID78K0-NS	√	–
ID78K0	√	√
SM78K0	√	–
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	English	Japanese
μPD78078, 78078Y Subseries User's Manual	U10641E	U10641J
μPD78076Y, 78078Y Data Sheet	This document	U10605J
μPD78P078Y Data Sheet	U10606E	U10606J
78K/0 Series User's Manual—Instructions	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J
μPD78078Y Subseries Special Function Register Table	—	IEM-5601
78K/0 Series Application Note—Basic (III)	U10182E	U10182J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version for designing, etc.

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.	
		English	Japanese
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC78K/0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	U12322J
PG-1500 PROM Programmer		EEU-1335	U11940J
PG-1500 Controller PC-9800 Series (MS-DOS™) Based		EEU-1291	EEU-704
PG-1500 Controller IBM PC Series (PC DOS™) Based		U10540E	EEU-5008
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-78K0-R-EX1		To be prepared	To be prepared
IE-78078-NS-EM1		To be prepared	To be prepared
IE-78078-R-EM		U10775E	U10775J
EP-78064		EEU-1469	EEU-934
SM78K0 System Simulator Windows Based	Reference	U10181E	U10181J
SM78K Series System Simulator	External part user open interface specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger	Reference	To be prepared	U12900J
ID78K0 Integrated Debugger EWS Based	Reference	—	U11151J
ID78K0 Integrated Debugger Windows Based	Guide	U11649E	U11649J
ID78K0 Integrated Debugger PC Based	Reference	U11539E	U11539J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version for designing, etc.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Other Documents

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer Product Series Guide	—	U11416J

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version for designing, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.1.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

NEC do Brasil S.A.
Cumbica-Guarulhos-SP, Brasil
Tel: 011-6465-6810
Fax: 011-6465-6829

J97. 8