
HB56A432 Series

4,194,304-word $\times$ 32-bit High Density Dynamic RAM Module

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ADE-203-
Rev. 0.0
Dec. 1, 1995

Description

The HB56A432 is a 4 M $\times$ 32 dynamic RAM module, mounted 8 pieces of 16-Mbit DRAM (HM5117400BS) sealed in SOJ package. An outline of the HB56A432 is 72-pin single in-line package. Therefore, the HB56A432 makes high density mounting possible without surface mount technology. The HB56A432 provides common data inputs and outputs.

Decoupling capacitors are mounted beneath each SOJ.

Features

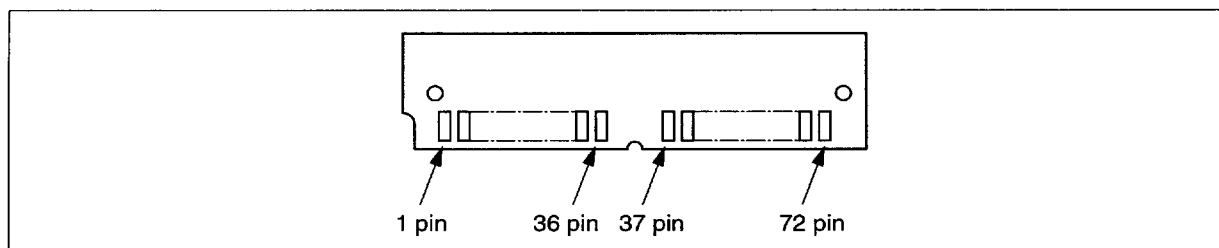
- 72-pin single in-line package
 - Lead pitch : 1.27 mm
- Single 5 V ($\pm 5\%$) supply
- High speed
 - Access time : 60 ns/70 ns/80 ns (max)
- Low power dissipation
 - Active mode : 4.62 W/4.20 W/3.78 W (max)
 - Standby mode : 84 mW (max)
- Fast page mode capability
- 2,048 refresh cycle: 32 ms
- 2 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- TTL compatible

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Ordering Information

Type No.	Access Time	Package	Contact Pad
HB56A432BR-6B	60ns	72-pin SIP socket type	gold
HB56A432BR-7B	70 ns		
HB56A432BR-8B	80 ns		
HB56A432SBR-6B	60ns	72-pin SIP socket type	solder
HB56A432SBR-7B	70 ns		
HB56A432SBR-8B	80 ns		

Pin Arrangement



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Pin Arrangement (cont)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V _{SS}	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V _{SS}	57	DQ12
4	DQ1	22	DQ5	40	$\overline{\text{CAS0}}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{\text{CAS2}}$	59	V _{CC}
6	DQ2	24	DQ6	42	$\overline{\text{CAS3}}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{\text{CAS1}}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{\text{RAS0}}$	62	DQ30
9	DQ19	27	DQ23	45	NC	63	DQ14
10	V _{CC}	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	$\overline{\text{WE}}$	65	DQ15
12	A0	30	V _{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	NC	51	DQ9	69	PD3
16	A4	34	$\overline{\text{RAS2}}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V _{SS}

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Pin Description

Pin Name	Function
A0–A10	Address input
A0–A10	Refresh address input
DQ0–DQ31	Data-in/data-out
$\overline{\text{CAS0}}\text{--}\overline{\text{CAS3}}$	Column address strobe
$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row address strobe
$\overline{\text{WE}}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1–PD4	Presence detect pin
NC	No connection

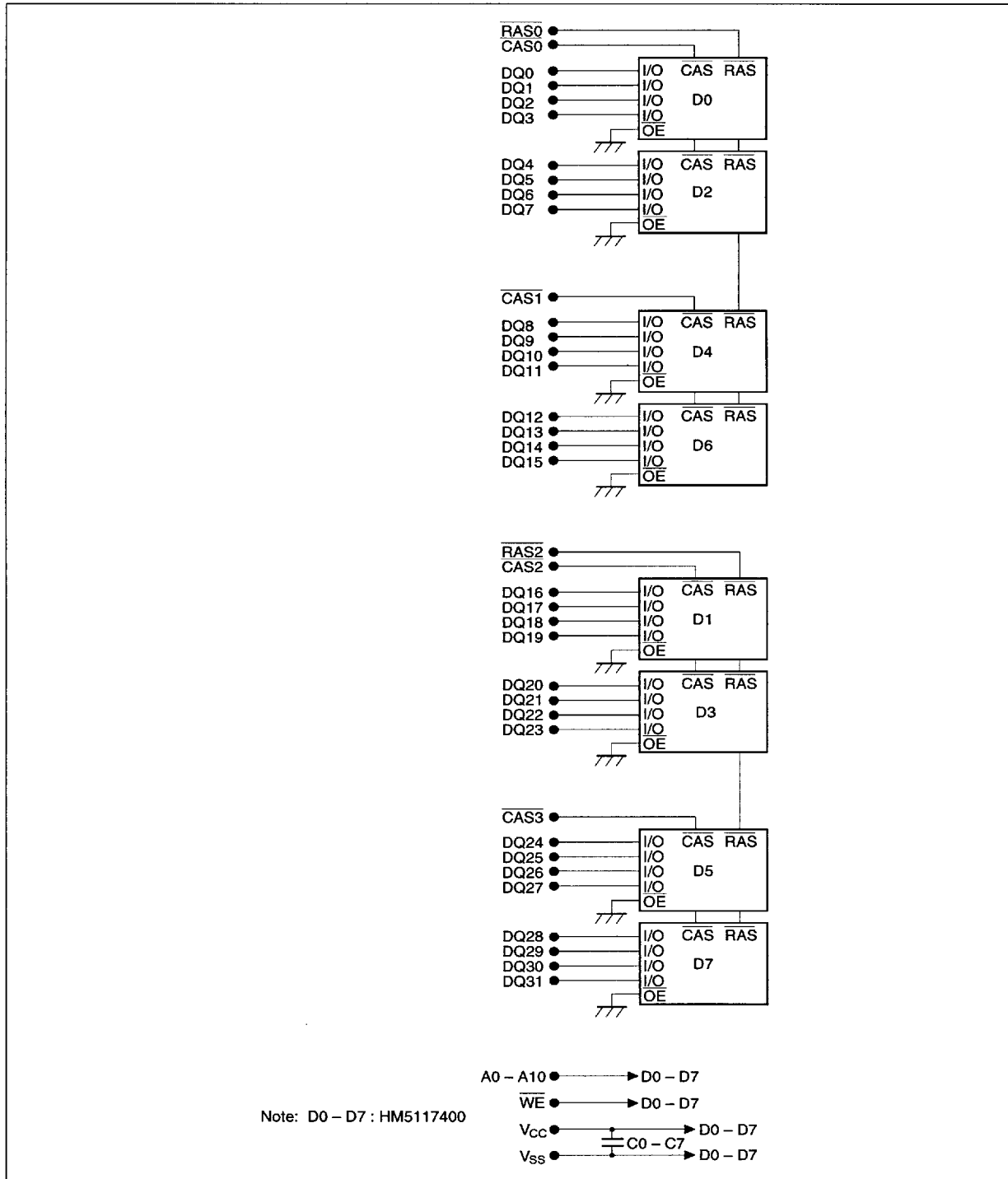
Presence Detect Pin Arrangement

Pin No.	Pin Name	HB56A432		
		60 ns	70 ns	80 ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	NC	NC	NC
69	PD3	NC	V_{SS}	NC
70	PD4	NC	NC	V_{SS}

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Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	8	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	-1.0	—	0.8	V	1

Note: 1. All voltage referred to V_{SS}

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DC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$)

		HB56A432BR/SBR								
		60 ns		70 ns		80 ns				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions	Notes
Operating current	I _{CC1}	—	880	—	800	—	720	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	16	—	16	—	16	mA	TTL interface, RAS, CAS = V _{IH} , Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface, RAS, CAS ≥ V _{CC} – 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	880	—	800	—	720	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	40	—	40	—	40	mA	RAS = V _{IH} , CAS = V _{IL} , Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	880	—	800	—	720	mA	t _{RC} = min	
Page mode current	I _{CC7}	—	640	—	560	—	520	mA	t _{PC} = min	1, 3
Input leakage current	I _{LI}	–10	10	–10	10	–10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I _{LO}	–10	10	–10	10	–10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = –5 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

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Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	68	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	76	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	43	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	29	pF	1
I/O capacitance (DQ0 – DQ31)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable Dout.

AC Characteristics

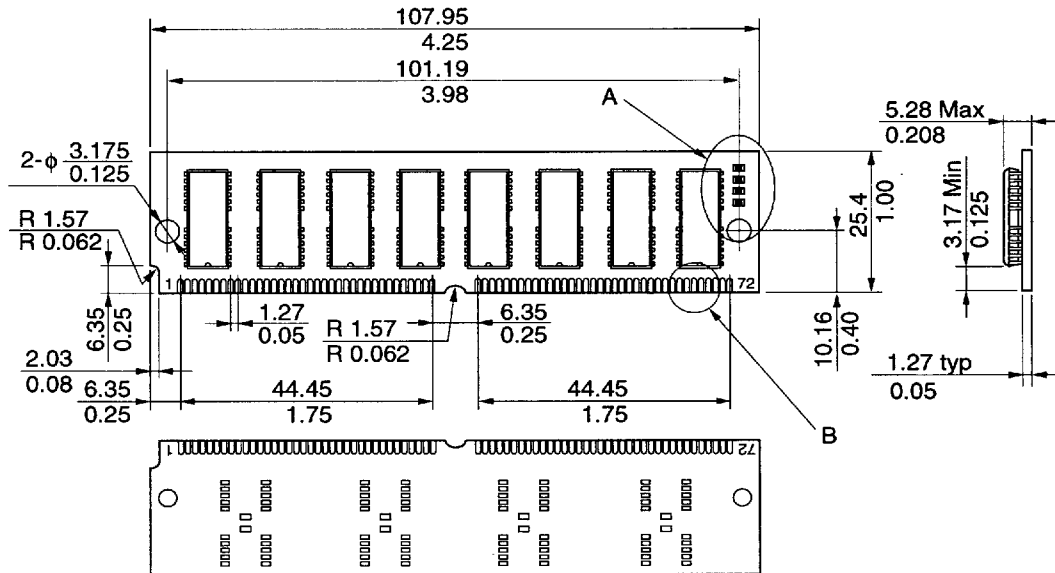
- Refer to the HM5117400B Series data sheet.
- The HB56A432 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}(\text{min})$).
Delayed write cycle is not available. ($\overline{OE}$ pin is fixed to V_{SS}).

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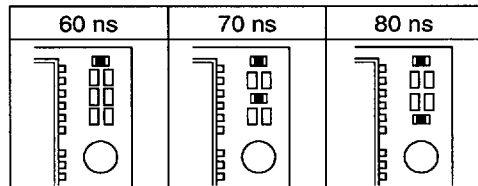
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Physical Outline

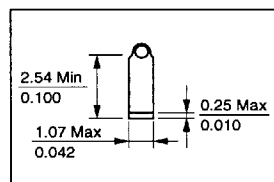
Unit: mm



Detail A



Detail B



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