

HB561009A-12, HB561009A-15, HB561009A-20

Preliminary
MARCH, 1986



262,144 × 9-bit Dynamic Random Access Memory Module

■ GENERAL DESCRIPTION

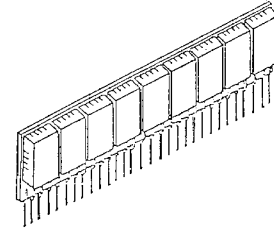
The HB561009A is a 2304K dynamic random-access memory module organized as 262,144 × 9-bits [bit nine (PD, PQ) is generally used for parity and is controlled by PCAS] in a 30-pin single-in-line package comprising nine HM50256CP, 262,144 × 1-bit dynamic RAM's in 18-pin Plastic Leaded Chip Carrier mounted on top of a substrate together and eight 0.1μF decoupling capacitors mounted beneath the chip carriers.

■ FEATURES

- 262,144 words × 9-bits Organization
- Industry standard 30-Pin Single Inline Package Memory Module
- Single 5V (± 10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561009A operates as nine HM50256CP as shown in the functional block diagram (P.2).
- Low Power:
 - Operating—2,160 mW TYP. (t_{RC} = 260ns)
 - Standby—135 mW TYP.
- High Speed:

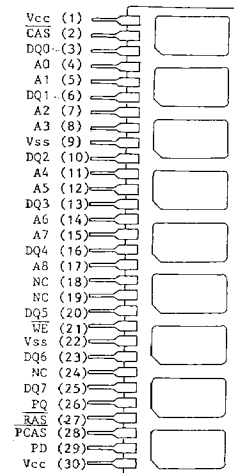
	Access Time from $\overline{\text{RAS}}$ (MAX)	Access Time from $\overline{\text{CAS}}$ (MAX)	Read or Write Cycle (MIN)
HB561009A-12	120ns	70ns	220ns
HB561009A-15	150ns	75ns	260ns
HB561009A-20	200ns	100ns	330ns
- Page Mode Capability
- TTL Compatible
- 256 Refresh Cycles (4ms)
- 3 Variations of Refresh
 - $\overline{\text{RAS}}$ only Refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
 - Hidden Refresh
- Operating Ambient Air, Temperature 0 ~ 70°C
- Common $\overline{\text{CAS}}$ control for eight common Data-In and Data-Out lines
- Separate $\overline{\text{CAS}}$ control for one separate pair of Data-In and Data-Out lines
- The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.



HB561009A

■ PIN ARRANGEMENT

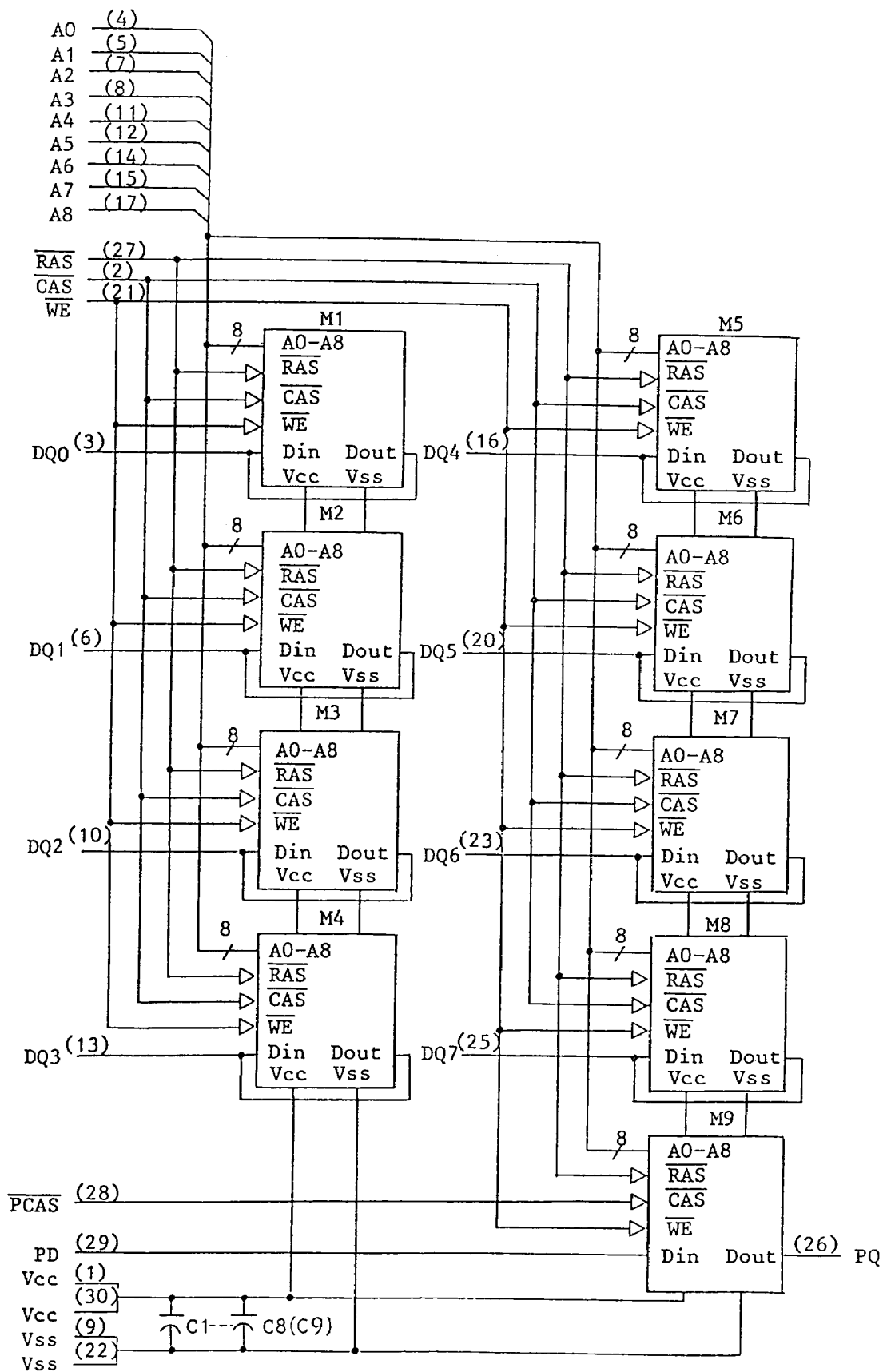


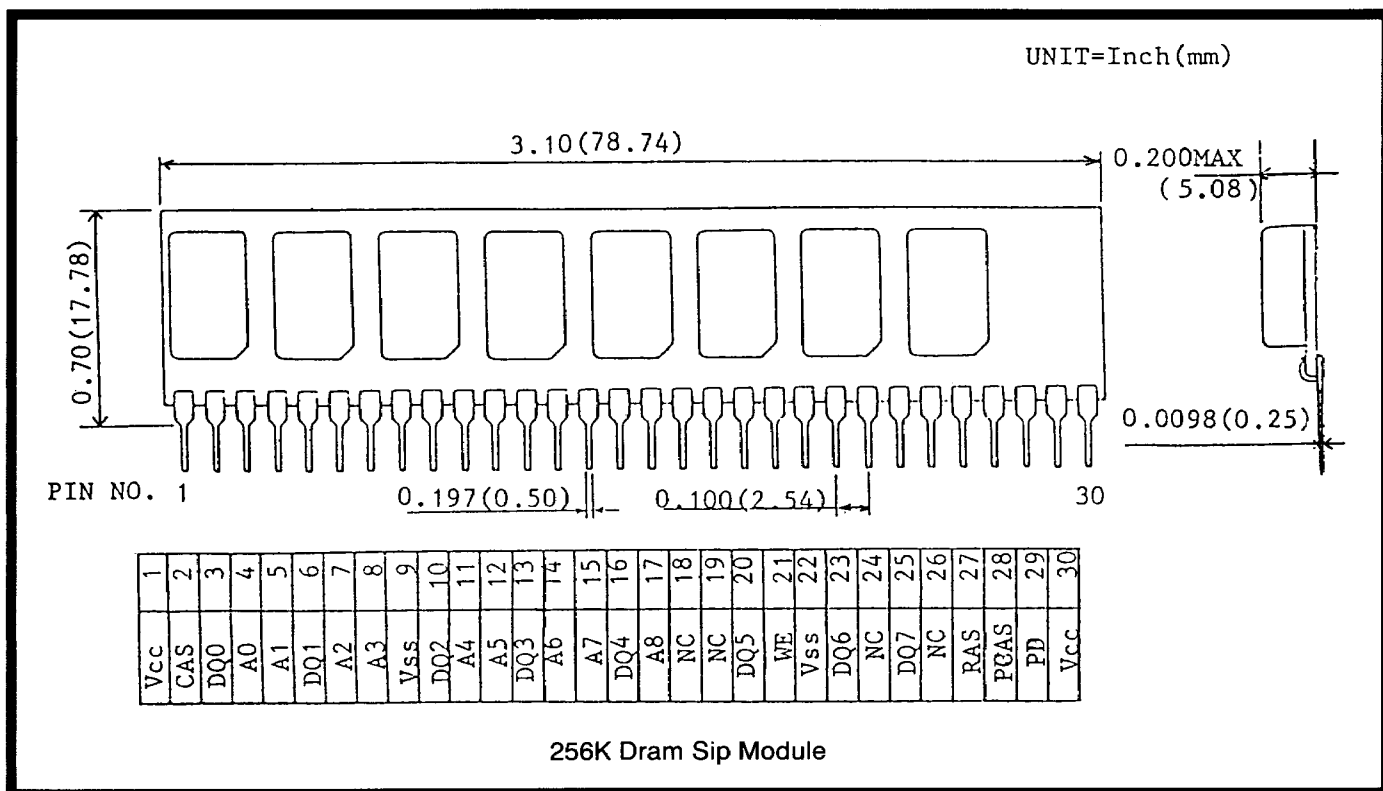
(Top View)

PIN NOMENCLATURE

A ₀ -A ₈	Address Inputs
CAS, PCAS	Column Address Strobes
DQ0-DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
RAS	Row Address Strobes
V _{CC}	+5V Supply
V _{SS}	Ground
WE	Write Enable

■ FUNCTIONAL BLOCK DIAGRAM





■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{ss}	-1V to 7V
Operating Temperature, T_a (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	-55°C to 125°C
Power Dissipation	9W
Short Circuit Output Current	50 mA

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{cc}	Supply voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High voltage	2.4		6.5	V	1
V_{IL}	Input Low voltage	-1.0		0.8	V	1

Notes:

All voltages referenced to V_{ss}

■ DC ELECTRICAL CHARACTERISTICS ($T_a = 0$ to 70°C $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

Symbol	Parameter	Min	Max	Unit	Notes
I _{cc1}	Operating current t _{RC} = 330 ns t _{RC} = 260 ns		495 630	mA	1
I _{cc2}	Standby current		40	mA	
I _{cc3}	Refresh current t _{RC} = 330 ns t _{RC} = 260 ns		378 477	mA	$\overline{\text{RAS}}$ only Refresh
I _{cc5}	Standby current (Dout Enable)		90	mA	1
I _{cc6}	Refresh current t _{RC} = 330 ns t _{RC} = 260 ns		405 522	mA	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
I _i (L)	Input leakage $0 < V_{in} < 7\text{V}$	-10	10	uA	
I _o (L)	Output leakage $0 < V_{out} < 7\text{V}$	-10	10	uA	Dout is disabled
VOH	Output levels High I _{out} = -5 mA	2.4	V _{CC}	V	
VOL	Low I _{out} = 4.2 mA	0	0.4	V	

■ AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Type	Max	Unit	Notes
CI1	Address		60	pF	2
CI2	Clocks		75	pF	2
CI3	DQ		17	pF	2,3
CI4	PQ		12	pF	2,3
CI5	PD		10	pF	2

Notes:

1. I_{cc} depends on output loading condition when the device is selected, I_{cc} max is specified at the output open condition.
2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
3. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

1), 9), 10) ($T_a = 0 \text{ to } 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

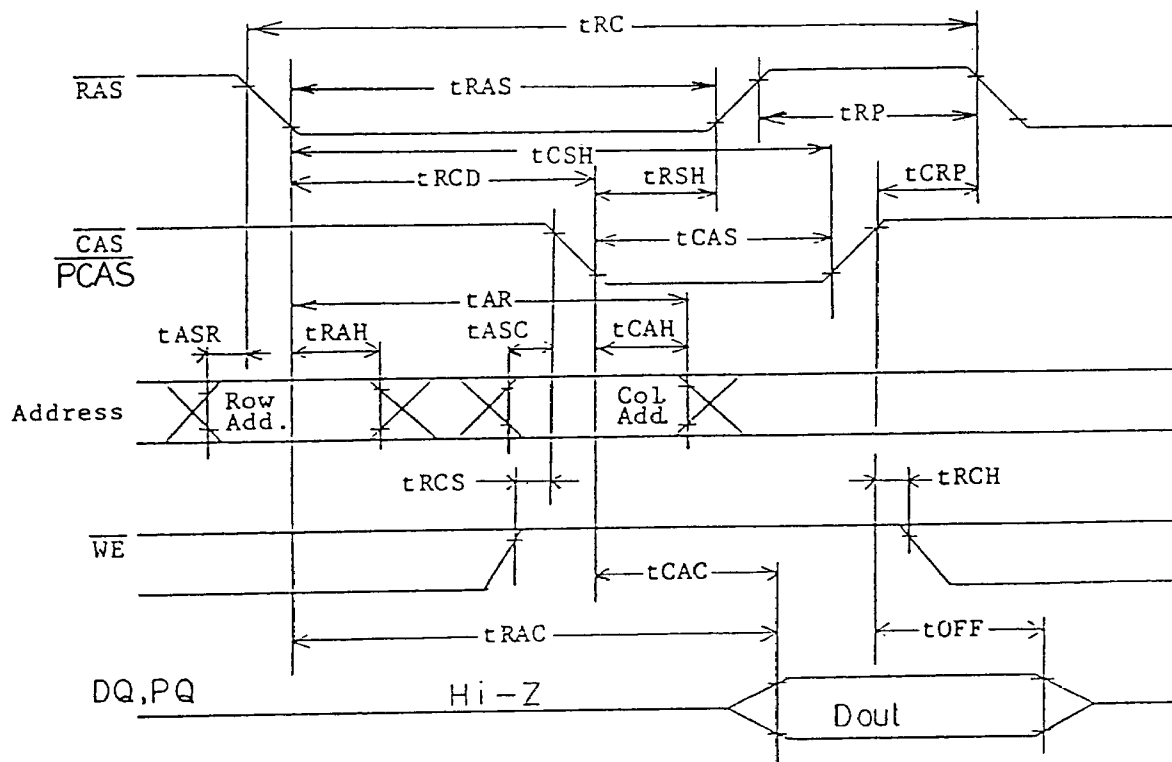
Symbol	HB561009A-12		HB561009A-15		HB561009A-20		Unit	Note
	min	max	min	max	min	max		
t_{RAC}		120		150		200	ns	2,3
t_{CAC}		70		75		100	ns	3,4
t_{OFF}		30		40		50	ns	5
t_T	3	50	3	50	3	50	ns	6
t_{RC}	220		260		330		ns	
t_{RP}	90		100		120		ns	
t_{RAS}	120	10000	150	10000	200	10000	ns	
t_{CAS}	70	10000	75	10000	100	10000	ns	
t_{RCD}	35	50	35	75	35	100	ns	7
t_{RSH}	70		75		100		ns	
t_{CSH}	120		150		200		ns	
t_{CRP}	10		10		10		ns	
t_{ASR}	0		0		0		ns	
t_{RAH}	15		15		20		ns	
t_{ASC}	0		0		0		ns	
t_{CAH}	25		25		30		ns	
t_{AR}	75		100		130		ns	
t_{WCS}	0		0		0		ns	8
t_{WCH}	40		45		55		ns	
t_{WCR}	90		120		155		ns	
t_{WP}	40		45		55		ns	
t_{RWL}	40		45		55		ns	
t_{CWL}	40		45		55		ns	
t_{DS}	0		0		0		ns	8
t_{DH}	40		45		55		ns	8
t_{DHR}	90		120		155		ns	
t_{RCS}	0		0		0		ns	
t_{RCH}	0		0		0		ns	
t_{RRH}	10		10		10		ns	
t_{REF}		4		4		4	ms	
t_{CPN}	50		60		80		ns	
t_{CSR}	10		10		10		ns	
t_{CHR}	120		150		200		ns	
t_{RPC}	0		0		0		ns	

Notes:

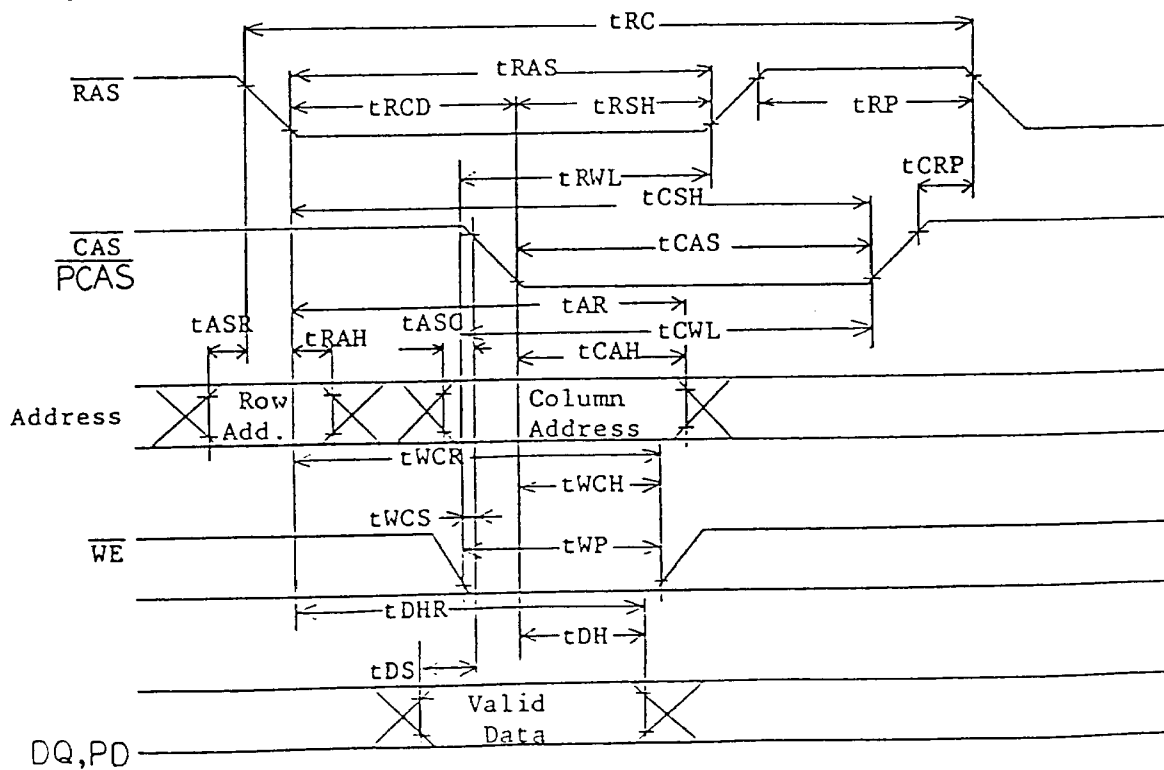
1. AC measurements assume $t_T = 5\text{ns}$.
2. Assumes that $t_{RCD} < t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} > t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met; $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} .
8. Early write cycle only ($t_{WCS} > t_{WCS}(\text{min})$)
9. An initial pause of 100 μs is required after power-up, then execute at least 8 initialization cycles.
10. At least, 8 CAS before RAS refresh cycle are required before using internal refresh counter.

■ WAVE FORMS

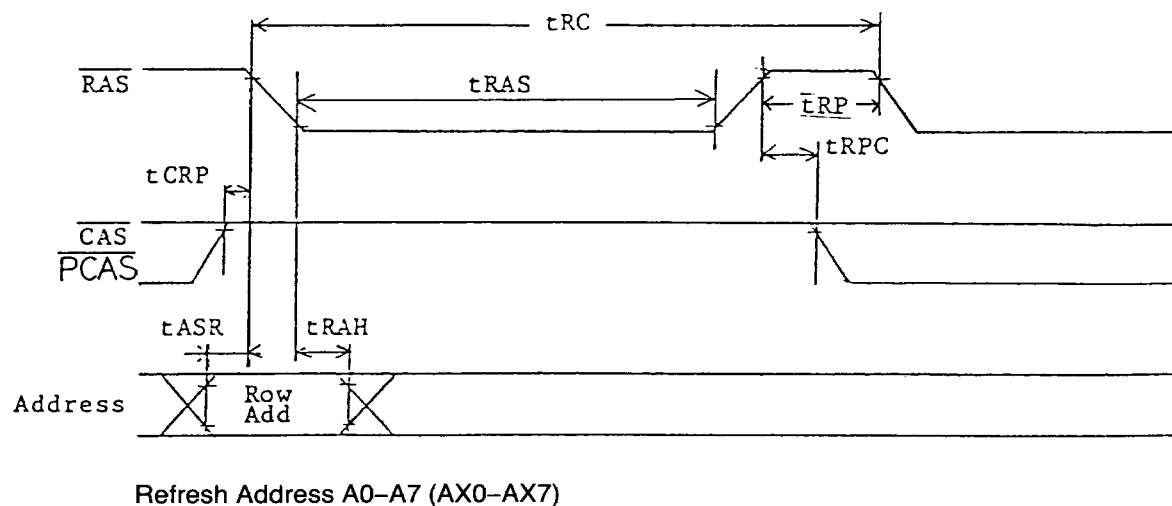
Read Cycle



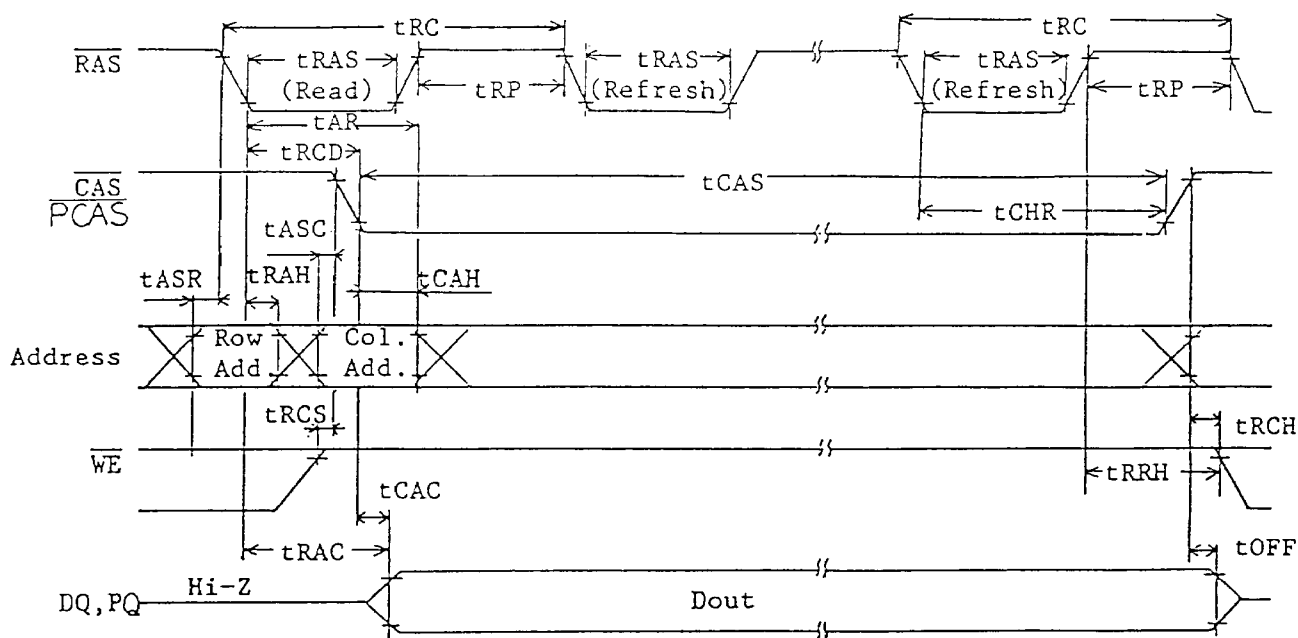
Write Cycle



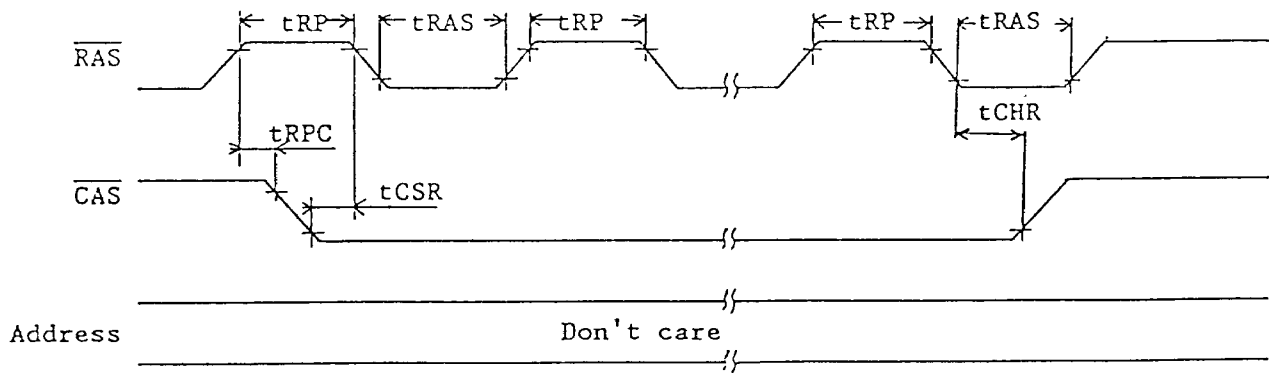
RAS Only Refresh Cycle



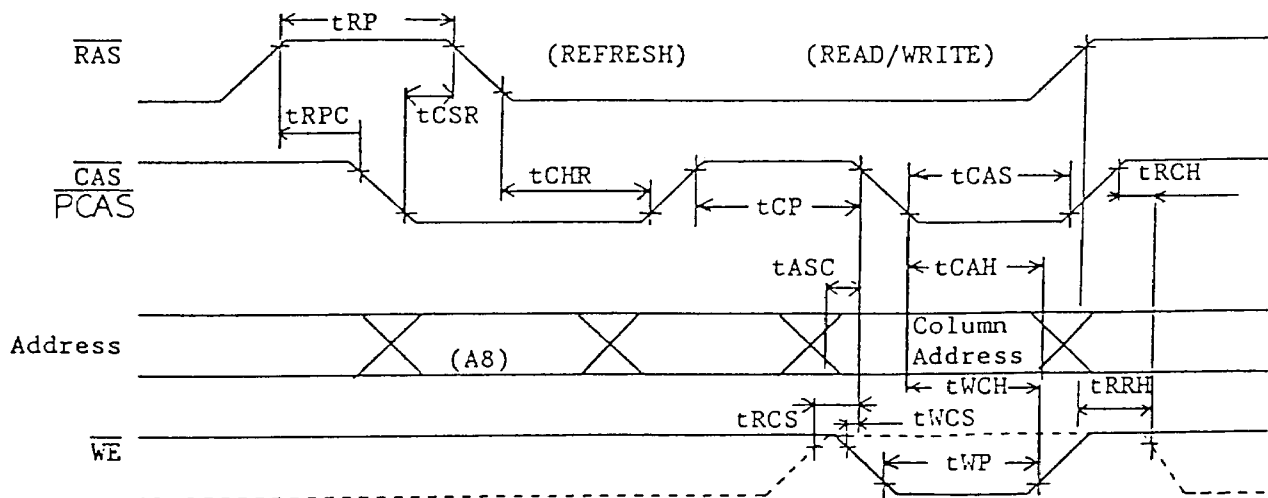
Hidden Refresh Cycle



$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

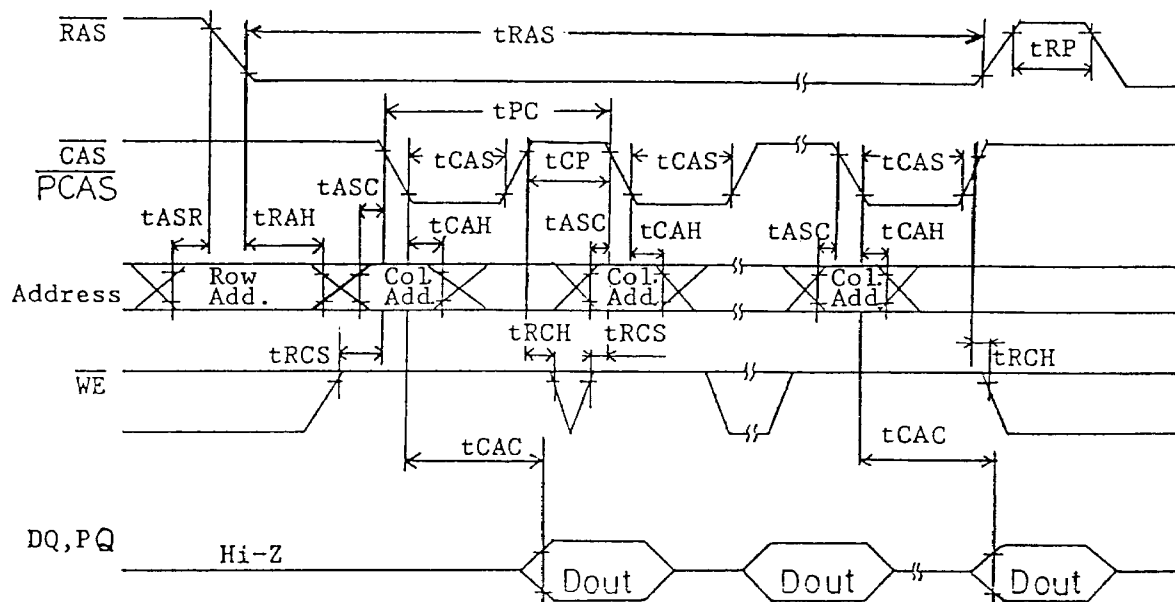


Counter Test

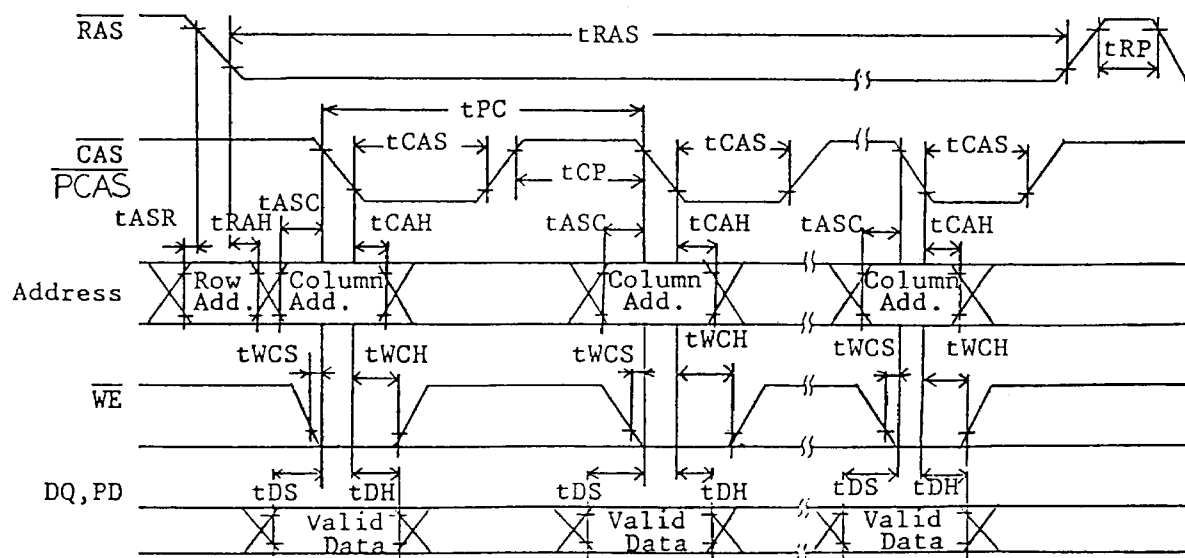


	HB561009A-12		HB561009A-15		HB561009A-20		unit	note
	min	max	min	max	min	max		
Icc7		513		432		333	mA	
tPC	130		145		190		ns	
tCP	50		60		80		ns	

Page Mode Read Cycle



Page Mode Write Cycle



The information in this data sheet has been carefully checked; however, the contents of this data sheet may be changed and modified without notice. The company shall assume no responsibility for inaccuracies, or any problem involving a patent caused when applying the descriptions in this data sheet.



We make things possible

Hitachi America, Ltd.

Semiconductor and IC Division

2210 O'Toole Avenue, San Jose, CA 95131 1-408-435-8300