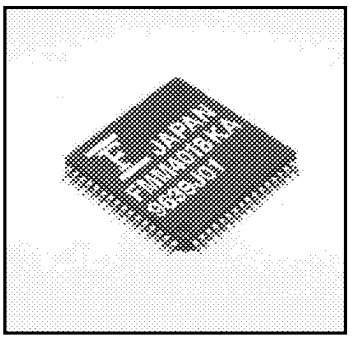
FMM4018KA/KB

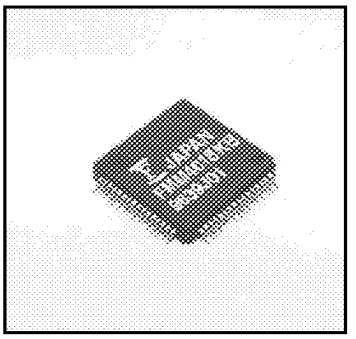
1.0625Gbps Fibre Channel IC

FEATURES

- 1.0625Gbps FIBRE CHANNEL
  based on ANSI X3T11 FC-0 layer
- 1 Chip Transmitter and Receiver with PLLs
- 10-Bit Interface for Transmitter and Receiver
- Very Low Power Consumption: 0.55W
- Single Power Supply Voltage: +3.3V
- LVTTL and PECL Interface
- Thermally Enhanced, QFP64 Mold Package with Heat Sink
- Standard Package, KA (14mm) and Small Package Outline, KB (10mm)



KA PACKAGE



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DESCRIPTION

The FMM4018 is a one-chip monolithic transmitter and receiver IC product that uses 0.5µm GaAs MESFET technology. It is compatible with ANSI X3T11 and supports Fibre Channel physical layer FC-0.

ABSOLUTE MAXIMUM RATINGS (Ambient Temperature Ta = 25°C)

Parameter		Symbol	Values	Unit
Supply Voltage		V_{DD}	-0.5 ~ +4.0	V
Output Current	PECL	I_{OUT}	-50 ~ +50	mA
	LVTTL	I_{OUT}	-25 ~ +25	mA
Input Voltage	PECL	V_{IN}	-0.5 ~ VDD+0.5	V
	LVTTL	V_{IN}	-0.5 ~ 5.5	V
Maximum Input ESD (MIL-STD-883C)		V_{ESD}	1500	V
Storage Temperature		T_{STG}	-65 ~ +150	°C
Case Temperature		T_C	-55 ~ +120	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values	Unit
Supply Voltage	V_{DD}	+3.3 ~ ±5%	V
AC Coupled Differential PECL Output Load	R_L	50	Ω
Ambient Temperature	T_A	0 ~ +70	°C
Junction Temperature	T_J	0 ~ +100	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS for PECL (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Limit		Unit
			Min.	Max.	
Single Ended Output Voltage Swing	V_{OUT}	50Ω to V_{DD} -2.0V	600	1300	mV
Differential Input Voltage Swing	V_{IND}	–	200	2600	mV

DC CHARACTERISTICS FOR LVTTL (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Value		Unit
			Min.	Max.	
Output HIGH Voltage	V_{OH}	I_{OH}=-1.0mA	2.4	V_{DD}	V
Output LOW Voltage	V_{OL}	I_{OL}=+1.0mA	0	0.6	V
Input HIGH Voltage	V_{IH}	–	2.0	5.5	V
Input LOW Voltage	V_{IL}	–	0	0.8	V
Input HIGH Current	I_{IH}	V_{IN}=V_{DD} -0.5V	-	50	μA
Input LOW Current	I_{IL}	V_{IN}=0.5V	-500	-	μA

SUPPLY CURRENT

Parameter	Symbol	Test Conditions	Limit		Unit
			Min.	Max.	
Supply Current	I_{DD}	V_{DD} = +3.3V, T_A = 25°C, 50Ω TO V_{DD} -2.0V	–	220	mA

AC CHARACTERISTICS (V_{DD}=3.3V, T_A=25°C)

Parameter	Symbol	Test Conditions	Value		Unit
			Min.	Max.	
Serial Baud Rate	B_r	–	1040	1080	Mbps
Parallel Clock Rate	F_{tbc}	–	104.0	108.0	MHz
Frequency Offset	F_{off}	Transmitter and Receiver frequency offset	-100	+100	ppm
TX/TXN Rise and Fall Time	T_{tr}, T_{tf}	20% to 80% 50Ω single ended load	-	300	pS
TTL Output Rise and Fall Time	T_{ttr}, T_{ttf}	0.8 to 2.0V with 10pF load	-	2.4	nS
Frequency Lock Time	T_{FL}	–	-	500	µS
Bit Lock Time	T_{BL}	–	-	2500	bit
Random Jitter	J_{RC}	TX K28.7 Pattern	-	10	pS
Deterministic Jitter	J_{DC}	TX K28.5 Pattern	-	100	pS

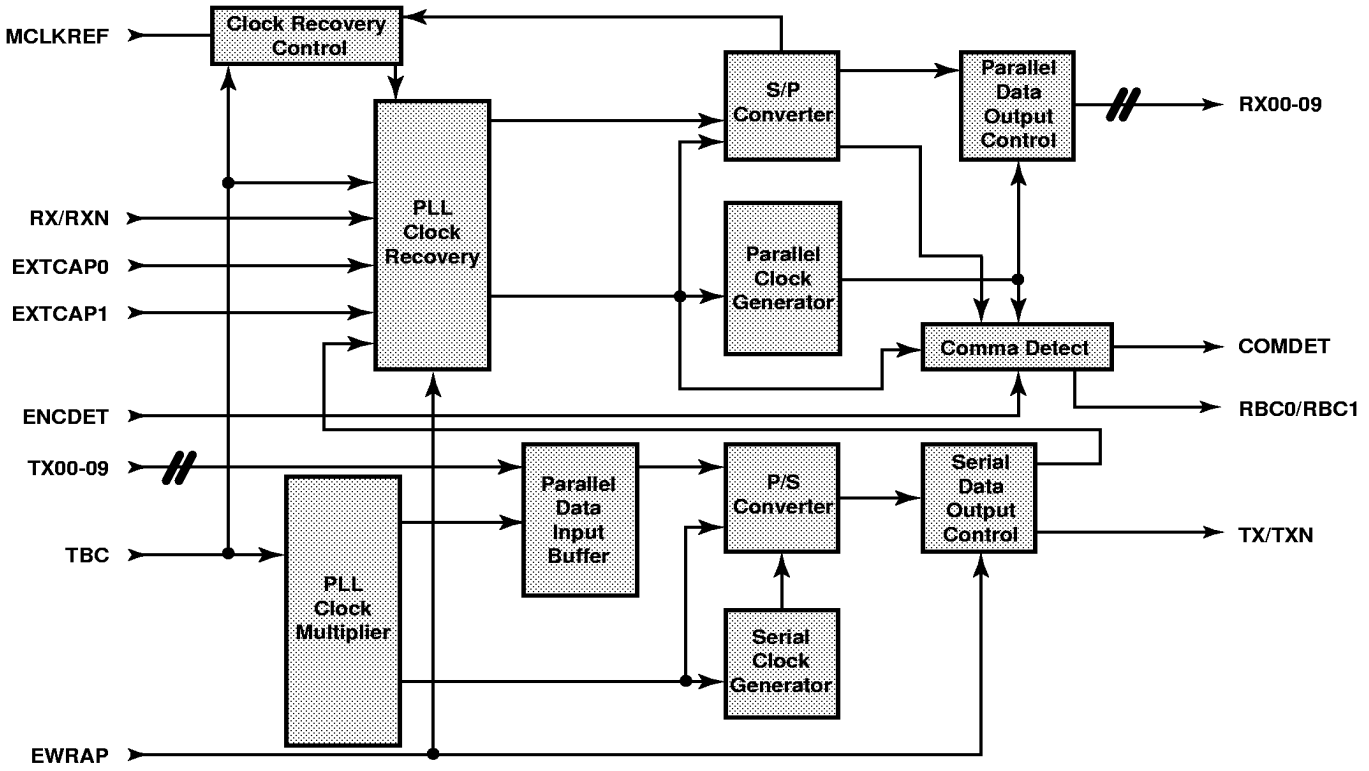


Figure 1: Functional Block Diagram of FMM4018KA/KB

Clock Multiplier

The input reference clock (TBC) is multiplied up to 10 times by the PLL to generate a high speed clock for serial data output. The TBC clock rate is nominally at 106.25MHz. The 10x multiplier results in a 1.0625GHz internal clock rate. The PLL multiplier does not need any additional external elements for the loop filter.

In order to have a clear eye pattern, the jitter of the PLL must be small. The PLL's jitter is caused by the phase noise of the VCO (Voltage Controlled Oscillator) and reference clock (TBC). The phase noise of the reference clock is small since it is usually a crystal oscillator. The PLL suppresses the VCO's phase noise near the oscillation frequency by phase locking to the reference clock. The closed loop transfer function of the PLL is designed to optimize phase noise between the VCO and reference clock. The phase noise of the VCO decreases as f^3 from the oscillation frequency (where f is offset from carrier), while the phase noise of the crystal oscillator increases as f^2.

One of the main concerns in high speed serial communications is jitter. The Fibre Channel jitter working group defines jitter as "short-term, non-cumulative deviation from the ideal timing of an event". There are two types of jitter, deterministic and random. Deterministic jitter is non-random in nature and is commonly associated with bandwidth limitations and power supply noise. Random jitter is Gaussian in nature. The source of random jitter in the SERDES chip is phase noise of the PLL. It can be measured using a K28.7 output pattern. With this technique, the FMM4018 has less than 10pS of jitter.

Parallel to Serial

The FMM4018 converts the 10-bit input parallel data to high speed serial data. The transmitted data format starts from the input parallel data TX00 to TX09. The 10-bit parallel data is latched to the input parallel F/Fs using the TBC clock. The data is then serialized by high speed shift registers. The differential output is on the high speed PECL output pins. The differential PECL outputs reduce the common mode noise from the power supply. The output is suitable for symmetrical transmission lines such as shielded twisted pair cable.

Clock Recovery

The FMM4018 extracts a clock signal from high speed input serial data. The FMM4018 uses two methods to extract clock signal from the serial data. The first is manual clock recovery using the MCLKREF signal. The second method is auto clock recovery. The manual clock recovery technique is as follows:

(1) The MCLKREF signal must be low for more than 500µS in order to lock to TBC
(2) After 500µS, MCLKREF is set high to lock to input serial data

The PLL of the receiver block is essentially the same as the transmitter block. When MCLKREF is low, the PLL functions as a clock multiplier similar to the transmitter PLL. TBC is used as the reference clock. When MCLKREF is high, the receiver PLL functions as a phase aligner. The receiver PLL aligns the phase to that of the input serial data. An external 0.1µF capacitor is required for the loop filter.

When MCLKREF is high, the auto clock recovery either counts the changes in the serial data of compares the frequency between TBC and recovered clock. Fibre Channel uses 8B/10B code to reduce DC levels of output serial data, so there must be at least one change in the serial input data during normal operation. If there is no change (fixed low or high) in the input serial data, the auto clock recovery circuit behaves as MCLKREF low state. When input serial data stream is normal, the auto clock recovery behaves as MCLKREF high. To enable auto clock recovery, values of the 10-bit shift registers are compared to determine whether they are fixed high or low. The Fibre Channel specification defines the allowable frequency offset (±100ppm) between the transmitter and receiver block. When the offset frequency between the recovered clock and 10 times TBC clock exceeds ±0.1%, the auto clock recovery circuit behaves as MCLKREF low.

Serial to Parallel

The FMM4018 converts the high speed serial input data to 10-bit parallel data which is available on the output F/Fs. Proper data alignment is required to regenerate the data frame. The comma detect word (K28.5) is used to locate the starting position of the 10-bit data in received serial stream. The data of each shift register is continuously compared with the comma detect word. If the two are identical, frame synchronization has occurred and frame sync (COMDET) is sent. When frame sync is confirmed, the RBC0/1 is aligned to the next receiver block (FC1 layer IC). This alignment method preserves a stable signal but results in stretching of RBC0 and RBC1 as shown in Figures 6, 7 and 8.

Synchronization

In serial transmission systems, frame synchronization is important since it detects the start of the data stream with a unique word. Fibre Channel uses a comma word which is always transmitted when the line is idle allowing the client system to synchronize to the server's system clock.

Frame synchronization and related output information have the following unique characteristics:

(1) RBC0 and RBC1 clock stretch

If comma word is received and realignment of received data is necessary, RBC0 and RBC1 clocks signals are stretched. Therefore, data will not be properly received at the first detection of the comma word.

(2) Non-consecutive transmission of the comma word

For proper comma detection, the comma word must not be transmitted consecutively. FC-0 specifications for word synchronization states that three 10-bit words plus comma detect word should be used.

Data Format of Fibre Channel

Fibre Channel uses code conversion techniques to eliminate the DC component in the transmitted spectrum. This is a desirable feature because it allows the use of AC coupling techniques. Fibre Channel converts 8-bit data to 10-bit data adding redundant bits. The 8-bit data has 256 (2^8) combinations, and the 10-bit data has 1024 (2^{10}) combinations. Therefore, 768 patterns are reserved for code balance of ("1" and "0"), special function codes, and framing word, etc. In order to regenerate the frame format from the received serial data, a comma word is required for receiver data alignment. Fibre Channel assigns the K28.5 as the "comma word".

Package Information

The FMM4018 is available in two package types: 10mm and 14mm size, thermally enhanced HQFP package. These packages have a copper heat spreader for die attach to reduce the thermal resistance from the chip junction to the package surface.

Figure 2: Package Pin Assignment

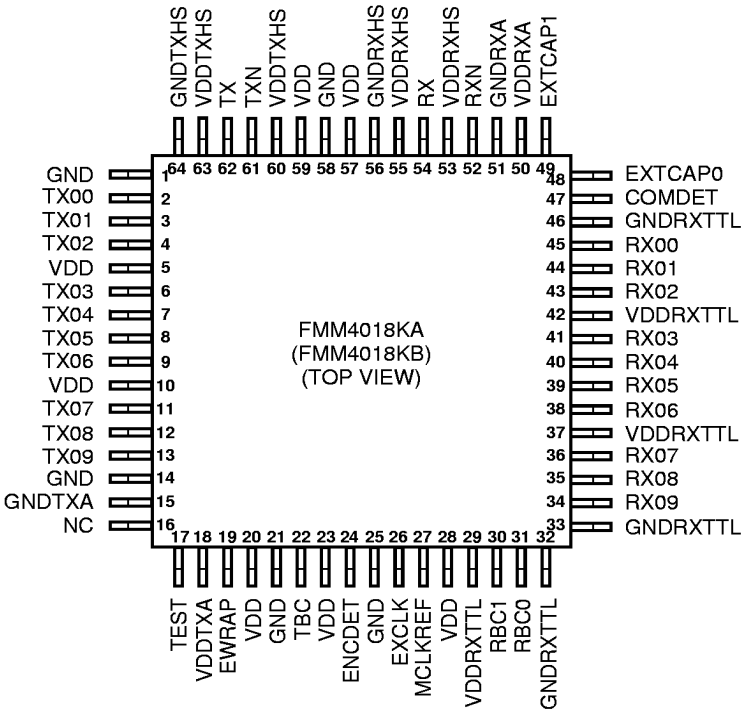


Table 1: Pin Description of Power Supply Voltage

Pin Name	Pin No.	Description
GND	1, 14, 21, 25, 58	**Ground for Logic Gates: 0V**
GNDTXA	15	**Analog Ground for TX: 0V**
GNDTXHS	64	**Ground for High Speed TX: 0V**
GNDRXA	51	**Analog Ground for RX: 0V**
GNDRXHS	56	**Ground for High Speed RX: 0V**
GNDRXTTL	32, 33, 46	**TTL Ground: 0V**
VDD	5, 10, 20, 23, 28, 57, 59	**Power Supply for Logic Gate: 3.3V**
VDDTXA	18	**Analog Power Supply for TX: 3.3V**
VDDTXHS	60, 63	**High Speed Power Supply for TX: 3.3V**
VDDRXA	50	**Analog Power Supply for RX: 3.3V**
VDDRXHS	53, 55	**High Speed Power Supply for RX: 3.3V**
VDDRXTTL	29, 37, 42	**TTL Output Power Supply: 3.3V**
NC	16	**N/C, leave open**

Table 2: Pin Description

Pin Name	Pin No.	I/O	Description
TX00 TX01 TX02 TX03 TX04 TX05 TX06 TX07 TX08 TX09	2 3 4 6 7 8 9 11 12 13	I-TTL	Data Inputs TX00 is the first bit transmitted
TBC	22	I-TTL	Transmit Byte Clock This is the 106.25MHz reference clock supplied by host system. The transmitter and receiver block use this clock for its reference clock. This clock signal must have good signal integrity.
TX TXN	62 61	O-PECL	High Speed Serial Data Output These lines are active when EWRAP is low. When EWRAP is high, TX and TXN hold low and high respectively.
EXCLK	26	I-TTL	Factory Test Pin This signal used for factory test only. For normal operation, leave it open.
TEST	17	I-TTL	Factory Test Pin This signal used for factory test only. For normal operation, leave it open.
RX RXN	54 52	I-PECL	High Speed Serial Data Input These lines are active when EWRAP is low. These pins are internally biased to VDD/2 by internal resistors.
RX00 RX01 RX02 RX03 RX04 RX05 RX06 RX07 RX08 RX09	45 44 43 41 40 39 38 36 35 34	O-TTL	Data Outputs RX00 is the first bit received.
RBC0 RBC1	31 30	O-TTL	Recovered Byte Clock of Receiver
COMDET	47	O-TTL	Comma Detect Output
ENCDET	24	I-TTL	Enable Byte Sync of Receiver When ENCDET is high, it enables byte sync. When ENCDET is low, it maintains the incoming data stream format.
EWRAP	19	I-TTL	Loopback Enable When EWRAP is high, it enables loopback When EWRAP is low, it operates as normal mode.
MCLKREF	27	I-TTL	Master Clock Reference When MCLKREF is low, PLL locks to TBC. When MCLKREF is high, PLL locks to recovered data.
EXTCAP0 EXTCAP1	48 49	EXT	External Capacitor Terminal for Loop Filter (0.1μF)

I-TTL: LVTTL INPUT, O-TTL: LVTTL OUTPUT, I-PECL: PECL INPUT, O-PECL: PECL OUTPUT, EXT: EXTERNAL TERMINAL

Table 3: Timing Characteristics of Transmitter Section

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Setup Time	T_{TSUP}	2.0	-	-	nS
Hold Time	T_{THLD}	1.5	-	-	nS
Latency Time	T_{TLAT}	-	5.4	-	nS

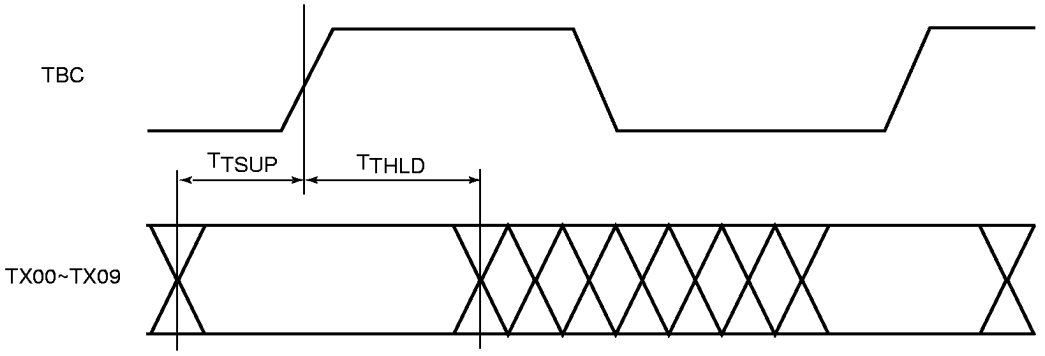


Figure 3: Transmitter Timing 1

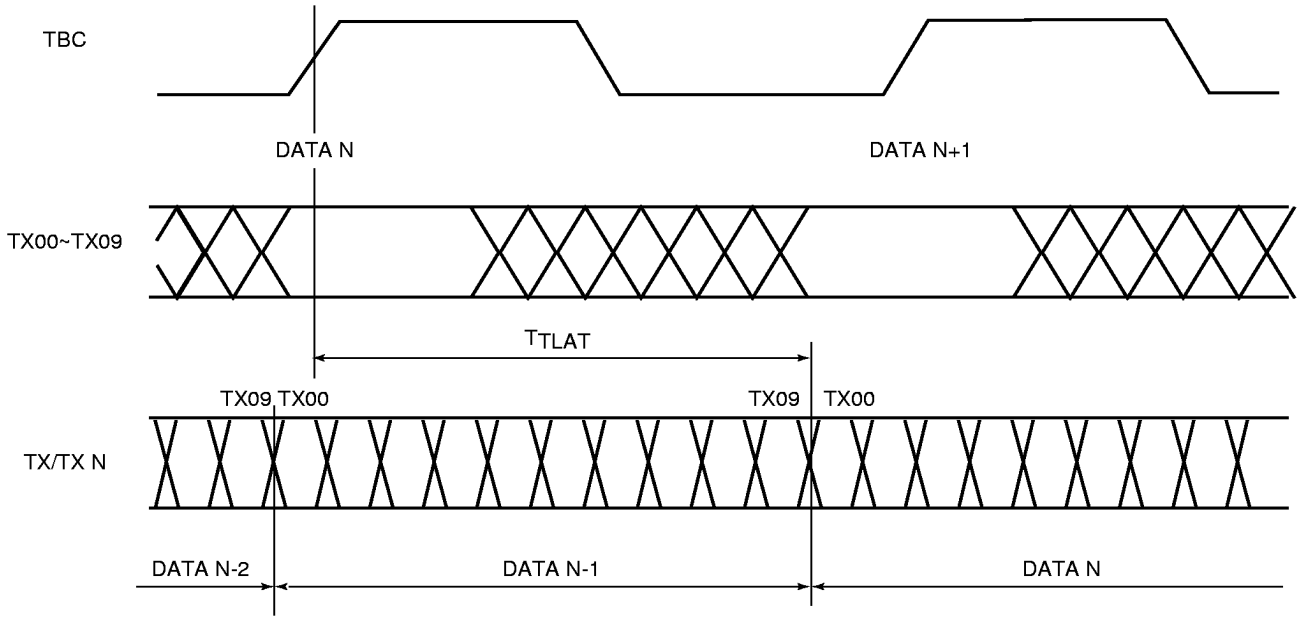


Figure 4: Transmitter Timing 2

Table 4: Timing Characteristics of Receiver Section

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Setup Time	T_{RSUP}	3.0	-	-	nS
Hold Time	T_{RHLD}	1.5	-	-	nS
Latency Time	T_{RLAT}	-	17.0	-	nS

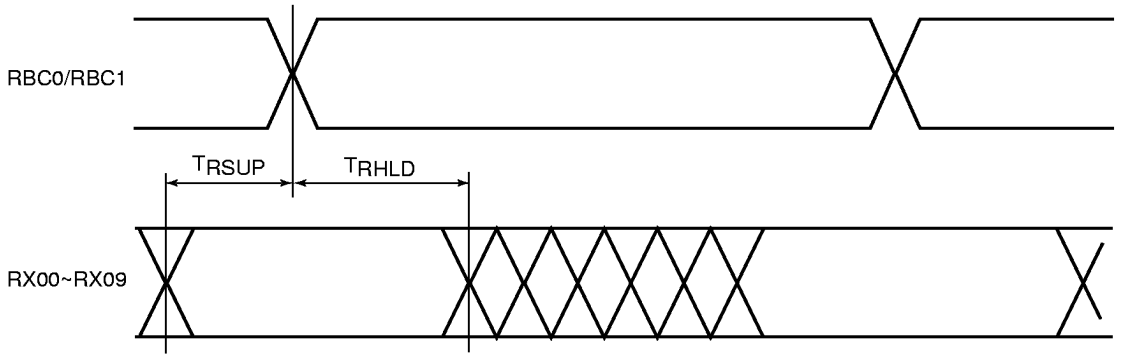


Figure 5: Receiver Timing 1

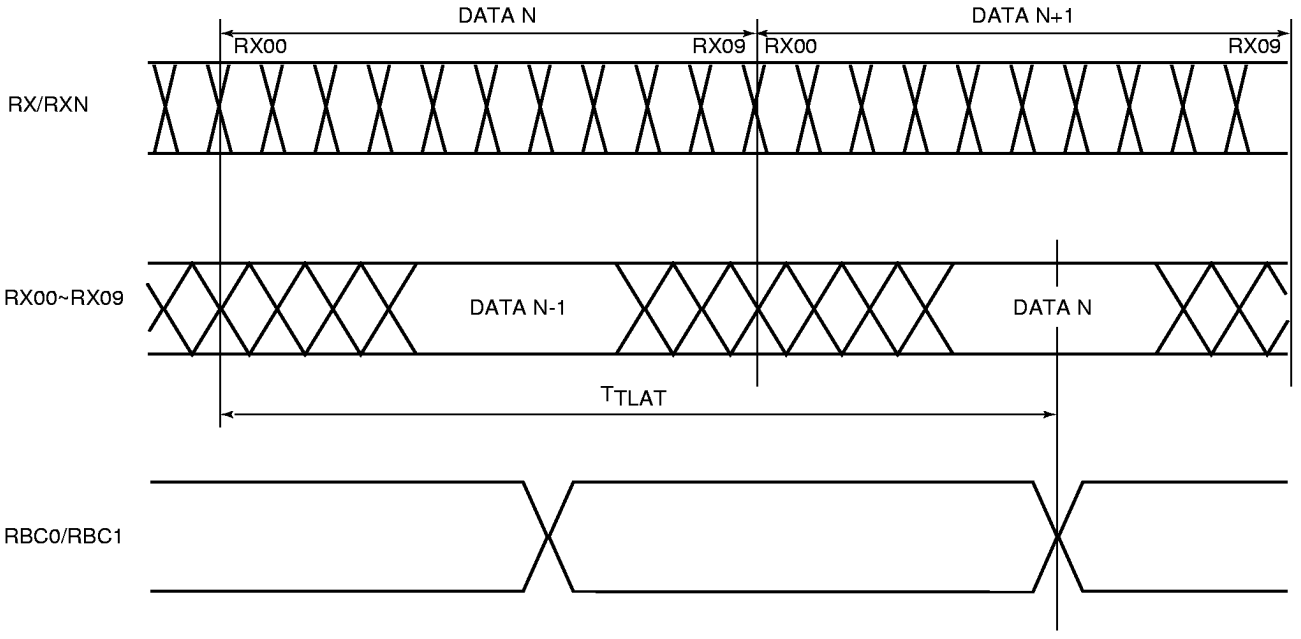


Figure 6: Receiver Timing 2

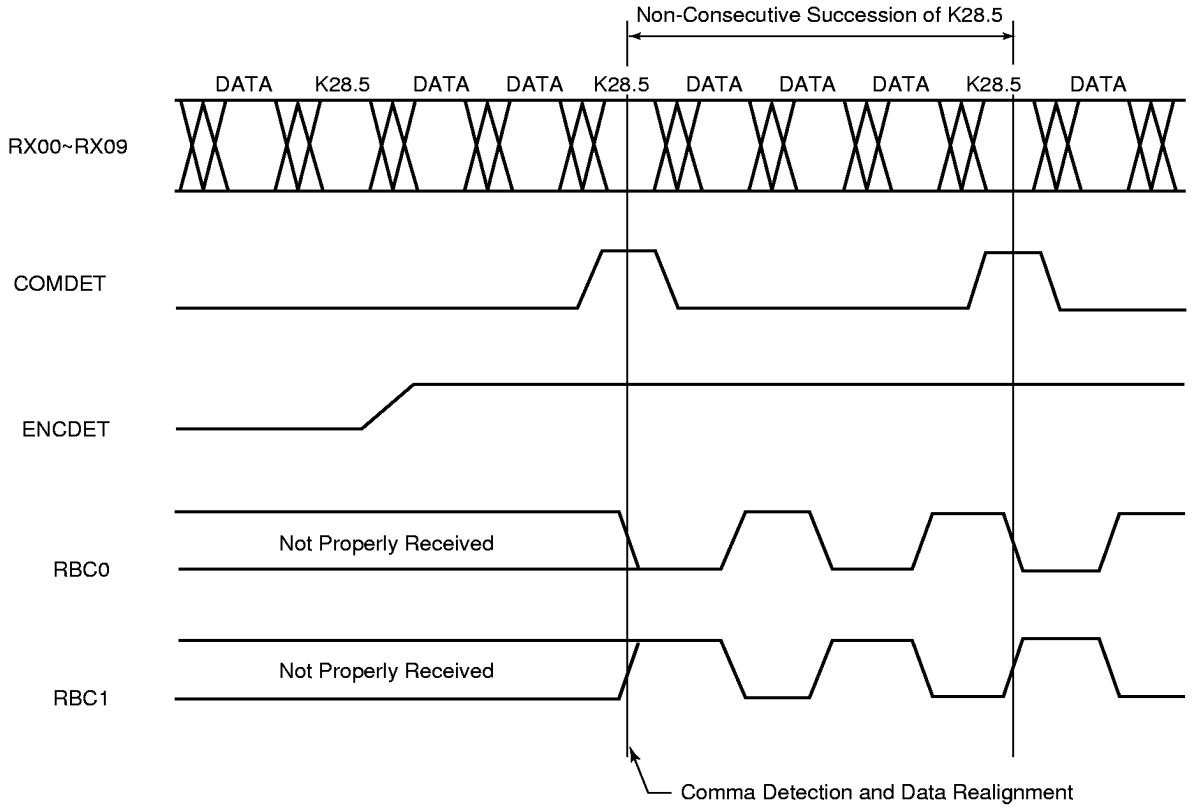


Figure 7: Synchronization Timing 1

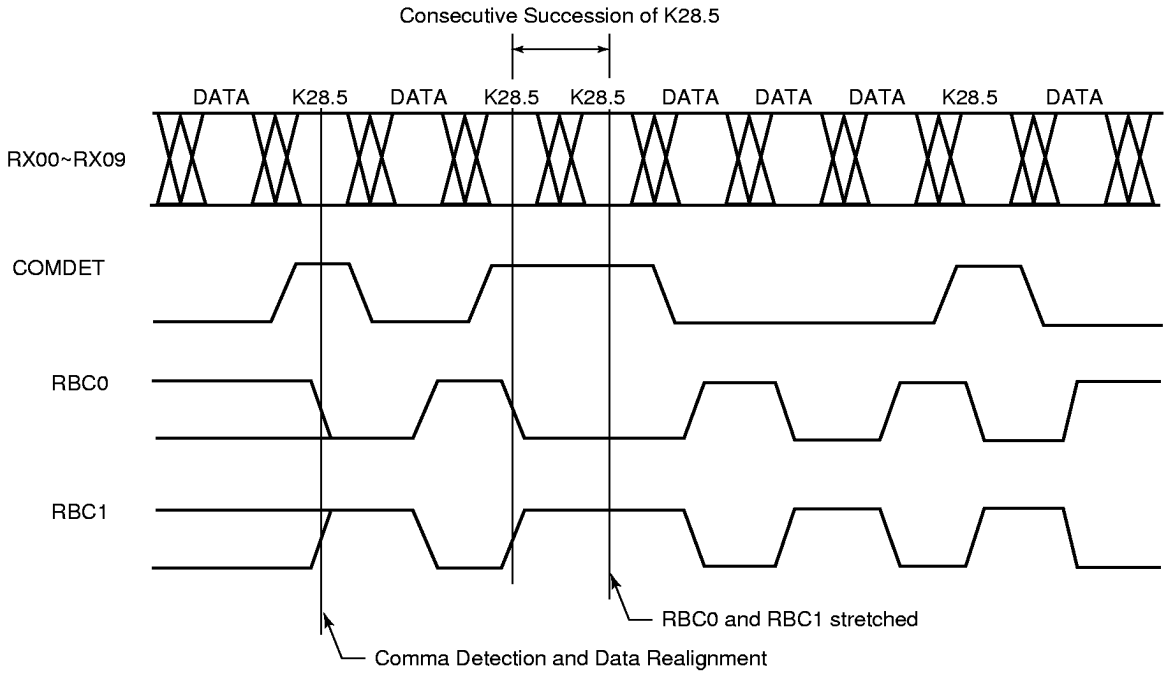


Figure 8: Synchronization Timing 2

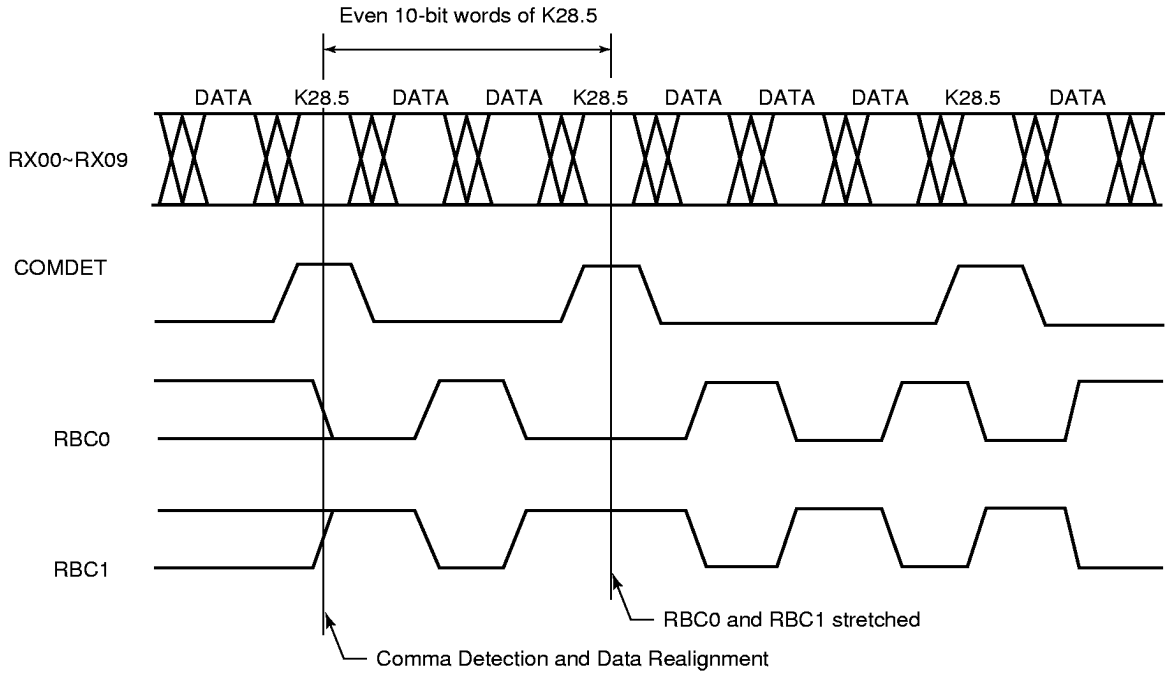


Figure 9: Synchronization Timing 3

High Speed Signal Termination

The FMM4018 has two high speed differential output pins. These pins must be terminated to psuedo ECL termination levels (VDD -2.0V). Figure 11 shows a typical termination circuit.

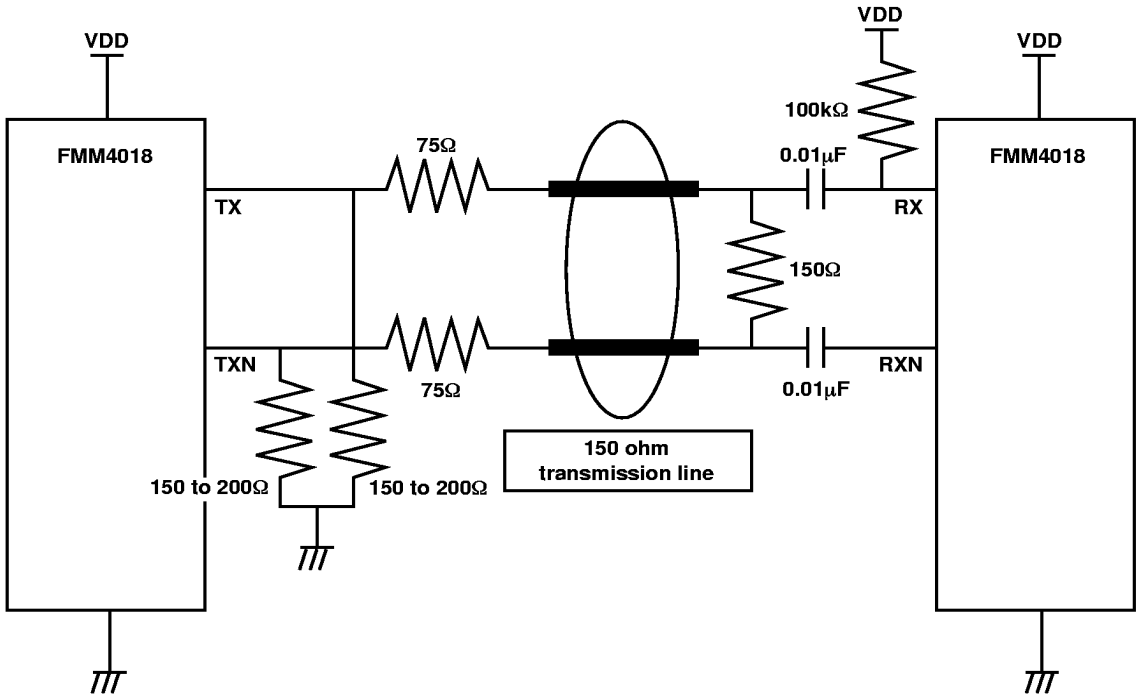
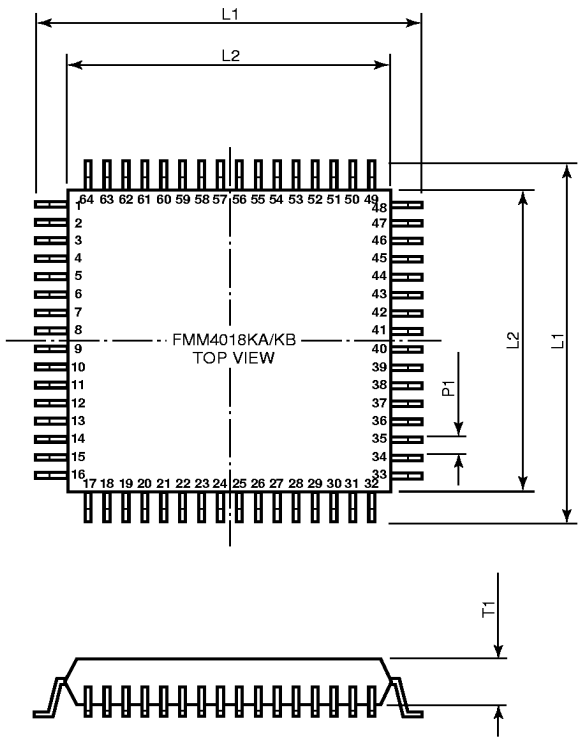


Figure 10: Termination Circuit for PECL Output

Power Supply Circuit

To reduce power supply noise, the bypass capacitors should be used as close as possible to each power supply pin. The FMM4018 has both analog and digital circuitry. The power supply for analog circuitry must be as noise free as possible. Ferrite beads are recommended for reducing power supply noise. All bypass capacitors are 0.1μF ceramic chip capacitor. For receiver block PLL, 0.1μF ceramic chip capacitor is required.

Case Style KA/KB



Item	FMM4018KA	FMM4018KB
L1	16.0mm	12.0mm
L2	14.0mm	10.0mm
P1	0.8mm	0.5mm
T1	1.4mm	1.4mm

For further information please contact:

FUJITSU COMPOUND SEMICONDUCTOR, INC.
2355 Zanker Rd.
San Jose, CA 95131-1138, U.S.A.
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Compound Semiconductor Division
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Phone:+44 (0)1628 504800
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