Octal bus transceiver/register, inverting (3-State)

54ABT648

FEATURES

- Combines 54ABT245 and 54ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real–time and stored data
- Output capability: +48mA/–24mA
- Latch–up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 54ABT648 high–performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

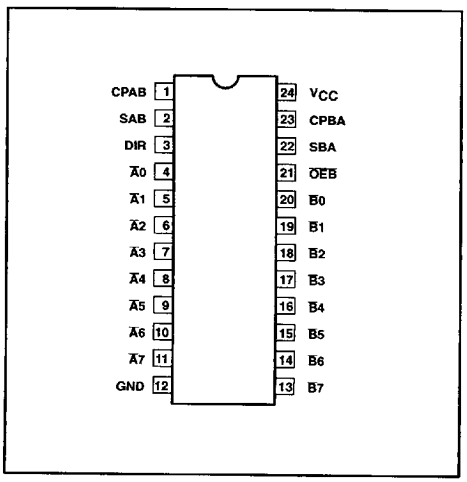
The Select (SAB, SBA) pins determine whether data is stored or transferred through the device in real–time. The DIR determines which bus will receive data when the $\overline{OE}$ is active (Low). In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. Outputs from real–time, or stored registers will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time. The examples on the next page demonstrate the four fundamental bus management functions that can be performed with the 54ABT648. The 54ABT648 transceiver/register consists of bus transceiver circuits with inverting 3–State outputs, D–type flip–flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

ORDERING INFORMATION

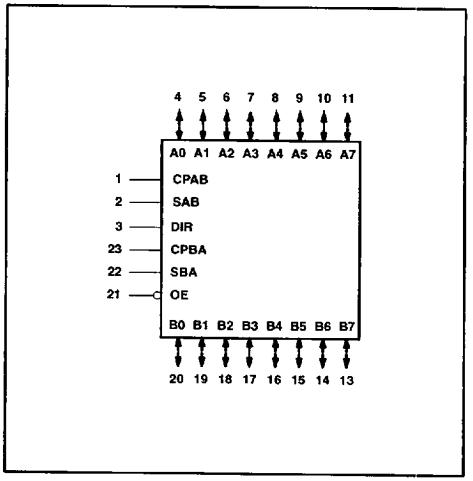
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-pin Ceramic DIP (300mil)	54ABT648/BLA	GDIP3-T24
28-pin LLCC	54ABT648/B3A	CQCC2-N28

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

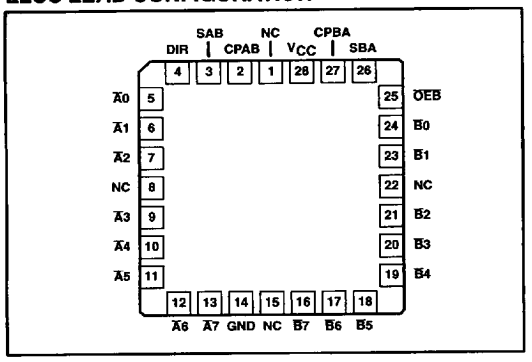
PIN CONFIGURATION

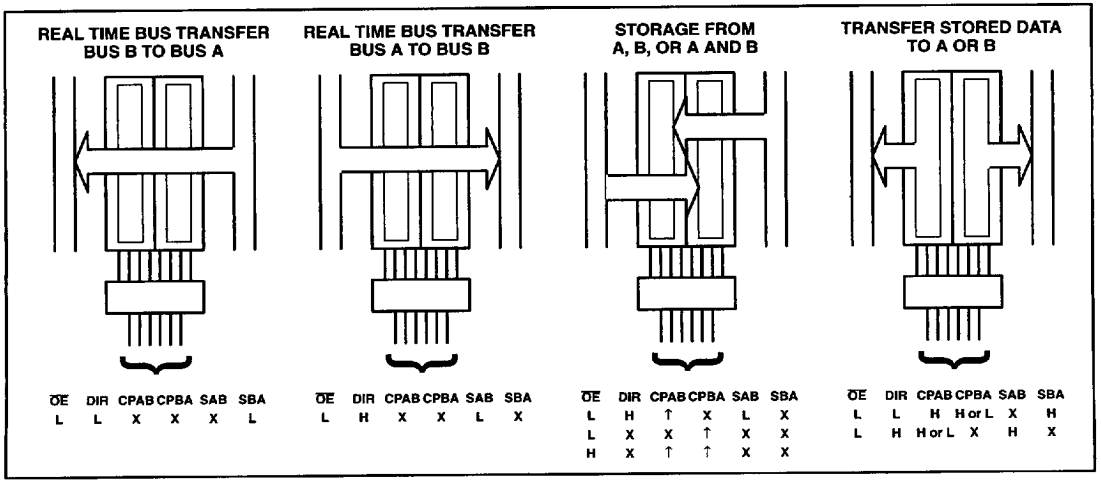


LOGIC SYMBOL



LLCC LEAD CONFIGURATION





PIN DESCRIPTION

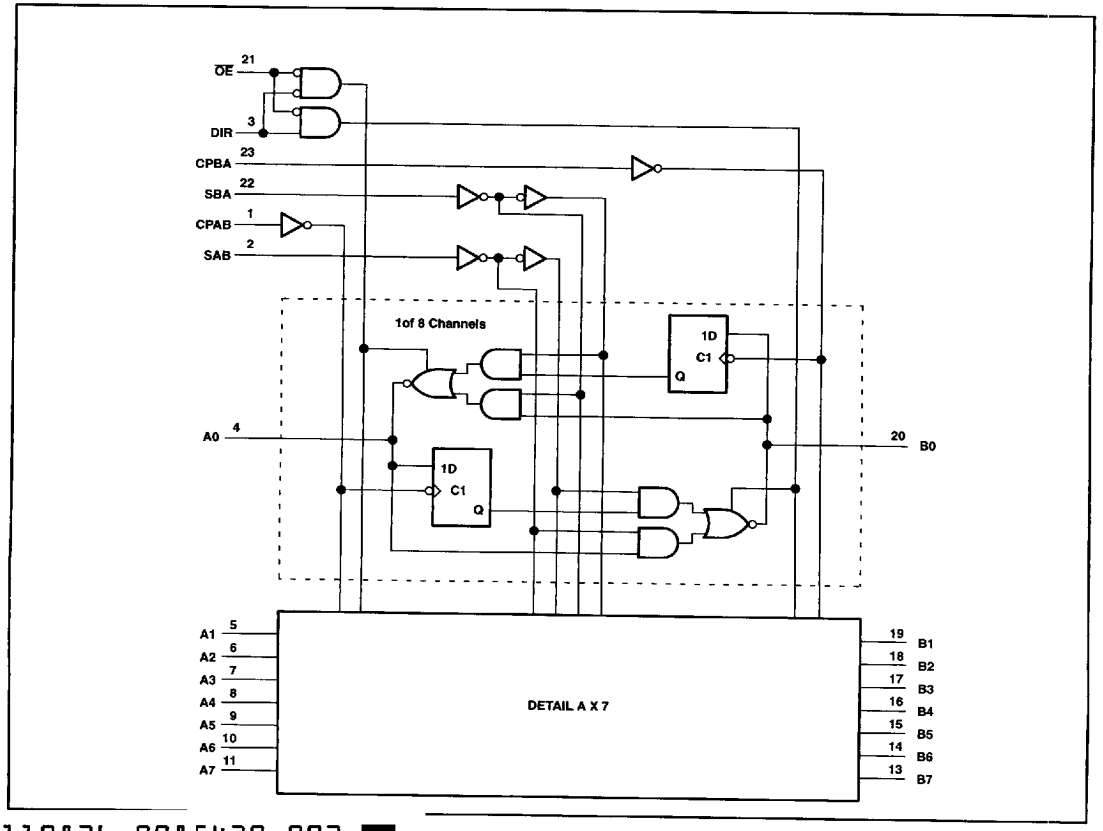
PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13	B0 – B7	Data inputs/outputs (B side)
21	$\overline{OE}$	Output enable input (active–Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	
X	X	↑	X	X	X	Input	Unspecified output*	Store A, B unspecified
X	X	X	↑	X	X	Unspecified output*	Input	Store B, A unspecified
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* The data output function may be enabled or disabled by various signals at the $\overline{OE}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low–to–High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	96	mA
T_{stg}	Storage temperature range		–65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High–level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High–level output current		–24	mA
I_{OL}	Low–level output current		48	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free–air temperature range	–55	+125	°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted: V_{CC} = MAX, $V_I = V_{IL}$ or V_{IH}, Tamb = –55 to +125°C

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2	V
V_{OH}	High–level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA	2.5	3.5		V
			V_{CC} = 4.5V; I_{OH} = –24mA	2.0	2.6		V
V_{OL}	Low–level output voltage		V_{CC} = 4.5V; I_{OL} = 48mA		0.42	0.55	V
I_I	Input leakage current	Control pins	V_I = GND or 5.5V		±0.01	±1.0	µA
		Data pins[6]	V_I = GND or 5.5V		±5	±100	µA
$I_{IH} + I_{OZH}$	3–State output High current		V_O = 2.7V; $V_I = V_{IL}$ or 3.0V		5.0	50	µA
$I_{IL} + I_{OZL}$	3–State output Low current		V_O = 0.5V; $V_I = V_{IL}$ or 3.0V		–5.0	–50	µA
I_O	Output current[4]		V_O = 2.5V; V_I = GND or V_{CC}	–50	–80	–180	mA
I_{CCH}	Quiescent supply current		Outputs High, V_I = GND or V_{CC}		50	250	µA
I_{CCL}			Outputs Low, V_I = GND or V_{CC}		20	30	mA
I_{CCZ}			Outputs 3–State; V_I = GND or V_{CC}		50	250	µA
ΔI_{CC}	Additional supply current per input pin[5]		V_{CC} = 5.5V; one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.3	1.5	mA

AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55 to +125°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	125	200		125[9]		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB to $\overline{B}n$ or CPBA to $\overline{A}n$	1	2.2 1.7	5.3 5.9	6.8 7.4	2.2 1.7	7.9 8.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}n$ to $\overline{B}n$ or $\overline{B}n$ to $\overline{A}n$	2, 3	1.0 1.5	3.6 4.2	5.1 5.6	1.0 1.5	6.9 6.3	ns
t_{PLH} t_{PHL}	Propagation delay SAB to $\overline{B}n$ or SBA to $\overline{A}n$	2, 3	1.5 1.5	4.6 5.4	6.1 6.9	1.5 1.5	7.4 7.7	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to $\overline{A}n$ or $\overline{B}n$	5 6	1.0 2.1	3.8 5.1	5.3 7.4	1.0 2.1	6.8 8.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to $\overline{A}n$ or $\overline{B}n$	5 6	1.5 1.5	6.2 5.7	7.3 7.0	1.5 1.5	8.3 7.6	ns
t_{PZH} t_{PZL}	Output enable time DIR to $\overline{A}n$ or $\overline{B}n$	5 6	1.2 2.5	4.2 5.5	5.7 9.0	1.2 2.5	7.1 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to $\overline{A}n$ or $\overline{B}n$	5 6	1.5 1.5	5.2 5.7	6.7 7.2	1.5 1.5	7.7 8.2	ns

AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5ns$, $C_L = 50pF$, $R_L = 500\Omega$

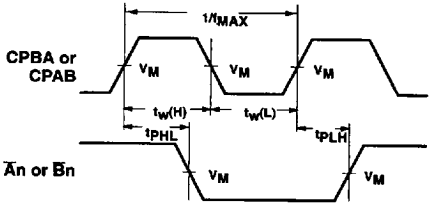
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -55 to +125°C, V_{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time $\overline{A}n$ to CPBA, $\overline{B}n$ to CPAB	4	3.0 3.0	1.5 1.0		3.0 3.0		ns
$t_h(H)$[7] $t_h(L)$[7]	Hold time $\overline{A}n$ to CPBA, $\overline{B}n$ to CPAB	4	0.0 0.0	−1.0 −1.0		0.0 0.0		ns
$t_w(H)$[8] $t_w(L)$[8]	Pulse width, High or Low CPAB or CPBA	1	3.5 4.0	2.0 2.9		3.5 4.0		ns

NOTES:

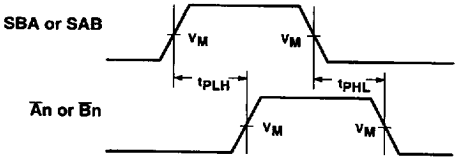
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
2. The performance capability of a high–performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
5. This is the increase in supply current for each input at 3.4V.
6. Input leakage on transceiver data pins also includes I_{OZH} or I_{OZL} current from the output circuitry.
7. T_{SET} and T_{HOLD} limits that are less than 3.0ns are guaranteed, but are only tested to a 3.0ns limit due to tester limitations.
8. T_W limits that are less than 6.0ns are guaranteed, but are only tested at a 6.0ns limit due to tester limitations.
9. Guaranteed by design, but not tested.

AC WAVEFORMS

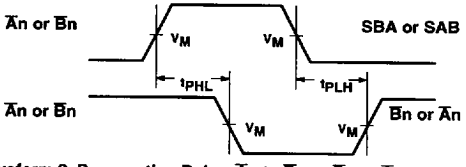
V_M = 1.5V, V_{IN} = GND to 3.0V



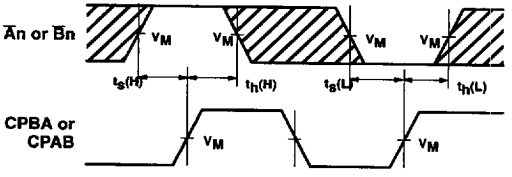
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



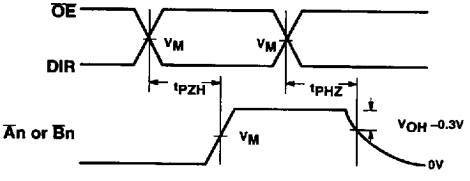
Waveform 2. Propagation Delay, SAB to Bn or SBA to An



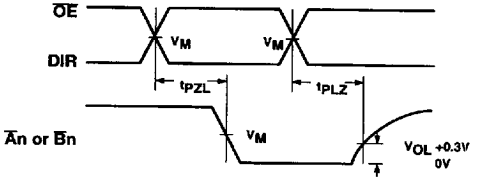
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA to An or SAB to Bn



Waveform 4. Data Setup and Hold Times



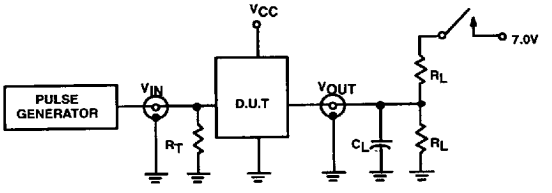
Waveform 5. 3–State Output Enable Time to High Level and Output Disable Time from High Level



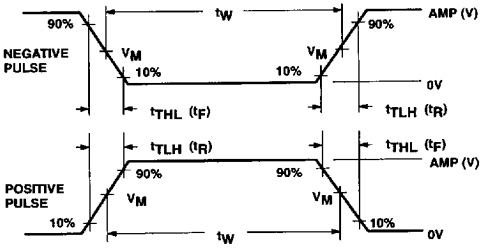
Waveform 6. 3–State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3–State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns