PRELIMINARY

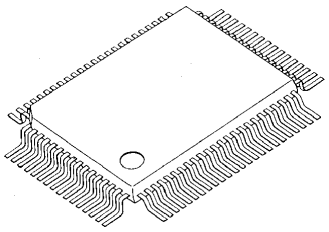
AV SWITCH

■GENERAL DESCRIPTION

The **NJW1310** is an Audio / Video switch for TV. All of functions are controlled by I²C BUS interface.

The **NJW1310** includes 7-input 2-output Audio switches. Also it includes 5-input 2-output Video switches, and 2-input 2-output YUV switches.

■ PACKAGE OUTLINE

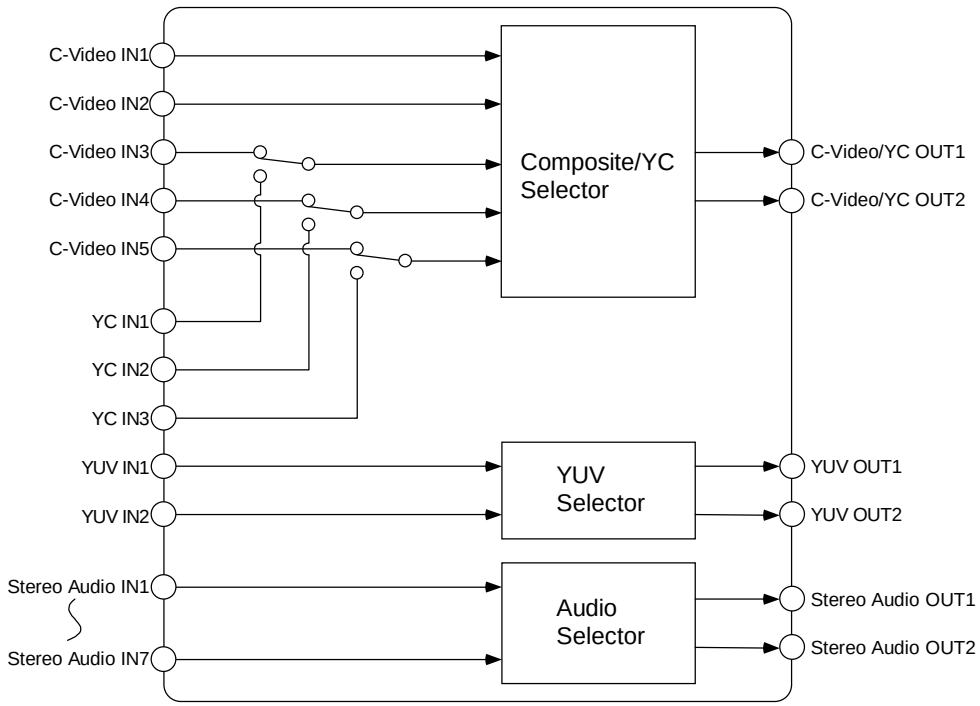


NJW1310FC2

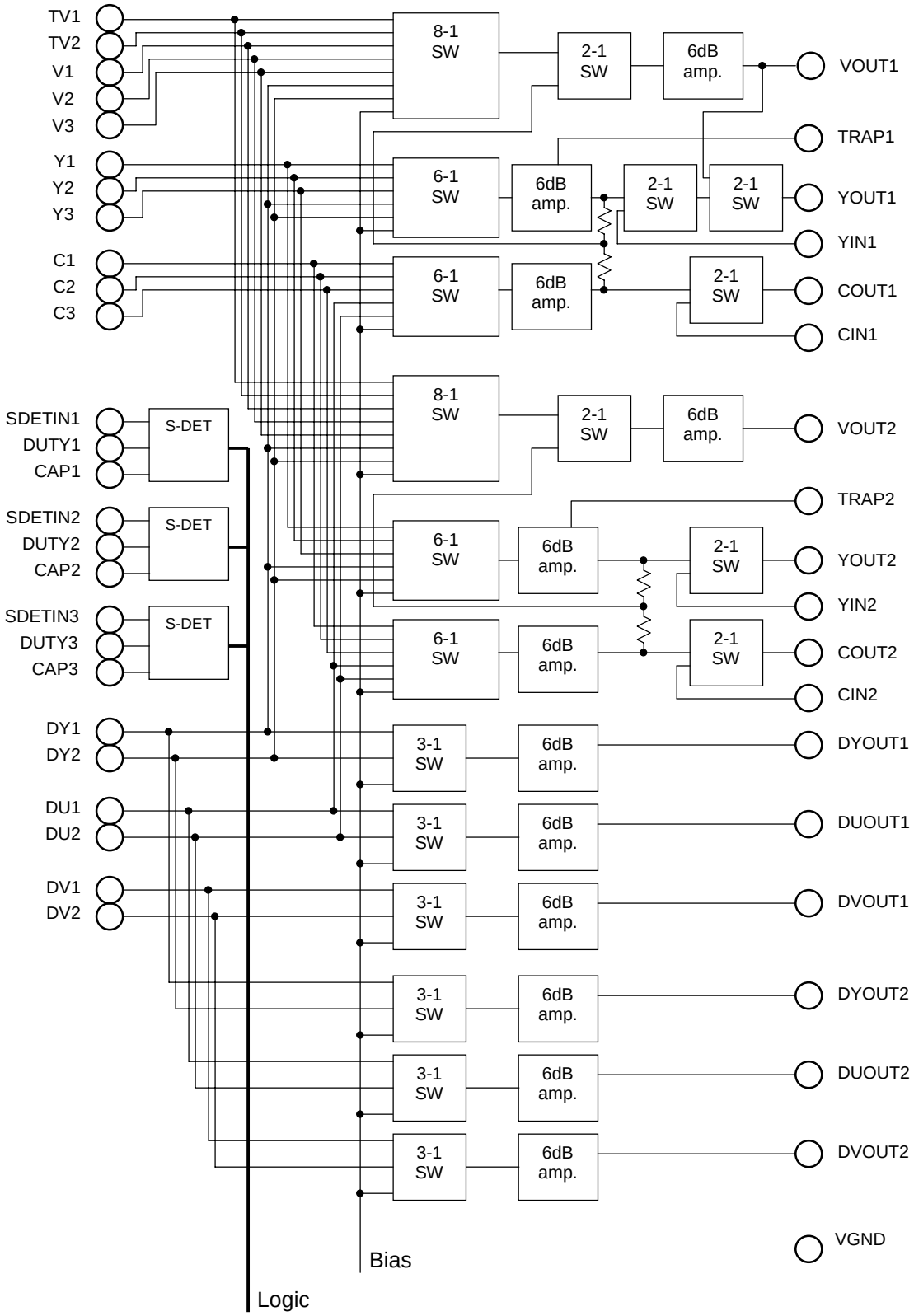
■FEATURES

- Operating Voltage 8 to 13V
- 7-Input 2-output Audio Switches
- 5-Input 2-output Video Switches
- 2-Input 2-output YUV Switches
- Y/C MIX Circuit
- S-Input Detection
- Wide Range Video Amplifier 20MHz, -3dB
- Audio Muting from External Pin
- Wide Range Audio Amplifier 3Vrms typ.
- Includes Auxiliary DC Outputs
- I²C BUS Interface
- Bi-CMOS Technology
- Package Outline QFP80

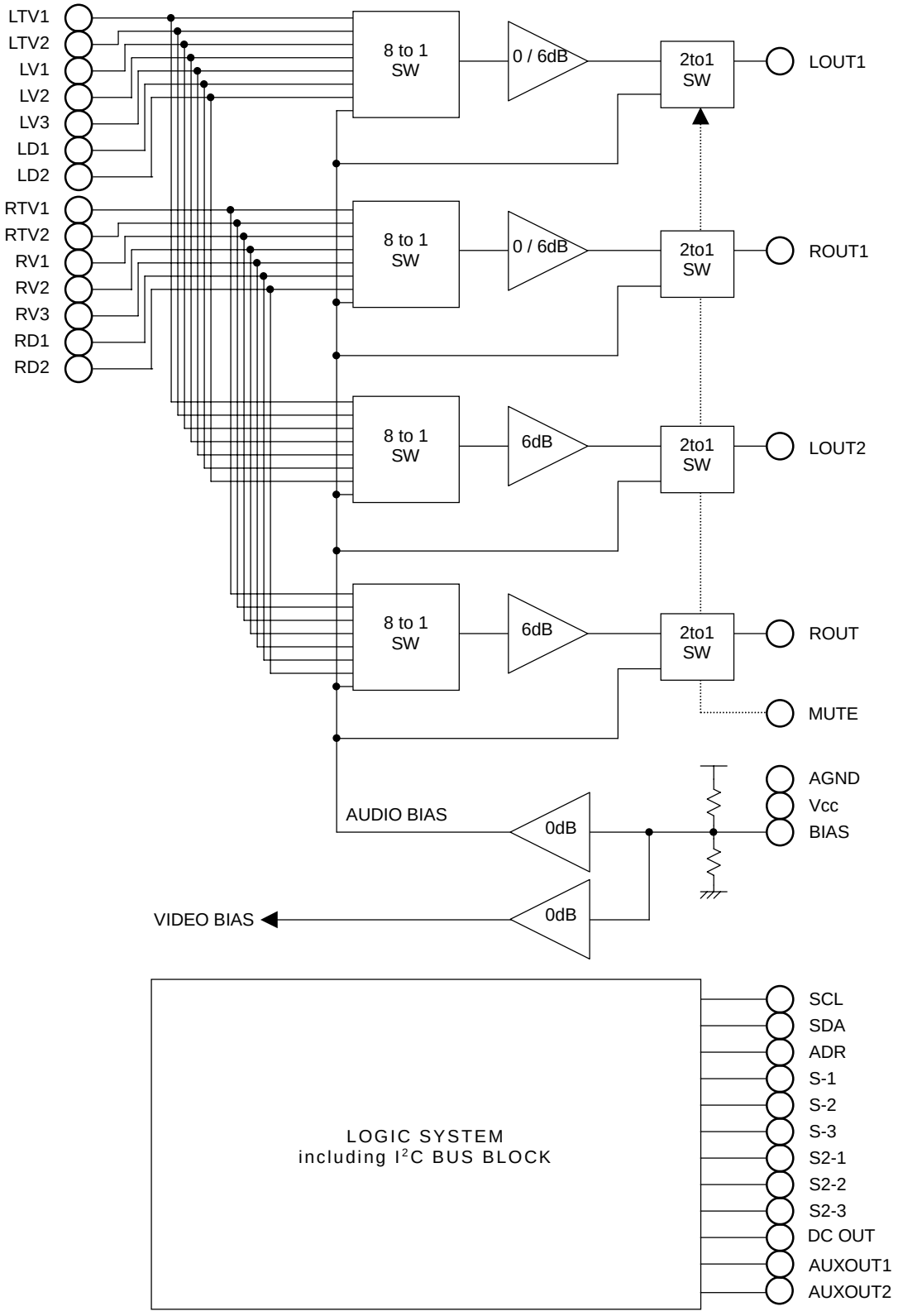
■FUNCTION BLOCK DIAGRAM



■BLOCK DIAGRAM (Video System)



■BLOCK DIAGRAM (Audio System, Logic System)



■**ABSOLUTE MAXIMUM RATING** (Ta=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V^+	15	V
Power Dissipation	P_D	1300	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +125	°C

■**ELECTRICAL CHARACTERISTICS** (Ta=25°C, V^+=9V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		8.0	9.0	13.0	V
Supply Current	I_{cc}	No Signal	56	80	104	mA
Reference Voltage	V_{REF}	No Signal	4.0	4.5	5.0	V

● **Video system**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gain	GV_V	f=100kHz, 0.3Vp-p input	5.9	6.4	6.9	dB
Frequency Response Characteristics	FBW_{V1}	f=100kHz, input frequency where output amplitude is -3dB with 0.3Vp-p output serving as 0dB	-	15	-	MHz
Frequency Response Characteristics (YUV)	FBW_{V2}		-	20	-	MHz
Input Dynamic Range	D_{dv}	f=100kHz, maximum with distortion < 1.0%	1.4	-	-	Vp-p
Cross Talk	V_{ctv}	f=4.43MHz, 1Vp-p input	-	-	-50	dB

● **Audio system**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gain	GV_A	f=1kHz, 1Vrms input, 5.7kΩ resistor inserted to input	-1	0	1	dB
Frequency Response Characteristics	FBW_A	f=1kHz, input frequency where output amplitude is -3dB with 1Vrms output serving as 0dB	50	-	-	kHz
Total Harmonic Distortion	THD	f=1kHz, 1Vrms input, where 400Hz HPF + 80kHz LPF are inserted	-	0.03	-	%
Input Dynamic Range	D_{dA}	f=1kHz, maximum with distortion < 0.3%	2.8	3.0	-	Vrms
Cross Talk	V_{ctv}	f=1kHz, 1Vrms input	-	-80	-	dB
Ripple Rejection Ratio	V_{rrA}	f=100Hz, 100mVrms applied to Vcc	-	-55	-40	dB
Output DC Offset	V_{off}	Offset voltage between input and output	-30	-	30	mV
Output Noise Voltage	V_{NO}	No signal JIS-A	-	20	-	uVrms

■**ELECTRICAL CHARACTERISTICS** (Ta=25°C, V^+=9V)

●**Audio system**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Mute Control Voltage	V_{muH}	Mute on	2.0	-	V^+	V
Low Level Mute Control Voltage	V_{muL}	Mute off	0	-	0.5	V

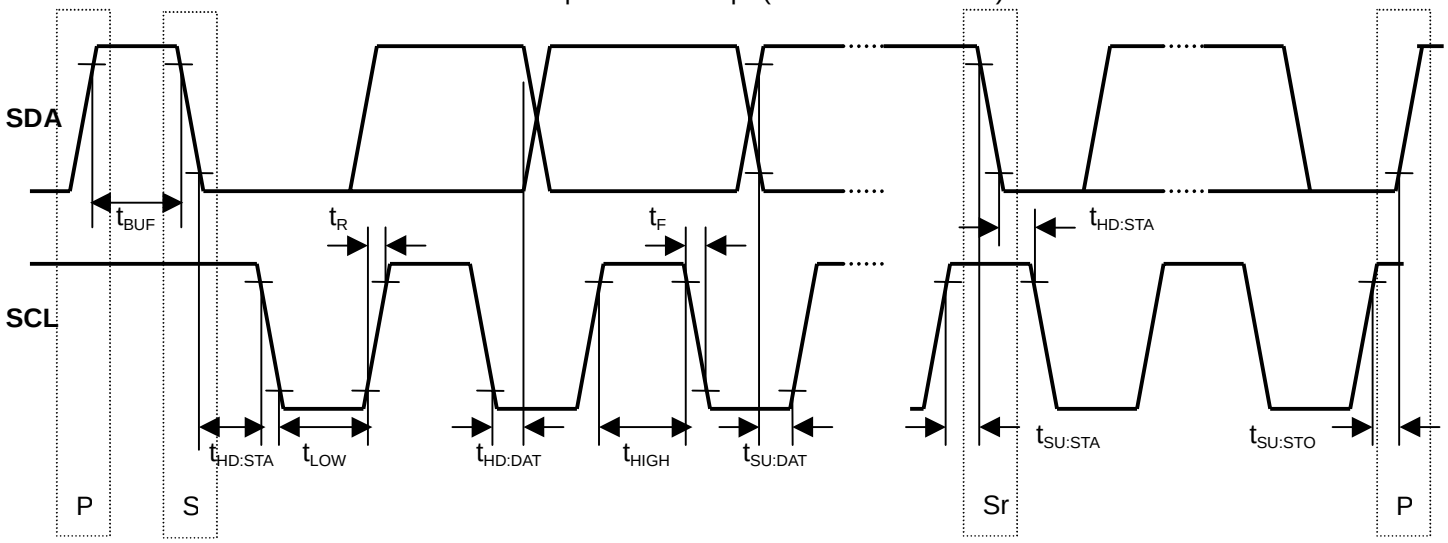
●**Logic system**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Auxiliary Output Voltage	V_{AUXH}	Isource=100uA	4.0	-	-	V
Low Level Auxiliary Output Voltage	V_{AUXL}	Isink=100uA	-	-	0.5	V

●I²C BUS (SDA, SCL)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
High Level Input Voltage	V_{IH}		3.0	-	5.0	V
Low Level Input Voltage	V_{IL}		0	-	1.5	V
Low Level Output Voltage	V_{OL}	With SDA 3mA current supplied	0	-	0.4	V
High Level Input Current	I_{IH}	V_{IH}=4.5V	0	-	10	uA
Low Level Input Current	I_{IL}	V_{IL}=0.4V	0	-	10	uA
Maximum Clock Frequency	f_{SCL}		0	-	100	kHz
Minimum Waiting Time for Data Change	t_{BUF}		4.7	-	-	us
Minimum Waiting Time for Data Transfer Start	$t_{HD:STA}$		4.0	-	-	us
Low Level Clock Pulse Width	t_{LOW}		4.7	-	-	us
High Level Clock Pulse Width	t_{HIGH}		4.0	-	-	us
Minimum Waiting Time for Start Preparation	$t_{SU:STA}$		4.7	-	-	us
Minimum Data Hold Time	$t_{HD:DAT}$		300	-	-	ns
Minimum Data Preparation Time	$t_{SU:DAT}$		250	-	-	ns
Rise Time	t_R		-	-	1	us
Fall Time	t_F		-	-	300	ns
Minimum Waiting Time for Stop Preparation	$t_{SU:STO}$		4.7	-	-	us

I2C BUS Load Condition:Pull up resistance 4kΩ(Connected to +5V)
Load Capacitance 200pF(Connected to GND)



■DESCRIPTION OF I²C BUS INTERFACE

The **NJW1310** has two function mode with I²C BUS interface, receive mode and transmit mode. And the **NJW 1310** can use two slave addresses, so it's possible to control two **NJW1310** with one Master.

●SLAVE ADDRESSES

	MSB							LSB
S	SLAVE ADDRESS							
	1	0	0	1	0	0	ADR	R/W

★Two Slave Addresses are available by to set the Bit ADR to either "0", or "1".

●RECEIVE MODE

◆CONSTRUCT OF CONTROL REGISTER

	MSB							LSB		MSB							LSB	
S	SLAVE ADDRESS								ACK	DATA1								ACK
	1	0	0	1	0	0	ADR	0		b7	b6	b5	b4	b3	b2	b1	b0	
	MSB							LSB		MSB							LSB	
	DATA2								ACK	DATA3								ACK P
	b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0	

★Bit R/W must be "0", to function the **NJW1310** with receive mode.
★Bit ADR specify the slave address. ADR 0 : 90H
1 : 92H

◆INVALID DATA PROCESSING

1) Different slave address.

	MSB			LSB		MSB			LSB	
S	SLAVE ADDRESS			$\overline{ACK}$		DATA1			$\overline{ACK}$	
	MSB			LSB		MSB			LSB	
	DATA2			$\overline{ACK}$		DATA3			$\overline{ACK}$	P

When the **NJW1310** receives a different slave address, no acknowledgement from the **NJW1310** is replied.

2) Incomplete data format

	MSB			LSB		MSB			LSB	
S	SLAVE ADDRESS			ACK		DATA1			ACK	P

As an example, if the **NJW1310** receives only 1st data, the **NJW1310** ignores the 1st data.

3) Too long data format

	MSB			LSB		MSB			LSB	
S	SLAVE ADDRESS			ACK		DATA1			ACK	
	MSB			LSB		MSB			LSB	
	DATA2			ACK		DATA3			ACK	
	MSB			LSB						
	DATA4			$\overline{ACK}$	P					

As an example, if the **NJW1310** receives 4th data, the **NJW1310** ignores the 4th data.
In addition, no acknowledgement after 4th data is replied.

◆CONSTRUCT OF DATA1 TO DATA3

	MSB b7	b6	b5	b4	b3	b2	b1	LSB b0
DATA1	S/COMP1	V-OUTPUT1			A-OUTPUT1			VMODE
DATA2	S/COMP2	V-OUTPUT2			A-OUTPUT2			A-GAIN
DATA3	V-OUTPUT3		V-OUTPUT4		AUX1	AUX2	S2OUT	

All resisters are reset to “0” when power on.

◆DETAILS OF EACH BIT

< V-OUTPUT1, VOUTPUT2 >

These Bit specify the input line which are sent to the port VOUT1, YOUT1, COUT1, VOUT2, YOUT2, and COUT2.

V-OUTPUT1			VOUT1, YOUT1, COUT1
V-OUTPUT2			VOUT2, YOUT2, COUT2
b6	b5	b4	selected input line
0	0	0	MUTE
0	0	1	TV1
0	1	0	TV2
0	1	1	V1, Y1/C1
1	0	0	V2, Y2/C2
1	0	1	V3, Y3/C3
1	1	0	DY1
1	1	1	DY2

< S/COMP1, S/COMP2 >

These Bit specify the types of the input signals which are sent to the port VOUT1, YOUT1, COUT1, VOUT2, YOUT2, and COUT2.

S/COMP1	VOUT1, YOUT1, COUT1
S/COMP2	VOUT2, YOUT2, COUT2
b7	selected type
0	Composite
1	S input

★Normally, the fixing of Video output signals needs the selection of both the input signal line and the types of the input signal.

< VMODE >

These Bit specify the types of the VOUT1 signals which are sent to the port YOUT1,

VOUT1	YOUT1
b0	selected type
0	S input
1	VOUT1

< V-OUTPUT3, V-OUTPUT4 >

These Bit specify the input line which are sent to the port DYOUT1, DUOUT1, DVOUT1, DYOUT2, DUOUT2, and DVOUT2.

V-OUTPUT3	b7	b6	DYOUT1, DUOUT1, DVOUT1
V-OUTPUT4	b5	b4	DYOUT2, DUOUT2, DVOUT2
			selected input line
	0	0	MUTE
	0	1	DY1, DU1, DV1
	1	0	DY2, DU2, DV2
	1	1	Reserved

< A-OUTPUT1, A-OUTPUT2 >

These Bit specify the input line which are sent to the port LOUT1, ROUT1,LOUT2, and ROUT2.

A-OUTPUT1			LOUT1, ROUT1
A-OUTPUT2			LOUT2, ROUT2
b3	b2	b1	selected input line
0	0	0	MUTE
0	0	1	LTV1, RTV1
0	1	0	LTV2, RTV2
0	1	1	LV1, RV1
1	0	0	LV2, RV2
1	0	1	LV3, RV3
1	1	0	LD1, RD1
1	1	1	LD2, RD2

★In each Audio output signals, both L ch. and R ch. are changed at the same time.

< A-GAIN >

This Bit specify the output gain of the port LOUT1, ROUT1.

A-GAIN	LOUT1, ROUT1
b0	output gain
0	+6dB
1	0dB

< AUX1, AUX2 >

These Bit specify the output DC voltage of port AUXOUT1, and AUXOUT2.

AUX1	b3	AUXOUT1
AUX2	b2	AUXOUT2
		output DC voltage
	0	Low
	1	High

< S2OUT >
These Bit specify the output DC voltage of port DCOUT.

S2OUT		DCOUT
b1	b0	output DC voltage
0	0	4.2V
0	1	1.9V
1	0	0V
1	1	4.2V

●TRANSMIT MODE

◆CONSTRUCT OF CONTROL REGISTER

	MSB							LSB		MSB							LSB	
S	SLAVE ADDRESS								ACK	DATA1								ACK
	1	0	0	1	0	0	ADR	1		b7	b6	b5	b4	b3	b2	b1	b0	

	MSB							LSB		
	DATA2								ACK	P
	b7	b6	b5	b4	b3	b2	b1	b0		

★Bit R/W must be “1”, to function the **NJW1310** with transmit mode.

★Bit ADR specify the slave address. ADR 0 : 91H

1 : 93H

◆CONSTRUCT OF DATA1 TO DATA2

	MSB b7	b6	b5	b4	b3	b2	b1	LSB b0
DATA1	S-1	S-2	S-3	0	S-DET1	S-DET2	S-DET3	0
DATA2	S2-1		S2-2		S2-3		0	0

0 : means Low level output

All resisters are reset to “0” when power on.

◆DETAILS OF EACH BIT

< S-1, S-2, S-3 >

These Bit show the input DC voltage level of port S-1, S-2, and S-3.

S-1	b7	S-1
S-2	b6	S-2
S-3	b5	S-3
		DC voltage level
	0	DC > 3.5V
	1	DC < 3.5V

< S-DET1, S-DET2, S-DET3 >

These Bit show the existence of the input signals of port S-DETIN1,S-DETIN2, and S-DETIN3.

S-DET1	b3	S-DETIN1
S-DET2	b2	S-DETIN2
S-DET3	b1	S-DETIN3
		existence of signals
	0	none
	1	exist

< S2-1, S2-2, S2-3 >

These Bit show the input DC voltage level of port S2-1, S2-2, and S2-3.

S2-1	b7	b6	S2-1
S2-2	b5	b4	S2-2
S2-3	b3	b2	S2-3
			DC voltage level
	0	0	DC < 1.3V
	0	1	1.3V < DC < 2.5V
	1	1	DC > 2.5V
	0	0	ports are open

●SWITCH CONTROL TABLE

■ V-OUTPUT1

DATA1									Output Signal				
Hex	b7	b6	b5	b4	b3	b2	b1	b0	VOUT1	YOUT1	COUT1	LOUT1	ROUT1
	S/COMP1	V-OUTPUT1			A-OUTPUT1			VMODE					
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE
12H	0	0	0	1	0	0	1	0	TV1	YIN1	CIN1	LTV1	RTV1
24H	0	0	1	0	0	1	0	0	TV2	YIN1	CIN1	LTV2	RTV2
36H	0	0	1	1	0	1	1	0	V1	YIN1	CIN1	LV1	RV1
48H	0	1	0	0	1	0	0	0	V2	YIN1	CIN1	LV2	RV2
5AH	0	1	0	1	1	0	1	0	V3	YIN1	CIN1	LV3	RV3
6CH	0	1	1	0	1	1	0	0	DY1	YIN1	CIN1	LD1	RD1
7EH	0	1	1	1	1	1	1	0	DY2	YIN1	CIN1	LD2	RD2
80H	1	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE
92H	1	0	0	1	0	0	1	0	MUTE	MUTE	MUTE	LTV1	RTV1
A4H	1	0	1	0	0	1	0	0	MUTE	MUTE	MUTE	LTV2	RTV2
B6H	1	0	1	1	0	1	1	0	Y1/C1 MIX	Y1	C1	LV1	RV1
C8H	1	1	0	0	1	0	0	0	Y2/C2 MIX	Y2	C2	LV2	RV2
DAH	1	1	0	1	1	0	1	0	Y3/C3 MIX	Y3	C3	LV3	RV3
ECH	1	1	1	0	1	1	0	0	DY1/DU1 MIX	DY1	DU1	LD1	RD1
FEH	1	1	1	1	1	1	1	0	DY2/DU2 MIX	DY2	DU2	LD2	RD2
01H	0	0	0	0	0	0	0	1	MUTE	MUTE	MUTE	MUTE	MUTE
13H	0	0	0	1	0	0	1	1	TV1	TV1	CIN1	LTV1	RTV1
25H	0	0	1	0	0	1	0	1	TV2	TV2	CIN1	LTV2	RTV2
37H	0	0	1	1	0	1	1	1	V1	V1	CIN1	LV1	RV1
49H	0	1	0	0	1	0	0	1	V2	V2	CIN1	LV2	RV2
5BH	0	1	0	1	1	0	1	1	V3	V3	CIN1	LV3	RV3
6DH	0	1	1	0	1	1	0	1	DY1	DY1	CIN1	LD1	RD1
7FH	0	1	1	1	1	1	1	1	DY2	DY2	CIN1	LD2	RD2
81H	1	0	0	0	0	0	0	1	MUTE	MUTE	MUTE	MUTE	MUTE
93H	1	0	0	1	0	0	1	1	MUTE	MUTE	MUTE	LTV1	RTV1
A5H	1	0	1	0	0	1	0	1	MUTE	MUTE	MUTE	LTV2	RTV2
B7H	1	0	1	1	0	1	1	1	Y1/C1 MIX	Y1/C1 MIX	C1	LV1	RV1
C9H	1	1	0	0	1	0	0	1	Y2/C2 MIX	Y2/C2 MIX	C2	LV2	RV2
DBH	1	1	0	1	1	0	1	1	Y3/C3 MIX	Y3/C3 MIX	C3	LV3	RV3
EDH	1	1	1	0	1	1	0	1	DY1/DU1 MIX	DY1/DU1 MIX	DU1	LD1	RD1
FFH	1	1	1	1	1	1	1	1	DY2/DU2 MIX	DY2/DU2 MIX	DU2	LD2	RD2

■ A-OUTPUT1*

DATA1									Output Signal				
Hex	b7	b6	b5	b4	b3	b2	b1	b0	VOUT1	YOUT1	COUT1	LOUT1	ROUT1
	S/COMP1	V-OUTPUT1			A-OUTPUT1			VMODE					
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE
12H	0	0	0	1	0	0	1	0	TV1	YIN1	CIN1	LTV1	RTV1
24H	0	0	1	0	0	1	0	0	TV2	YIN1	CIN1	LTV2	RTV2
36H	0	0	1	1	0	1	1	0	V1	YIN1	CIN1	LV1	RV1
48H	0	1	0	0	1	0	0	0	V2	YIN1	CIN1	LV2	RV2
5AH	0	1	0	1	1	0	1	0	V3	YIN1	CIN1	LV3	RV3
6CH	0	1	1	0	1	1	0	0	DY1	YIN1	CIN1	LD1	RD1
7EH	0	1	1	1	1	1	1	0	DY2	YIN1	CIN1	LD2	RD2

■ V-OUTPUT2

DATA2									Output Signal					
Hex	b7	b6	b5	b4	b3	b2	b1	b0	VOUT2	YOUT2	COUT2	LOUT2	ROUT2	LOUT1, ROUT1 GAIN
	S/COMP2	V-OUTPUT2			A-OUTPUT2			A-GAIN						
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	6dB
12H	0	0	0	1	0	0	1	0	TV1	YIN2	CIN2	LTV1	RTV1	6dB
24H	0	0	1	0	0	1	0	0	TV2	YIN2	CIN2	LTV2	RTV2	6dB
36H	0	0	1	1	0	1	1	0	V1	YIN2	CIN2	LV1	RV1	6dB
48H	0	1	0	0	1	0	0	0	V2	YIN2	CIN2	LV2	RV2	6dB
5AH	0	1	0	1	1	0	1	0	V3	YIN2	CIN2	LV3	RV3	6dB
6CH	0	1	1	0	1	1	0	0	DY1	YIN2	CIN2	LD1	RD1	6dB
7EH	0	1	1	1	1	1	1	0	DY2	YIN2	CIN2	LD2	RD2	6dB
81H	1	0	0	0	0	0	0	1	MUTE	MUTE	MUTE	MUTE	MUTE	(0dB)
93H	1	0	0	1	0	0	1	1	MUTE	MUTE	MUTE	LTV1	RTV1	0dB
A5H	1	0	1	0	0	1	0	1	MUTE	MUTE	MUTE	LTV2	RTV2	0dB
B7H	1	0	1	1	0	1	1	1	Y1/C1 MIX	Y1	C1	LV1	RV1	0dB
C9H	1	1	0	0	1	0	0	1	Y2/C2 MIX	Y2	C2	LV2	RV2	0dB
DBH	1	1	0	1	1	0	1	1	Y3/C3 MIX	Y3	C3	LV3	RV3	0dB
EDH	1	1	1	0	1	1	0	1	DY1/DU1 MIX	DY1	DU1	LD1	RD1	0dB
FFH	1	1	1	1	1	1	1	1	DY2/DU2 MIX	DY2	DU2	LD2	RD2	0dB

■ A-OUTPUT2

DATA2									Output Signal					
Hex	b7	b6	b5	b4	b3	b2	b1	b0	VOUT2	YOUT2	COUT2	LOUT2	ROUT2	LOUT1, ROUT1 GAIN
	S/COMP2	V-OUTPUT2			A-OUTPUT2			A-GAIN						
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	6dB
12H	0	0	0	1	0	0	1	0	TV1	YIN2	CIN2	LTV1	RTV1	6dB
24H	0	0	1	0	0	1	0	0	TV2	YIN2	CIN2	LTV2	RTV2	6dB
36H	0	0	1	1	0	1	1	0	V1	YIN2	CIN2	LV1	RV1	6dB
48H	0	1	0	0	1	0	0	0	V2	YIN2	CIN2	LV2	RV2	6dB
5AH	0	1	0	1	1	0	1	0	V3	YIN2	CIN2	LV3	RV3	6dB
6CH	0	1	1	0	1	1	0	0	DY1	YIN2	CIN2	LD1	RD1	6dB
7EH	0	1	1	1	1	1	1	0	DY2	YIN2	CIN2	LD2	RD2	6dB

■ A-GAIN

DATA2									Output Signal					
Hex	b7	b6	b5	b4	b3	b2	b1	b0	VOUT2	YOUT2	COUT2	LOUT2	ROUT2	LOUT1, ROUT1 GAIN
	S/COMP2	V-OUTPUT2			A-OUTPUT2			A-GAIN						
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	6dB
FFH	1	1	1	1	1	1	1	1	DY2/DU2 MIX	DY2	DU2	LD2	RD2	0dB

■ V-OUTPUT3

DATA3									Output Signal								
Hex	b7	b6	b5	b4	b3	b2	b1	b0	DVOUT1	DUOUT1	DVOUT1	DVOUT2	DUOUT2	DVOUT2	AUXOUT1	AUXOUT2	DCOUT
	V-OUTPUT3		V-OUTPUT4		AUX1	AUX2	S2OUT										
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9
40H	0	1	0	0	0	0	0	0	DY1	DU1	DV1	MUTE	MUTE	MUTE	Low	Low	16vs9
80H	1	0	0	0	0	0	0	0	DY2	DU2	DV2	MUTE	MUTE	MUTE	Low	Low	16vs9
C0H	1	1	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9

■ V-OUTPUT4

DATA3									Output Signal								
Hex	b7	b6	b5	b4	b3	b2	b1	b0	DVOUT1	DUOUT1	DVOUT1	DVOUT2	DUOUT2	DVOUT2	AUXOUT1	AUXOUT2	DCOUT
	V-OUTPUT3		V-OUTPUT4		AUX1	AUX2	S2OUT										
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9
10H	0	0	0	1	0	0	0	0	MUTE	MUTE	MUTE	DY1	DU1	DV1	Low	Low	16vs9
20H	0	0	1	0	0	0	0	0	MUTE	MUTE	MUTE	DY2	DU2	DV2	Low	Low	16vs9
30H	0	0	1	1	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9

■ AUXOUT1

DATA3									Output Signal								
Hex	b7	b6	b5	b4	b3	b2	b1	b0	DVOUT1	DUOUT1	DVOUT1	DVOUT2	DUOUT2	DVOUT2	AUXOUT1	AUXOUT2	DCOUT
	V-OUTPUT3		V-OUTPUT4		AUX1	AUX2	S2OUT										
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9
08H	0	0	0	0	1	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	High	Low	16vs9

■ AUXOUT2

DATA3									Output Signal								
Hex	b7	b6	b5	b4	b3	b2	b1	b0	DVOUT1	DUOUT1	DVOUT1	DVOUT2	DUOUT2	DVOUT2	AUXOUT1	AUXOUT2	DCOUT
	V-OUTPUT3		V-OUTPUT4		AUX1	AUX2	S2OUT										
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9
04H	0	0	0	0	0	1	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	High	16vs9

■ S2OUT

DATA3									Output Signal								
Hex	b7	b6	b5	b4	b3	b2	b1	b0	DVOUT1	DUOUT1	DVOUT1	DVOUT2	DUOUT2	DVOUT2	AUXOUT1	AUXOUT2	DCOUT
	V-OUTPUT3		V-OUTPUT4		AUX1	AUX2	S2OUT										
00H	0	0	0	0	0	0	0	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9
01H	0	0	0	0	0	0	0	1	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	4vs3
02H	0	0	0	0	0	0	1	0	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	Letter
03H	0	0	0	0	0	0	1	1	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	Low	Low	16vs9

■Note

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