EEPROM

AVAILABLE AS MILITARY SPECIFICATIONS

•MIL-STD-883

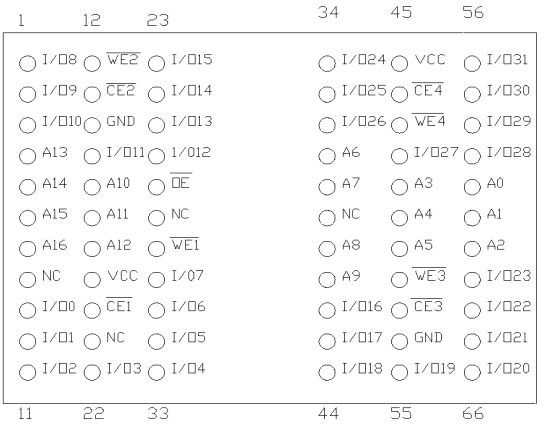
FEATURES

- Access times of 120, 150, 200 ns
- Built in decoupling caps for low noise operation
- Organized as 128K x32; User configurable as 256K x16 or 512K x8
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs

OPTIONS MARKINGS

- Timing
  - 120ns access -12
  - 150ns access -15
  - 200ns access -20
- Packaging
  - 66 lead Pin Grid Array P No. 801

PIN ASSIGNMENT (Top View)
66 Lead PGA

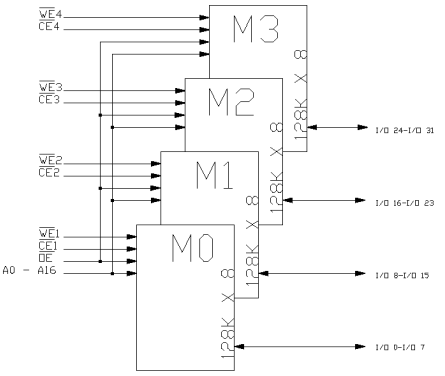


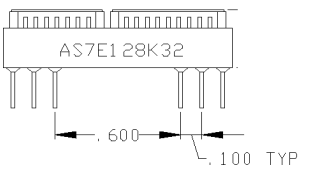
GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS7E128K32 is a 4 Megabit CMOS EEPROM Module organized as 128K32-bits and user configurable to 256K x16 or 512Kx 8. Built with AT28C010 components, the AS7E128K32P can be provided to Full 883 compliance. The module achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

The military grade product is manufactured in compliance with the latest revision of MIL-STD 883, making the AS7E128K32 ideally suited for military or space applications.

The AS7E128K32 module is constructed using a 1.075 sq inch ceramic pin grid array substrate. This compact layout reduces space requirements for board assembly to a minimum.





DEVICE OPERATION:

The AS7E128K32 is an electricaly erasable and programmable memory module that is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte-page register to allow writing of up to 128 bytes of data simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

READ:

The AS7E128K32 is accessed like a Static RAM. When CE and OE are low and WE is High, the data stored at the memory location determined by the address pins is asserted on the outputs. The module can be read as a 32 bit, 16 bit or 8 bit device. The outputs are put in the high impedance state when either CE or OE is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE:

A low pulse on the WE or CE input with CE or WE low (respectively) and OE high initiates a write cycle. The address is latched on the falling edge of CE or WE, whichever occurs last. The data is latched by the first rising edge of CE or WE. Once a BWDW (byte, word or double word) write has been started it will automatically time itself to completion.

PAGE WRITE:

The page write operation of the AS7E128K32 allows 1 to 128 BWDWs of data to be written into the device during a single internal programming period. Each new BWDW must be written within 15-us (tBLC) of the previous BWDW. If the tBLC limit is exceeded the AS7E128K32 will cease accepting data and commence the internal programming operation. For each WE high to low transition during the page write operation, A7-A16 must be the same.

The A0-A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING:

he AS7E128K32 features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at anytime during the write cycle.

TOGGLE BIT:

In addition to DATA Polling the AS7E128K32 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION:

If precautions are not taken, inadvertent writes may occur during transitions of the host power supply. The E^2 module has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION:

Hardware features protect against inadvertent writes to the AS7E128K32 in the following ways: (a) VCC sense - if VCC is below 3.8 V (typical) the write function is inhibited; (b) VCC power-on delay - once VCC has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of OE low, CE high or WE high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the WE or CE inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION:

A software controlled data protection feature has been implemented on theAS7E128K32. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user and is shipped with SDP disabled, SDP is enabled by the host system issuing a series of thre e write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after tWC the entire AS7E128K32 will be protected from inadvertent write operations. It should be noted, that once protected the host may still perform a byte of page write to the AS7E128K32. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP. Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AS7E128K32 during power-up and Power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte of page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of tWC, read operations will effectively be polling operations.

CAPACITANCE TABLE

V_{IN} = 0V, f = 1MHz, TA =25ºC

Symbol	Parameter	Maximum	Units	Notes
C_{ADD}	A0-A16 Capactiance	40	pF	4, 14
C_{OE}	OE\ Capactiance	40	pF	4, 14
C_{WE}, C_{CE}	WE\ and CE\ Capactiance	10	pF	4, 14
C_{IO}	I/O 0 - I/O 31 Capactiance	12	pF	4, 14

OPERATING MODE

MODE	CE	OE	WE	I/O
Read	V_{IL}	V_{IH}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

DC OPERATING CONDITIONS

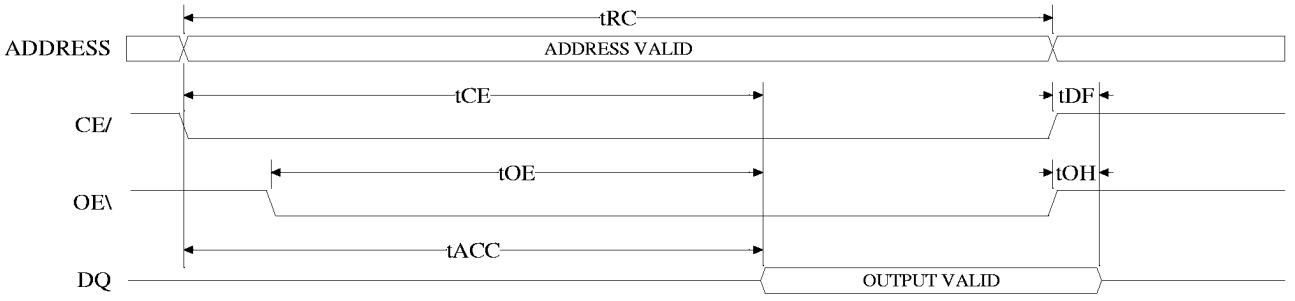
Symbol	Parameter	Condition	Min	Max	Units
ILI	Input Load Current	VIN=0V to VCC+1V		43	uA
ILO	Output Leakage Current	VI/O=0VtoVCC		43	uA
ISB1	VCC Standby Current CMOS	CE=VCC-0.3V to VCC+1		1.3	mA
ISB2	VCC Standby Current TTL	CE=2.0V to VCC+1		13	mA
ICC	VCC Active Current	f=5MHz; IOUT=0mA		340	mA
VIL	Input Low Voltage			0.8	V
VIH	Input High Voltage		2		V
VOL	Output Low Voltage	IOL=2.1mA		0.45	V
VOH1	Output High Voltage	IOH=-400uA	2.4		V
VOH2	Output High Voltage CMOS	IOH=-100uA; VCC=4.5V	4.2		V

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

		120		150		200		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Units
tACC	Address to Output Delay		120		150		200	ns
tCE (1)	CE\ to Output Delay		120		150		200	ns
tOE (2)	OE\ to Output Delay	0	50	0	55	0	55	ns
tDF (3,4)	CE\ or OE\ to Output Float	0	50	0	55	0	55	ns
tOH	Output Hold from OE\, CE\ or Address, whichever occurs first	0		0		0		ns

A.C. Read Waveforms(1,2,3,4)



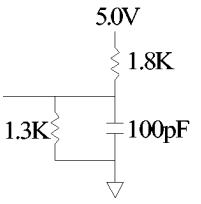
Notes:

1. CE may be delayed to t_{ACC}-t_{CE} after the address transition without inpact on t_{ACC}.
2. OE may be delayed to t_{CE}-t_{OE} after the falling edge of CE without inpact on t_{CE} or by t_{ACC}-t_{OE} after an address change without inpact on t_{ACC}.
3. t_{DF} is specified from OE or CE whichever occurs first (C_L = 5pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement level AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5nS
Input and Output Timing Reference Levels	1.5V

Output Test Load

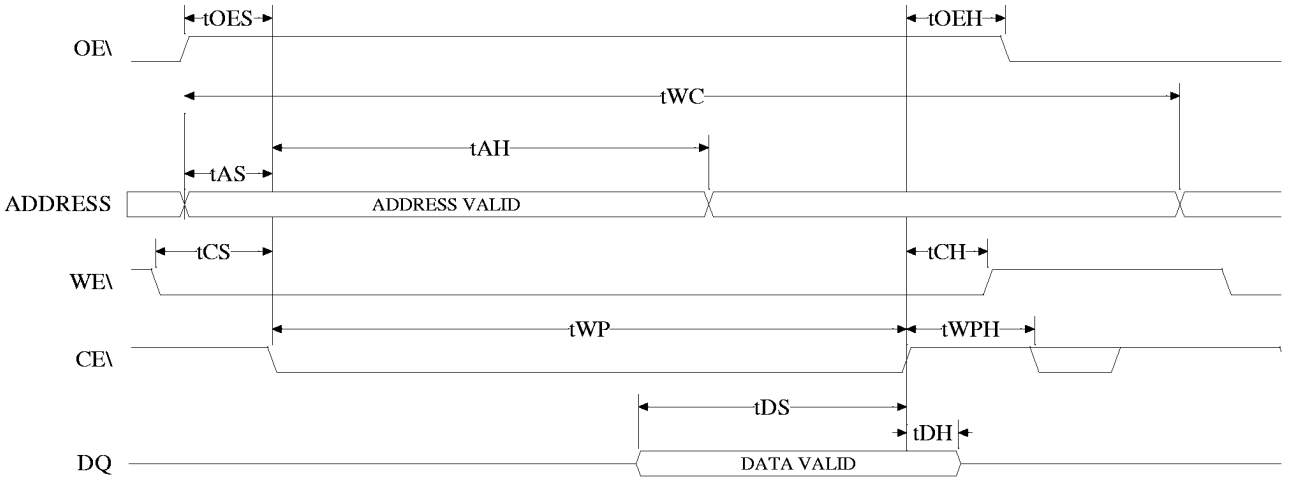


AC WRITE CHARACTERISTICS

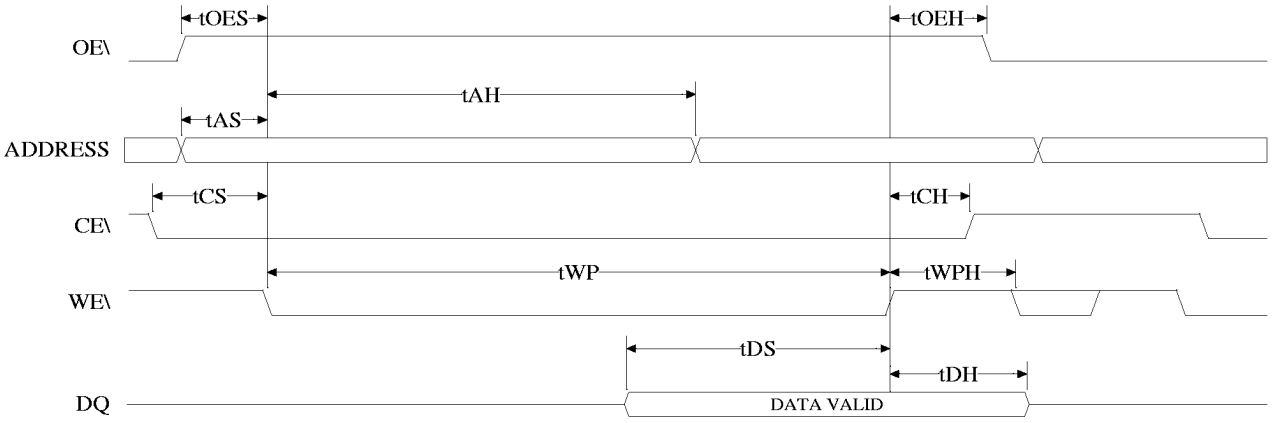
(-55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

Symbol	Parameter	Min	Max	Unit
t_{AS}, t_{OES}	Address, OE\ Set-Up time	0		ns
t_{AH}	Address, Hold time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (WE\ or CE\)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, OE\ Hold Time	0		ns

WRITE CYCLE NO 1.
(Chip Enable Controlled)



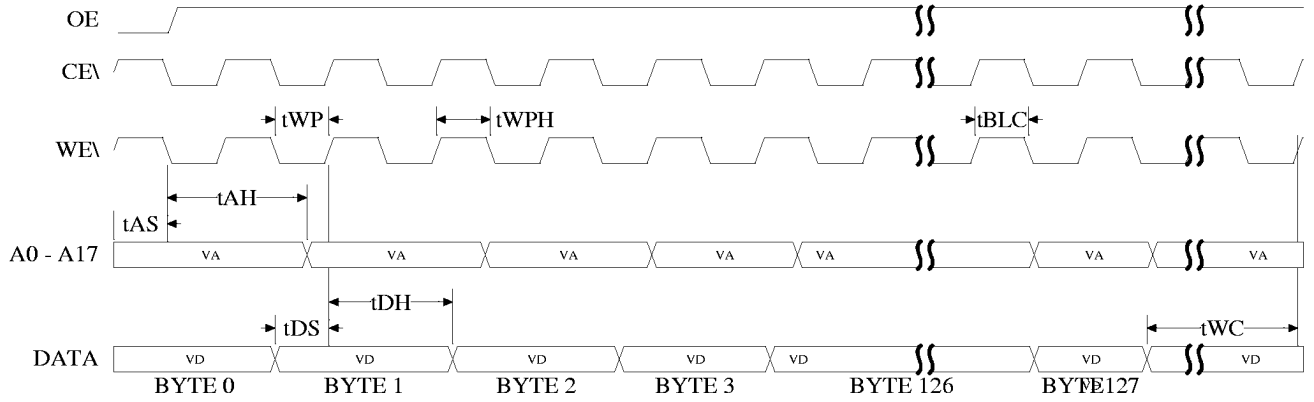
WRITE CYCLE NO 2.
(Chip Enable Controlled)



Page Mode Characteristics

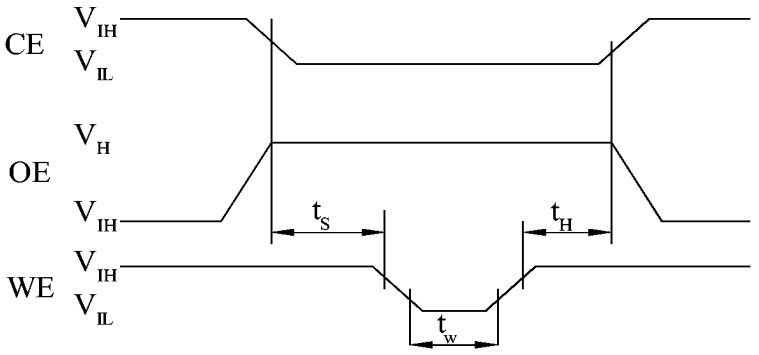
Symbol	Parameter	Min	Max	Units
tWC	Write Cycle Time		10	ms
tAS	Address Set-up time	0		ns
tAH	Address Hold Time	50		ns
tDS	Data Set-up Time	50		ns
tDH	Data Hold Time	0		ns
tWP	Write Pulse Width	100		ns
tBLC	Byte Load Cycle Time		150	us
tWPH	Write Pulse Width High	50		ns

Page Mode Write Waveforms(1,2)



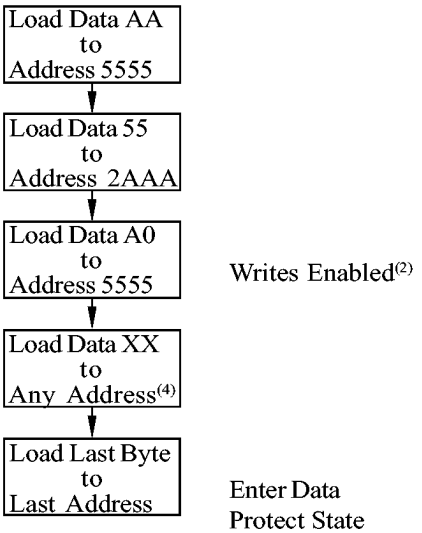
Notes:
1. A7 through A16 must specify the page address during each high to low transition of WE (or CE).
2. OE must be high only when WE and CE are both low.
3. VD - Valid Data
4. VA - Valid Address

Chip Erase Waveforms

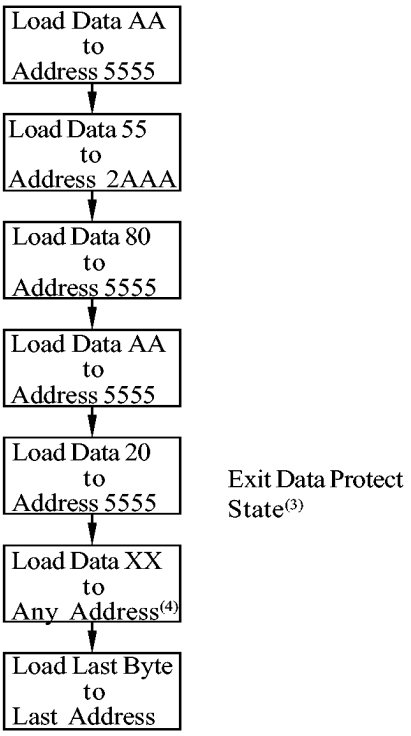


t_S = 5used (min)
$t_W = t_H$ = 10 msec (min)
V_H=12.0 V +/- 0.5 V

Software Data Protection Enable Algorithm[1]



Software Data Protection Disable Algorithm[1]



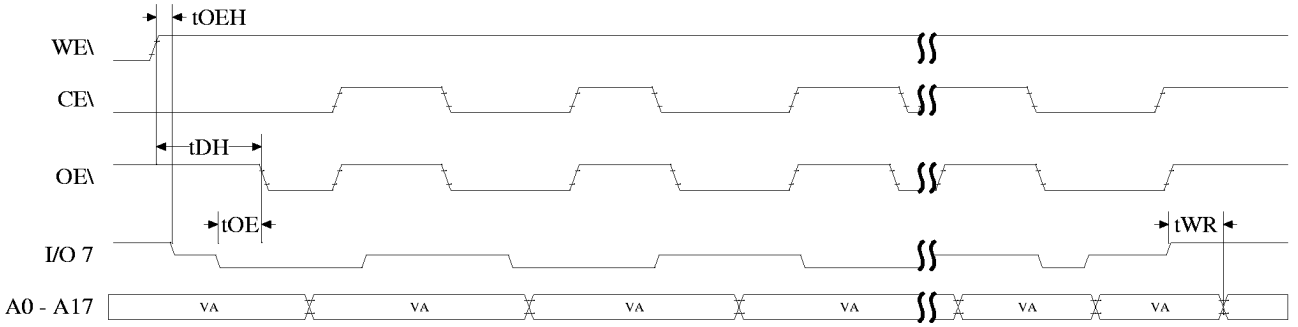
Notes:
1. Data Format: I/O 7 - I/O0 (Hex)
2. Write Protect state will be active at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.
5. A0-A14 must conform to the addressing sequence for the first three bytes as shown above.
6. After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A16) must be the same for each high to low transition of WE (or CE).
7. OE Must be high only when WE and CE are both low.

Data Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
TDH	Data hold Time	10			ns
TOEH	OE Hold Time	10			ns
TOE	OE to Output Delay (2)				ns
TWR	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

Data Polling Waveforms

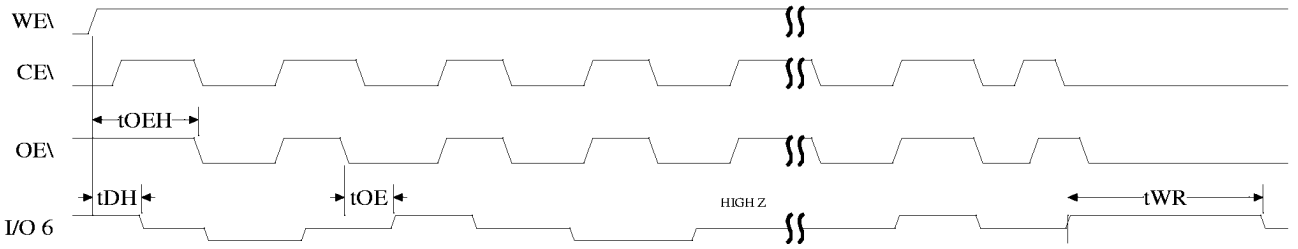


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
TDH	Data Hold Time	10			ns
TOEH	OE Hold Time	10			ns
TOE	OE to Output Delay (2)				ns
TOEHP	OE High Pulse	150			ns
ICC	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characteristics.

Toggle Bit Waveforms(1,2,3)



Notes: 1. Toggling either OE or CE or Both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

DEVICE IDENTIFICATION:

An extra 128 bytes of EEPROM memory are available to the user for identification. By raising A9 to 12 V +/- 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE:

The entire device can be erased using a six byte software code. Please see Software Chip Erase application note for details.

MECHANICAL DEFINITION
for the AS7E128K32 Pin Grid Array Package No. 801