NEC

MOS INTEGRATED CIRCUIT

# μPD16715A

## 384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

### DESCRIPTION

The μPD16715A is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values γ-corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as $V_{SS2}$ + 0.1 V to $V_{DD2}$ – 0.1 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 55 MHz when driving at 3.0 V, this driver is applicable to XGA/SXGA-standard TFT-LCD panels.

### FEATURES

- CMOS level input
- 384 outputs
- Input of 6 bits (gradation data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Logic power supply ($V_{DD1}$): 3.3 V ± 0.3 V
- Driver power supply ($V_{DD2}$): 11.0 V $^{+2.5}_{-2.0}$ V
- High-speed data transfer: $f_{CLK}$ = 55 MHz (internal data transfer speed when operating at 3.0 V)
- Output dynamic range $V_{SS2}$ + 0.1 V to $V_{DD2}$ – 0.1 V
- Apply for only dot-line inversion
- Single bank arrangement is possible (POL)
- Display data inversion function (POL2)
- Low power control function (LPC)
- ★ • Single-sided mounting (Slim TCP)

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD16715AN- xxx | TCP (TAB package) |

**Remark** The TCP's external shape is customized. To order your TCP's external shape, please contact an NEC salesperson.



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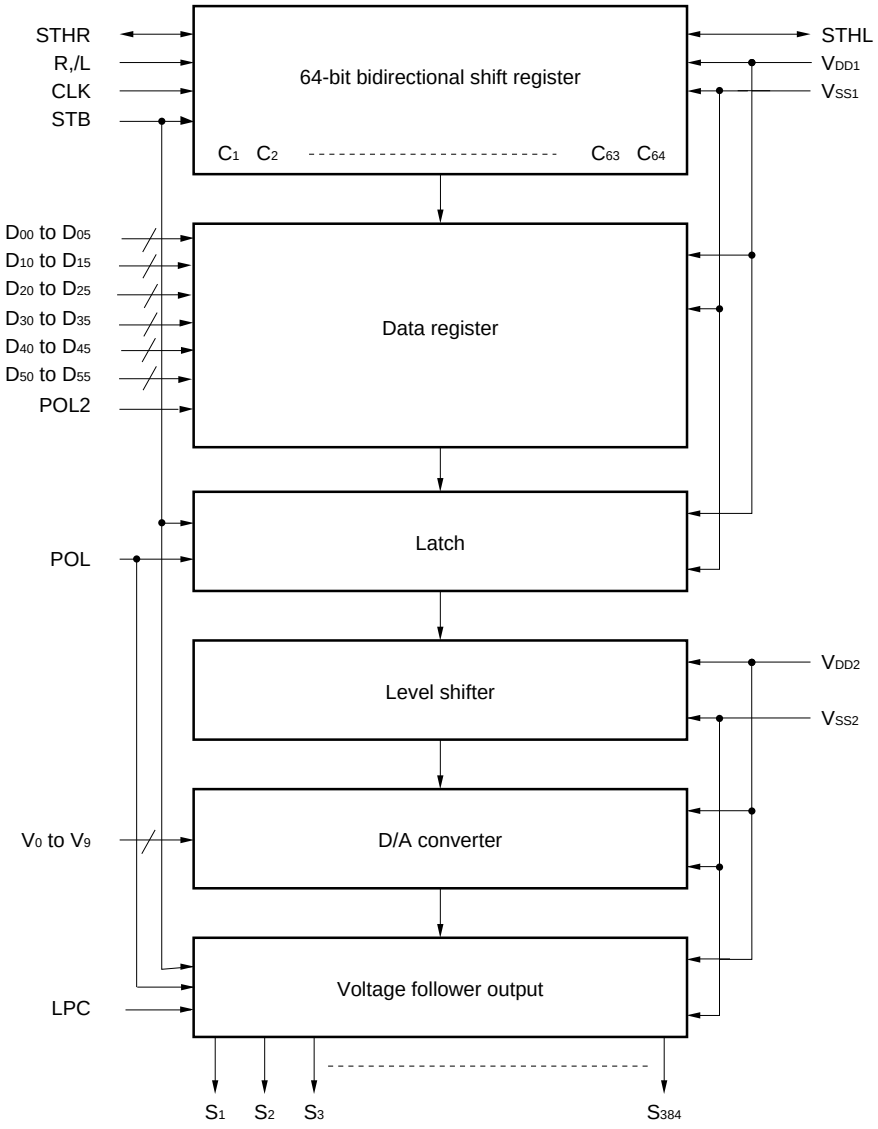
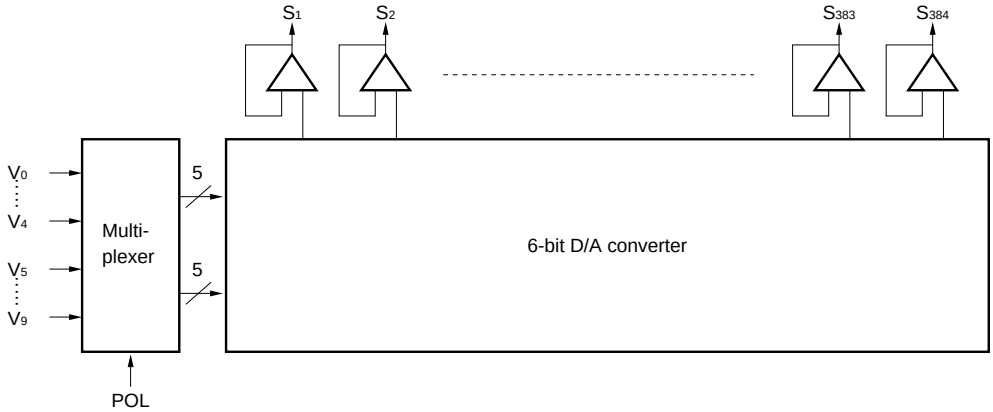
**The mark ★ shows major revised points.**

## 1. BLOCK DIAGRAM

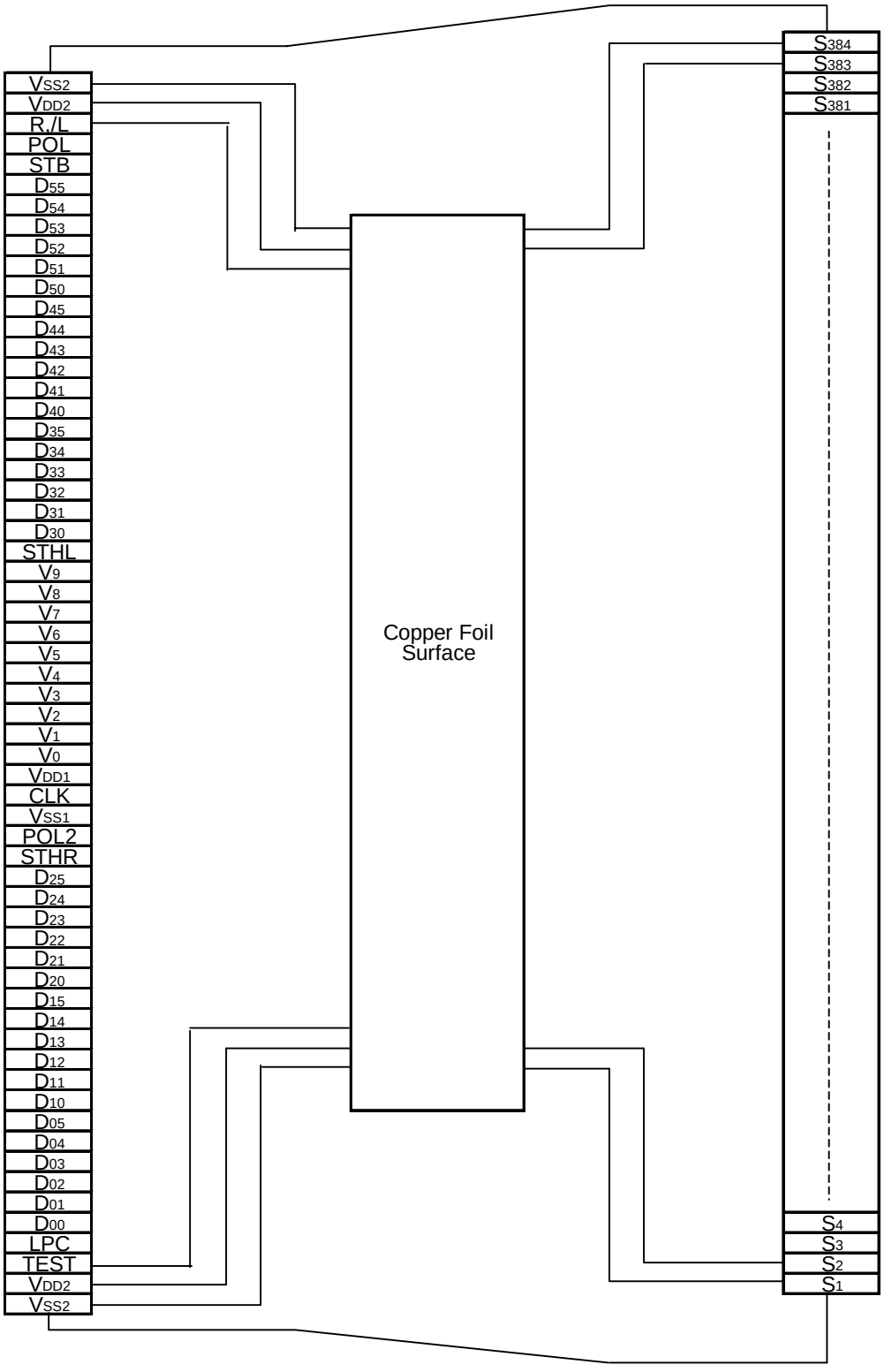



**Remark** /xxx indicates active low signal.

## 2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



### 3. PIN CONFIGURATION (μPD16715AN-xxx)




**Remark** This figure does not specify the TCP package.

## 4. PIN FUNCTIONS

(1/2)

| Pin Symbol | Pin Name | Description |
|---|---|---|
| $S_1$ to $S_{384}$ | Driver output | The D/A converted 64-gray scale analog voltage is output. |
| $D_{00}$ to $D_{05}$ | Display data input | The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels).<br>$D_{X0}$ : LSB, $D_{X5}$: MSB |
| $D_{10}$ to $D_{15}$ | | |
| $D_{20}$ to $D_{25}$ | | |
| $D_{30}$ to $D_{35}$ | | |
| $D_{40}$ to $D_{45}$ | | |
| $D_{50}$ to $D_{55}$ | | |
| R,/L | Shift direction control input | These refer to the start pulse input/output pins when driver ICs are connected in cascade. The shift directions of the shift registers are as follows.<br>R,/L = H: STHR input, $S_1 \rightarrow S_{384}$, STHL output<br>R,/L = L : STHL input, $S_{384} \rightarrow S_1$, STHR output |
| STHR | Right shift start pulse input/output | R,/L = H: Becomes the start pulse input pin.<br>R,/L = L : Becomes the start pulse output pin. |
| STHL | Left shift start pulse input/output | R,/L = H: Becomes the start pulse output pin.<br>R,/L = L : Becomes the start pulse input pin. |
| CLK | Shift clock input | Refers to the shift register's shift clock input. The display data is incorporated into the data register at the rising edge. At the rising edge of the 64th clock after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. The initial-level driver's 64th clock becomes valid as the next-level driver's start pulse is input. If 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge. |
| STB | Latch input | The contents of the data register are transferred to the latch circuit at the rising edge. And, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period. |
| POL | Polarity input | POL = L: The $S_{2n-1}$ output uses $V_0$ to $V_4$ as the reference supply ;<br>The $S_{2n}$ output uses $V_5$ to $V_9$ as the reference supply.<br>POL = H : The $S_{2n-1}$ output uses $V_5$ to $V_9$ as the reference supply ;<br>The $S_{2n}$ output uses $V_0$ to $V_4$ as the reference supply.<br>$S_{2n-1}$ indicates the odd output: and $S_{2n}$ indicates the even output. Input of the POL signal is allowed the setup time ($t_{POL-STB}$) with respect to STB's rising edge. |
| POL2 | Data inversion | POL2 = H : Display data is inverted.<br>POL2 = L : Display data is not inverted |
| LPC | Driver voltage selection | The output buffer constant current source is blocked, reducing current consumption. Low power mode (LPC = 'H': DC-level input possible). The condition that low power mode can be used is that the load constant is at least 10 kΩ + 50 pF. |
| $V_0$ to $V_9$ | γ-corrected power supplies | Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level.<br>$V_{DD2} - 0.1\ V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\ V$ |
| TEST | Test pin | Test pin. Please input H or Open. |
| $V_{DD1}$ | Logic power supply | 3.3 V ± 0.3 V |
| $V_{DD2}$ | Driver power supply | 11.0 V $^{+2.5}_{-2.0}$ V |
| $V_{SS1}$ | Logic ground | Grounding |
| $V_{SS2}$ | Driver ground | Grounding |

**Cautions 1. The power start sequence must be $V_{DD1}$, logic input, and $V_{DD2}$ & $V_0$ to $V_9$ in that order. Reverse this sequence to shut down. (Simultaneous power application to $V_{DD2}$ and $V_0$ to $V_9$ is possible.)**

**2. To stabilize the supply voltage, please be sure to insert a 0.47 μF bypass capacitor between $V_{DD1}$-$V_{SS1}$ and $V_{DD2}$-$V_{SS2}$. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also advised between the γ-corrected power supply terminals ($V_0$, $V_1$, $V_2$, ⋯, $V_9$) and $V_{SS2}$.**

## 5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The μPD16715A incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors $r_0$ to $r_{62}$ are so designed that the ratios between the LCD panel's γ - corrected voltages and $V_{0'}$ to $V_{63'}$ and $V_{0''}$ to $V_{63''}$ are roughly equal; and their respective resistance values are as shown on next page. Among the 5-by-2 γ -corrected voltages, input gray scale voltages of the same polarity with respect to the common voltage, for the respective five γ -corrected voltages of $V_0$ to $V_4$ and $V_5$ to $V_9$

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages $V_{DD2}$ and $V_{SS2}$, common electrode potential $V_{COM}$, and γ - corrected voltages $V_0$ to $V_9$ and the input data. Be sure to maintain the voltage relationships of

$$V_{DD2} - 0.1\ V > V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2} + 0.1\ V.$$

Figures 5-2 and 5-3 show the relationship between the input data and the output voltage. Therefore, please do not use it for γ - corrected power supply level inversion in double-sided mounting.

**Figure 5–1. Relationship Between Input Data and γ - corrected Power Supply**

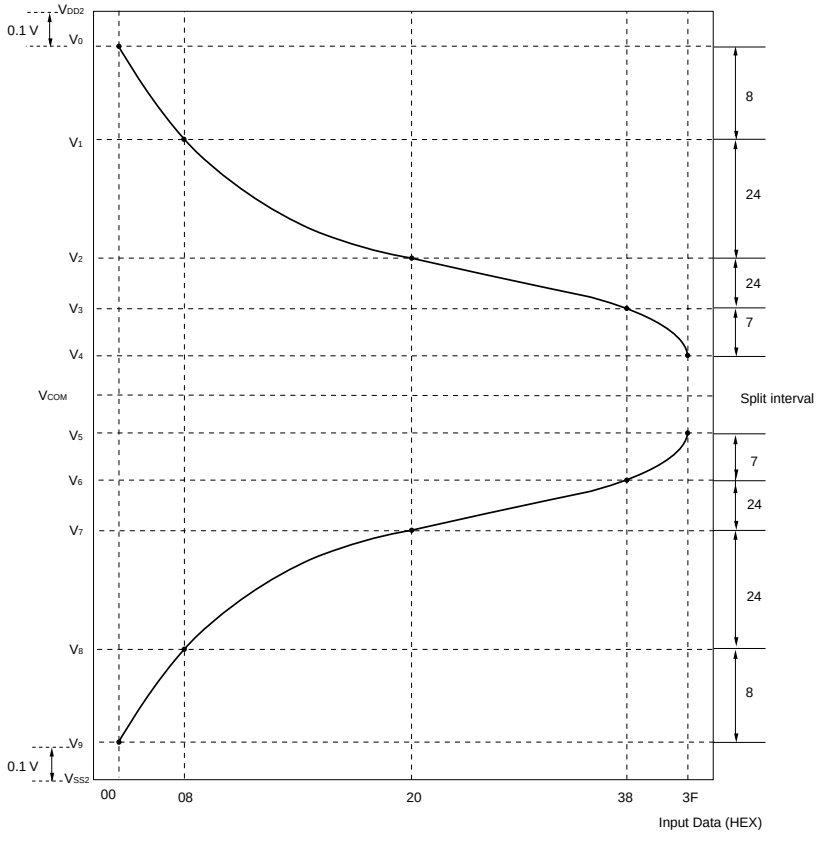
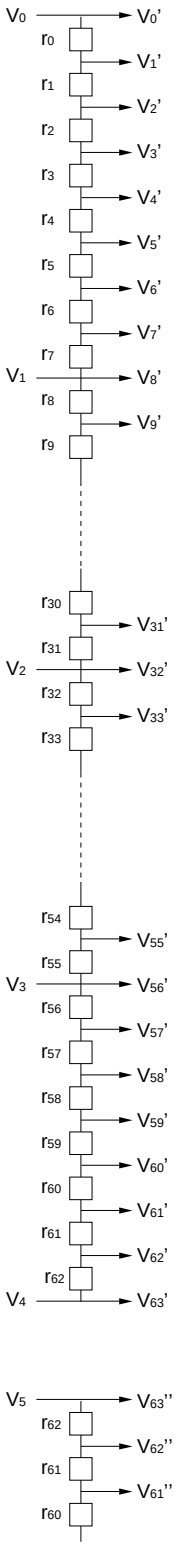


**Figure 5–2. Relationship between Input Data and Output Voltage (1/2)**

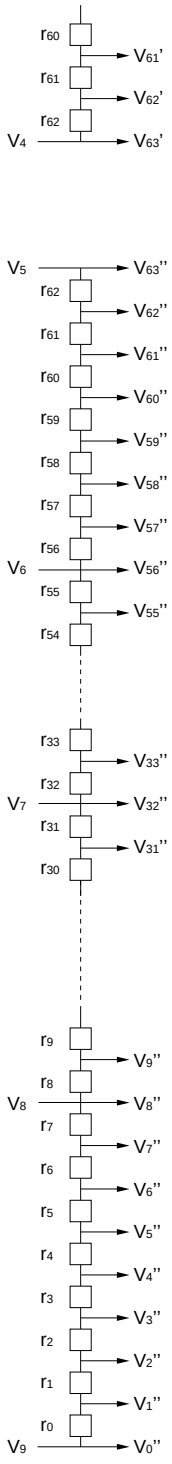
**$V_{DD2}$ – 0.1 V > $V_0$ > $V_1$ > $V_2$ > $V_3$ > $V_4$**




| Data | $D_{X5}$ | $D_{X4}$ | $D_{X3}$ | $D_{X2}$ | $D_{X1}$ | $D_{X0}$ | Output Voltage | | | | r n(Ω) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00H | 0 | 0 | 0 | 0 | 0 | 0 | $V_0$' | $V_0$ | | | r0 | 800 |
| 01H | 0 | 0 | 0 | 0 | 0 | 1 | $V_1$' | $V_1+(V_0-V_1)\times$ | 4300 / | 5100 | r1 | 750 |
| 02H | 0 | 0 | 0 | 0 | 1 | 0 | $V_2$' | $V_1+(V_0-V_1)\times$ | 3550 / | 5100 | r2 | 700 |
| 03H | 0 | 0 | 0 | 0 | 1 | 1 | $V_3$' | $V_1+(V_0-V_1)\times$ | 2850 / | 5100 | r3 | 650 |
| 04H | 0 | 0 | 0 | 1 | 0 | 0 | $V_4$' | $V_1+(V_0-V_1)\times$ | 2200 / | 5100 | r4 | 600 |
| 05H | 0 | 0 | 0 | 1 | 0 | 1 | $V_5$' | $V_1+(V_0-V_1)\times$ | 1600 / | 5100 | r5 | 550 |
| 06H | 0 | 0 | 0 | 1 | 1 | 0 | $V_6$' | $V_1+(V_0-V_1)\times$ | 1050 / | 5100 | r6 | 550 |
| 07H | 0 | 0 | 0 | 1 | 1 | 1 | $V_7$' | $V_1+(V_0-V_1)\times$ | 500 / | 5100 | r7 | 500 |
| 08H | 0 | 0 | 1 | 0 | 0 | 0 | $V_8$' | $V_1$ | | | r8 | 500 |
| 09H | 0 | 0 | 1 | 0 | 0 | 1 | $V_9$' | $V_1+(V_0-V_1)\times$ | 5200 / | 5700 | r9 | 400 |
| 0AH | 0 | 0 | 1 | 0 | 1 | 0 | $V_{10}$' | $V_1+(V_0-V_1)\times$ | 4800 / | 5700 | r10 | 400 |
| 0BH | 0 | 0 | 1 | 0 | 1 | 1 | $V_{11}$' | $V_1+(V_0-V_1)\times$ | 4400 / | 5700 | r11 | 350 |
| 0CH | 0 | 0 | 1 | 1 | 0 | 0 | $V_{12}$' | $V_1+(V_0-V_1)\times$ | 4050 / | 5700 | r12 | 350 |
| 0DH | 0 | 0 | 1 | 1 | 0 | 1 | $V_{13}$' | $V_1+(V_0-V_1)\times$ | 3700 / | 5700 | r13 | 350 |
| 0EH | 0 | 0 | 1 | 1 | 1 | 0 | $V_{14}$' | $V_1+(V_0-V_1)\times$ | 3350 / | 5700 | r14 | 300 |
| 0FH | 0 | 0 | 1 | 1 | 1 | 1 | $V_{15}$' | $V_1+(V_0-V_1)\times$ | 3050 / | 5700 | r15 | 300 |
| 10H | 0 | 1 | 0 | 0 | 0 | 0 | $V_{16}$' | $V_1+(V_0-V_1)\times$ | 2750 / | 5700 | r16 | 300 |
| 11H | 0 | 1 | 0 | 0 | 0 | 1 | $V_{17}$' | $V_2+(V_1-V_2)\times$ | 2450 / | 5700 | r17 | 250 |
| 12H | 0 | 1 | 0 | 0 | 1 | 0 | $V_{18}$' | $V_2+(V_1-V_2)\times$ | 2200 / | 5700 | r18 | 250 |
| 13H | 0 | 1 | 0 | 0 | 1 | 1 | $V_{19}$' | $V_2+(V_1-V_2)\times$ | 1950 / | 5700 | r19 | 250 |
| 14H | 0 | 1 | 0 | 1 | 0 | 0 | $V_{20}$' | $V_2+(V_1-V_2)\times$ | 1700 / | 5700 | r20 | 200 |
| 15H | 0 | 1 | 0 | 1 | 0 | 1 | $V_{21}$' | $V_2+(V_1-V_2)\times$ | 1500 / | 5700 | r21 | 200 |
| 16H | 0 | 1 | 0 | 1 | 1 | 0 | $V_{22}$' | $V_2+(V_1-V_2)\times$ | 1300 / | 5700 | r22 | 200 |
| 17H | 0 | 1 | 0 | 1 | 1 | 1 | $V_{23}$' | $V_2+(V_1-V_2)\times$ | 1100 / | 5700 | r23 | 150 |
| 18H | 0 | 1 | 1 | 0 | 0 | 0 | $V_{24}$' | $V_2+(V_1-V_2)\times$ | 950 / | 5700 | r24 | 150 |
| 19H | 0 | 1 | 1 | 0 | 0 | 1 | $V_{25}$' | $V_2+(V_1-V_2)\times$ | 800 / | 5700 | r25 | 150 |
| 1AH | 0 | 1 | 1 | 0 | 1 | 0 | $V_{26}$' | $V_2+(V_1-V_2)\times$ | 650 / | 5700 | r26 | 150 |
| 1BH | 0 | 1 | 1 | 0 | 1 | 1 | $V_{27}$' | $V_2+(V_1-V_2)\times$ | 500 / | 5700 | r27 | 100 |
| 1CH | 0 | 1 | 1 | 1 | 0 | 0 | $V_{28}$' | $V_2+(V_1-V_2)\times$ | 400 / | 5700 | r28 | 100 |
| 1DH | 0 | 1 | 1 | 1 | 0 | 1 | $V_{29}$' | $V_2+(V_1-V_2)\times$ | 300 / | 5700 | r29 | 100 |
| 1EH | 0 | 1 | 1 | 1 | 1 | 0 | $V_{30}$' | $V_2+(V_1-V_2)\times$ | 200 / | 5700 | r30 | 100 |
| 1FH | 0 | 1 | 1 | 1 | 1 | 1 | $V_{31}$' | $V_2+(V_1-V_2)\times$ | 100 / | 5700 | r31 | 100 |
| 20H | 1 | 0 | 0 | 0 | 0 | 0 | $V_{32}$' | $V_2$ | | | r32 | 100 |
| 21H | 1 | 0 | 0 | 0 | 0 | 1 | $V_{33}$' | $V_3+(V_2-V_3)\times$ | 2450 / | 2550 | r33 | 100 |
| 22H | 1 | 0 | 0 | 0 | 1 | 0 | $V_{34}$' | $V_3+(V_2-V_3)\times$ | 2350 / | 2550 | r34 | 100 |
| 23H | 1 | 0 | 0 | 0 | 1 | 1 | $V_{35}$' | $V_3+(V_2-V_3)\times$ | 2250 / | 2550 | r35 | 100 |
| 24H | 1 | 0 | 0 | 1 | 0 | 0 | $V_{36}$' | $V_3+(V_2-V_3)\times$ | 2150 / | 2550 | r36 | 100 |
| 25H | 1 | 0 | 0 | 1 | 0 | 1 | $V_{37}$' | $V_3+(V_2-V_3)\times$ | 2050 / | 2550 | r37 | 100 |
| 26H | 1 | 0 | 0 | 1 | 1 | 0 | $V_{38}$' | $V_3+(V_2-V_3)\times$ | 1950 / | 2550 | r38 | 100 |
| 27H | 1 | 0 | 0 | 1 | 1 | 1 | $V_{39}$' | $V_3+(V_2-V_3)\times$ | 1850 / | 2550 | r39 | 100 |
| 28H | 1 | 0 | 1 | 0 | 0 | 0 | $V_{40}$' | $V_3+(V_2-V_3)\times$ | 1750 / | 2550 | r40 | 100 |
| 29H | 1 | 0 | 1 | 0 | 0 | 1 | $V_{41}$' | $V_3+(V_2-V_3)\times$ | 1650 / | 2550 | r41 | 100 |
| 2AH | 1 | 0 | 1 | 0 | 1 | 0 | $V_{42}$' | $V_3+(V_2-V_3)\times$ | 1550 / | 2550 | r42 | 100 |
| 2BH | 1 | 0 | 1 | 0 | 1 | 1 | $V_{43}$' | $V_3+(V_2-V_3)\times$ | 1450 / | 2550 | r43 | 100 |
| 2CH | 1 | 0 | 1 | 1 | 0 | 0 | $V_{44}$' | $V_3+(V_2-V_3)\times$ | 1350 / | 2550 | r44 | 100 |
| 2DH | 1 | 0 | 1 | 1 | 0 | 1 | $V_{45}$' | $V_3+(V_2-V_3)\times$ | 1250 / | 2550 | r45 | 100 |
| 2EH | 1 | 0 | 1 | 1 | 1 | 0 | $V_{46}$' | $V_3+(V_2-V_3)\times$ | 1150 / | 2550 | r46 | 100 |
| 2FH | 1 | 0 | 1 | 1 | 1 | 1 | $V_{47}$' | $V_3+(V_2-V_3)\times$ | 1050 / | 2550 | r47 | 100 |
| 30H | 1 | 1 | 0 | 0 | 0 | 0 | $V_{48}$' | $V_3+(V_2-V_3)\times$ | 950 / | 2550 | r48 | 100 |
| 31H | 1 | 1 | 0 | 0 | 0 | 1 | $V_{49}$' | $V_4+(V_3-V_4)\times$ | 850 / | 2550 | r49 | 100 |
| 32H | 1 | 1 | 0 | 0 | 1 | 0 | $V_{50}$' | $V_4+(V_3-V_4)\times$ | 750 / | 2550 | r50 | 100 |
| 33H | 1 | 1 | 0 | 0 | 1 | 1 | $V_{51}$' | $V_4+(V_3-V_4)\times$ | 650 / | 2550 | r51 | 100 |
| 34H | 1 | 1 | 0 | 1 | 0 | 0 | $V_{52}$' | $V_4+(V_3-V_4)\times$ | 550 / | 2550 | r52 | 100 |
| 35H | 1 | 1 | 0 | 1 | 0 | 1 | $V_{53}$' | $V_4+(V_3-V_4)\times$ | 450 / | 2550 | r53 | 150 |
| 36H | 1 | 1 | 0 | 1 | 1 | 0 | $V_{54}$' | $V_4+(V_3-V_4)\times$ | 300 / | 2550 | r54 | 150 |
| 37H | 1 | 1 | 0 | 1 | 1 | 1 | $V_{55}$' | $V_4+(V_3-V_4)\times$ | 150 / | 2550 | r55 | 150 |
| 38H | 1 | 1 | 1 | 0 | 0 | 0 | $V_{56}$' | $V_3$ | | | r56 | 200 |
| 39H | 1 | 1 | 1 | 0 | 0 | 1 | $V_{57}$' | $V_4+(V_3-V_4)\times$ | 2300 / | 2500 | r57 | 200 |
| 3AH | 1 | 1 | 1 | 0 | 1 | 0 | $V_{58}$' | $V_4+(V_3-V_4)\times$ | 2100 / | 2500 | r58 | 250 |
| 3BH | 1 | 1 | 1 | 0 | 1 | 1 | $V_{59}$' | $V_4+(V_3-V_4)\times$ | 1850 / | 2500 | r59 | 250 |
| 3CH | 1 | 1 | 1 | 1 | 0 | 0 | $V_{60}$' | $V_4+(V_3-V_4)\times$ | 1600 / | 2500 | r60 | 300 |
| 3DH | 1 | 1 | 1 | 1 | 0 | 1 | $V_{61}$' | $V_4+(V_3-V_4)\times$ | 1300 / | 2500 | r61 | 500 |
| 3EH | 1 | 1 | 1 | 1 | 1 | 0 | $V_{62}$' | $V_4+(V_3-V_4)\times$ | 800 / | 2500 | r62 | 800 |
| 3FH | 1 | 1 | 1 | 1 | 1 | 1 | $V_{63}$' | $V_4$ | | | rtotal | 15850 |

**Figure 5–3. Relationship between Input Data and Output Voltage (2/2)**

**$V_5 > V_6 > V_7 > V_8 > V_9 > V_{SS2}$ + 0.1 V**




| Data | $D_{X5}$ | $D_{X4}$ | $D_{X3}$ | $D_{X2}$ | $D_{X1}$ | $D_{X0}$ | Output Voltage | | | | rn(Ω) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 00H | 0 | 0 | 0 | 0 | 0 | 0 | $V_0$" | $V_9$ | | | r0 | 800 |
| 01H | 0 | 0 | 0 | 0 | 0 | 1 | $V_1$" | $V_9+(V_8-V_9)\times$ | 800 / | 5100 | r1 | 750 |
| 02H | 0 | 0 | 0 | 0 | 1 | 0 | $V_2$" | $V_9+(V_8-V_9)\times$ | 1550 / | 5100 | r2 | 700 |
| 03H | 0 | 0 | 0 | 0 | 1 | 1 | $V_3$" | $V_9+(V_8-V_9)\times$ | 2250 / | 5100 | r3 | 650 |
| 04H | 0 | 0 | 0 | 1 | 0 | 0 | $V_4$" | $V_9+(V_8-V_9)\times$ | 2900 / | 5100 | r4 | 600 |
| 05H | 0 | 0 | 0 | 1 | 0 | 1 | $V_5$" | $V_9+(V_8-V_9)\times$ | 3500 / | 5100 | r5 | 550 |
| 06H | 0 | 0 | 0 | 1 | 1 | 0 | $V_6$" | $V_9+(V_8-V_9)\times$ | 4050 / | 5100 | r6 | 550 |
| 07H | 0 | 0 | 0 | 1 | 1 | 1 | $V_7$" | $V_9+(V_8-V_9)\times$ | 4600 / | 5100 | r7 | 500 |
| 08H | 0 | 0 | 1 | 0 | 0 | 0 | $V_8$" | $V_8$ | | | r8 | 500 |
| 09H | 0 | 0 | 1 | 0 | 0 | 1 | $V_9$" | $V_9+(V_8-V_9)\times$ | 500 / | 5700 | r9 | 400 |
| 0AH | 0 | 0 | 1 | 0 | 1 | 0 | $V_{10}$" | $V_9+(V_8-V_9)\times$ | 900 / | 5700 | r10 | 400 |
| 0BH | 0 | 0 | 1 | 0 | 1 | 1 | $V_{11}$" | $V_9+(V_8-V_9)\times$ | 1300 / | 5700 | r11 | 350 |
| 0CH | 0 | 0 | 1 | 1 | 0 | 0 | $V_{12}$" | $V_9+(V_8-V_9)\times$ | 1650 / | 5700 | r12 | 350 |
| 0DH | 0 | 0 | 1 | 1 | 0 | 1 | $V_{13}$" | $V_9+(V_8-V_9)\times$ | 2000 / | 5700 | r13 | 350 |
| 0EH | 0 | 0 | 1 | 1 | 1 | 0 | $V_{14}$" | $V_9+(V_8-V_9)\times$ | 2350 / | 5700 | r14 | 300 |
| 0FH | 0 | 0 | 1 | 1 | 1 | 1 | $V_{15}$" | $V_9+(V_8-V_9)\times$ | 2650 / | 5700 | r15 | 300 |
| 10H | 0 | 1 | 0 | 0 | 0 | 0 | $V_{16}$" | $V_9+(V_8-V_9)\times$ | 2950 / | 5700 | r16 | 300 |
| 11H | 0 | 1 | 0 | 0 | 0 | 1 | $V_{17}$" | $V_8+(V_7-V_8)\times$ | 3250 / | 5700 | r17 | 250 |
| 12H | 0 | 1 | 0 | 0 | 1 | 0 | $V_{18}$" | $V_8+(V_7-V_8)\times$ | 3500 / | 5700 | r18 | 250 |
| 13H | 0 | 1 | 0 | 0 | 1 | 1 | $V_{19}$" | $V_8+(V_7-V_8)\times$ | 3750 / | 5700 | r19 | 250 |
| 14H | 0 | 1 | 0 | 1 | 0 | 0 | $V_{20}$" | $V_8+(V_7-V_8)\times$ | 4000 / | 5700 | r20 | 200 |
| 15H | 0 | 1 | 0 | 1 | 0 | 1 | $V_{21}$" | $V_8+(V_7-V_8)\times$ | 4200 / | 5700 | r21 | 200 |
| 16H | 0 | 1 | 0 | 1 | 1 | 0 | $V_{22}$" | $V_8+(V_7-V_8)\times$ | 4400 / | 5700 | r22 | 200 |
| 17H | 0 | 1 | 0 | 1 | 1 | 1 | $V_{23}$" | $V_8+(V_7-V_8)\times$ | 4600 / | 5700 | r23 | 150 |
| 18H | 0 | 1 | 1 | 0 | 0 | 0 | $V_{24}$" | $V_8+(V_7-V_8)\times$ | 4750 / | 5700 | r24 | 150 |
| 19H | 0 | 1 | 1 | 0 | 0 | 1 | $V_{25}$" | $V_8+(V_7-V_8)\times$ | 4900 / | 5700 | r25 | 150 |
| 1AH | 0 | 1 | 1 | 0 | 1 | 0 | $V_{26}$" | $V_8+(V_7-V_8)\times$ | 5050 / | 5700 | r26 | 150 |
| 1BH | 0 | 1 | 1 | 0 | 1 | 1 | $V_{27}$" | $V_8+(V_7-V_8)\times$ | 5200 / | 5700 | r27 | 100 |
| 1CH | 0 | 1 | 1 | 1 | 0 | 0 | $V_{28}$" | $V_8+(V_7-V_8)\times$ | 5300 / | 5700 | r28 | 100 |
| 1DH | 0 | 1 | 1 | 1 | 0 | 1 | $V_{29}$" | $V_8+(V_7-V_8)\times$ | 5400 / | 5700 | r29 | 100 |
| 1EH | 0 | 1 | 1 | 1 | 1 | 0 | $V_{30}$" | $V_8+(V_7-V_8)\times$ | 5500 / | 5700 | r30 | 100 |
| 1FH | 0 | 1 | 1 | 1 | 1 | 1 | $V_{31}$" | $V_8+(V_7-V_8)\times$ | 5600 / | 5700 | r31 | 100 |
| 20H | 1 | 0 | 0 | 0 | 0 | 0 | $V_{32}$" | $V_7$ | | | r32 | 100 |
| 21H | 1 | 0 | 0 | 0 | 0 | 1 | $V_{33}$" | $V_7+(V_6-V_7)\times$ | 100 / | 2550 | r33 | 100 |
| 22H | 1 | 0 | 0 | 0 | 1 | 0 | $V_{34}$" | $V_7+(V_6-V_7)\times$ | 200 / | 2550 | r34 | 100 |
| 23H | 1 | 0 | 0 | 0 | 1 | 1 | $V_{35}$" | $V_7+(V_6-V_7)\times$ | 300 / | 2550 | r35 | 100 |
| 24H | 1 | 0 | 0 | 1 | 0 | 0 | $V_{36}$" | $V_7+(V_6-V_7)\times$ | 400 / | 2550 | r36 | 100 |
| 25H | 1 | 0 | 0 | 1 | 0 | 1 | $V_{37}$" | $V_7+(V_6-V_7)\times$ | 500 / | 2550 | r37 | 100 |
| 26H | 1 | 0 | 0 | 1 | 1 | 0 | $V_{38}$" | $V_7+(V_6-V_7)\times$ | 600 / | 2550 | r38 | 100 |
| 27H | 1 | 0 | 0 | 1 | 1 | 1 | $V_{39}$" | $V_7+(V_6-V_7)\times$ | 700 / | 2550 | r39 | 100 |
| 28H | 1 | 0 | 1 | 0 | 0 | 0 | $V_{40}$" | $V_7+(V_6-V_7)\times$ | 800 / | 2550 | r40 | 100 |
| 29H | 1 | 0 | 1 | 0 | 0 | 1 | $V_{41}$" | $V_7+(V_6-V_7)\times$ | 900 / | 2550 | r41 | 100 |
| 2AH | 1 | 0 | 1 | 0 | 1 | 0 | $V_{42}$" | $V_7+(V_6-V_7)\times$ | 1000 / | 2550 | r42 | 100 |
| 2BH | 1 | 0 | 1 | 0 | 1 | 1 | $V_{43}$" | $V_7+(V_6-V_7)\times$ | 1100 / | 2550 | r43 | 100 |
| 2CH | 1 | 0 | 1 | 1 | 0 | 0 | $V_{44}$" | $V_7+(V_6-V_7)\times$ | 1200 / | 2550 | r44 | 100 |
| 2DH | 1 | 0 | 1 | 1 | 0 | 1 | $V_{45}$" | $V_7+(V_6-V_7)\times$ | 1300 / | 2550 | r45 | 100 |
| 2EH | 1 | 0 | 1 | 1 | 1 | 0 | $V_{46}$" | $V_7+(V_6-V_7)\times$ | 1400 / | 2550 | r46 | 100 |
| 2FH | 1 | 0 | 1 | 1 | 1 | 1 | $V_{47}$" | $V_7+(V_6-V_7)\times$ | 1500 / | 2550 | r47 | 100 |
| 30H | 1 | 1 | 0 | 0 | 0 | 0 | $V_{48}$" | $V_7+(V_6-V_7)\times$ | 1600 / | 2550 | r48 | 100 |
| 31H | 1 | 1 | 0 | 0 | 0 | 1 | $V_{49}$" | $V_6+(V_5-V_6)\times$ | 1700 / | 2550 | r49 | 100 |
| 32H | 1 | 1 | 0 | 0 | 1 | 0 | $V_{50}$" | $V_6+(V_5-V_6)\times$ | 1800 / | 2550 | r50 | 100 |
| 33H | 1 | 1 | 0 | 0 | 1 | 1 | $V_{51}$" | $V_6+(V_5-V_6)\times$ | 1900 / | 2550 | r51 | 100 |
| 34H | 1 | 1 | 0 | 1 | 0 | 0 | $V_{52}$" | $V_6+(V_5-V_6)\times$ | 2000 / | 2550 | r52 | 100 |
| 35H | 1 | 1 | 0 | 1 | 0 | 1 | $V_{53}$" | $V_6+(V_5-V_6)\times$ | 2100 / | 2550 | r53 | 150 |
| 36H | 1 | 1 | 0 | 1 | 1 | 0 | $V_{54}$" | $V_6+(V_5-V_6)\times$ | 2250 / | 2550 | r54 | 150 |
| 37H | 1 | 1 | 0 | 1 | 1 | 1 | $V_{55}$" | $V_6+(V_5-V_6)\times$ | 2400 / | 2550 | r55 | 150 |
| 38H | 1 | 1 | 1 | 0 | 0 | 0 | $V_{56}$" | $V_6$ | | | r56 | 200 |
| 39H | 1 | 1 | 1 | 0 | 0 | 1 | $V_{57}$" | $V_6+(V_5-V_6)\times$ | 200 / | 2500 | r57 | 200 |
| 3AH | 1 | 1 | 1 | 0 | 1 | 0 | $V_{58}$" | $V_6+(V_5-V_6)\times$ | 400 / | 2500 | r58 | 250 |
| 3BH | 1 | 1 | 1 | 0 | 1 | 1 | $V_{59}$" | $V_6+(V_5-V_6)\times$ | 650 / | 2500 | r59 | 250 |
| 3CH | 1 | 1 | 1 | 1 | 0 | 0 | $V_{60}$" | $V_6+(V_5-V_6)\times$ | 900 / | 2500 | r60 | 300 |
| 3DH | 1 | 1 | 1 | 1 | 0 | 1 | $V_{61}$" | $V_6+(V_5-V_6)\times$ | 1200 / | 2500 | r61 | 500 |
| 3EH | 1 | 1 | 1 | 1 | 1 | 0 | $V_{62}$" | $V_6+(V_5-V_6)\times$ | 1700 / | 2500 | r62 | 800 |
| 3FH | 1 | 1 | 1 | 1 | 1 | 1 | $V_{63}$" | $V_5$ | | | rtotal | 15850 |

## 6. RELATIONSHIP BETWEEN OUTPUT DATA AND D/A CONVERTER

Data format : 6 bits × 2 RGBs (6 dots)
Input width : 36 bits (2-pixel data)

**R,/L = H (Right shift)**

| Output | $S_1$ | $S_2$ | $S_3$ | $S_4$ | ··· | $S_{383}$ | $S_{384}$ |
|---|---|---|---|---|---|---|---|
| Data | $D_{00}$ to $D_{05}$ | $D_{10}$ to $D_{15}$ | $D_{20}$ to $D_{25}$ | $D_{30}$ to $D_{35}$ | ··· | $D_{40}$ to $D_{45}$ | $D_{50}$ to $D_{55}$ |

**R,/L = L (Left shift)**

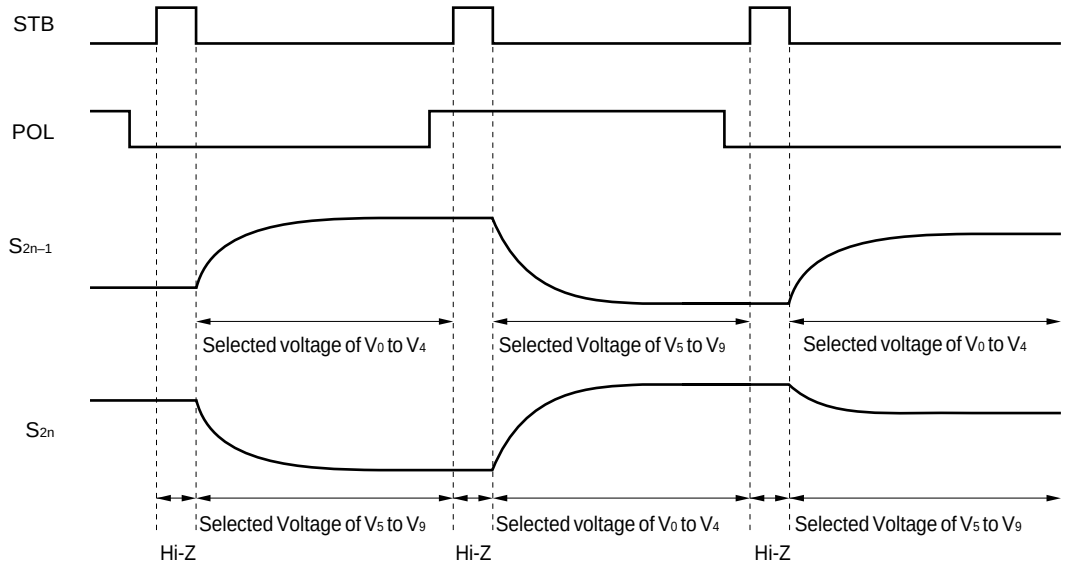
| Output | $S_1$ | $S_2$ | $S_3$ | $S_4$ | ··· | $S_{383}$ | $S_{384}$ |
|---|---|---|---|---|---|---|---|
| Data | $D_{00}$ to $D_{05}$ | $D_{10}$ to $D_{15}$ | $D_{20}$ to $D_{25}$ | $D_{30}$ to $D_{35}$ | ··· | $D_{40}$ to $D_{45}$ | $D_{50}$ to $D_{55}$ |

| POL | $S_{2n-1}$ Note | $S_{2n}$ Note |
|---|---|---|
| L | $V_0$ to $V_4$ | $V_5$ to $V_9$ |
| H | $V_5$ to $V_9$ | $V_0$ to $V_4$ |

**Note** $S_{2n-1}$ (Odd output), $S_{2n}$ (Even output), n = 1,2,···,192

## 7. RELATIONSHIP BETWEEN STB, POL, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



## 8. RELATIONSHIP BETWEEN OUTPUT DATA AND D/A CONVERTER

The μPD16715A is a dot inversion and inverts dots by alternately using a charging output buffer and a discharging output buffer. Therefore, the output voltage of the first line may not be correctly written because the last line's output polarity of frame n (n + 1) and the first line's output polarity are the same (refer to Figure 8-1).

Consequently, polarity inversion and write operation must be performed between frames (vertical blanking period) in order to invert (clear) the polarity of the wiring level of the liquid crystal panel by using the last line output of the previous frame (refer to Figure 8-2).

**Figure 8-1. Incase of the output voltage may not be correctly written**

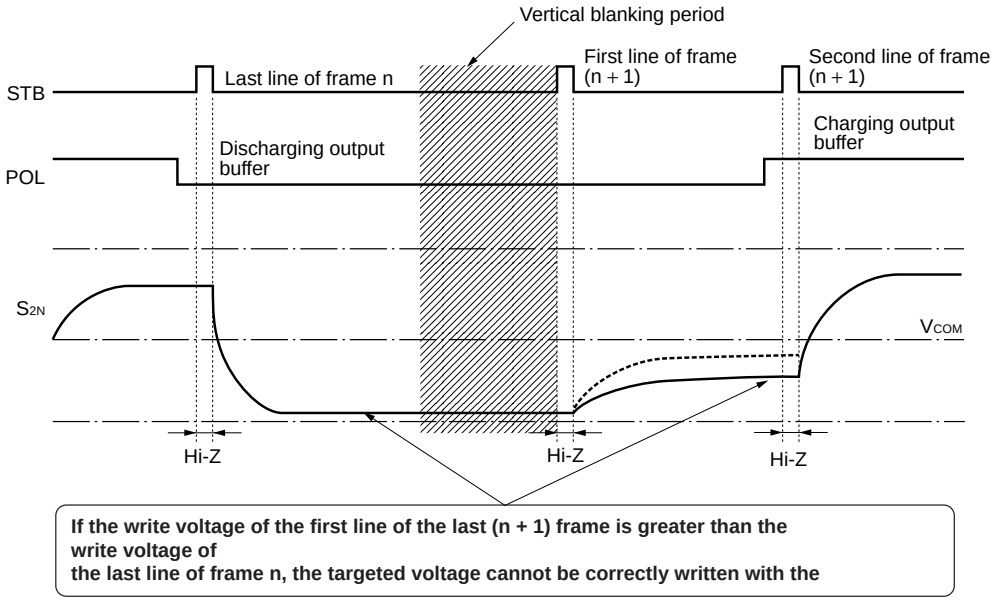
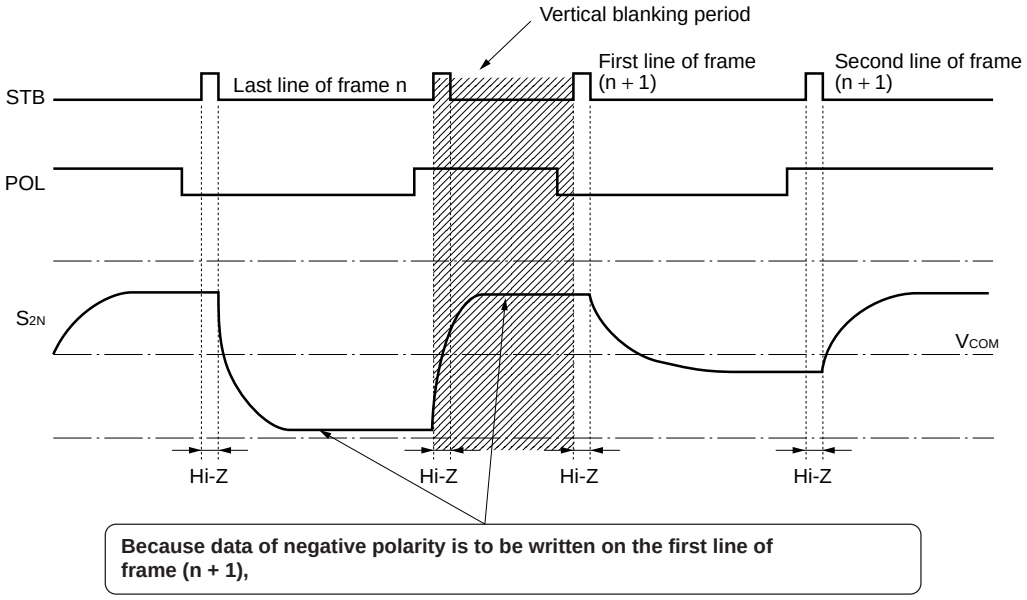



**Figure 8-2. Polarity inversion and write operation**



## 5. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings ($T_A$ = 25 °C, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Logic Part Supply Voltage | $V_{DD1}$ | –0.3 to + 6.5 | V |
| Driver Part Supply Voltage | $V_{DD2}$ | –0.5 to + 15.0 | V |
| Logic Part Input Voltage | $V_{I1}$ | –0.3 to $V_{DD1}$ + 0.3 | V |
| Driver Part Input Voltage | $V_{I2}$ | –0.3 to $V_{DD2}$ + 0.3 | V |
| Logic Part Output Voltage | $V_{O1}$ | –0.3 to $V_{DD1}$ + 0.3 | V |
| Driver Part Output Voltage | $V_{O2}$ | –0.3 to $V_{DD2}$ + 0.3 | V |
| Operating Ambient Temperature | $T_A$ | –10 to +75 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +125 | °C |

**Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.**

**Recommended Operating Range ($T_A$ = –10 to +75 °C, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Logic Supply Voltage | $V_{DD1}$ | 3.0 | 3.3 | 3.6 | V |
| Driver Supply Voltage | $V_{DD2}$ | 9.0 | 11.0 | 13.5 | V |
| High-Level Input Voltage | $V_{IH}$ | 0.7 $V_{DD1}$ | | $V_{DD1}$ | V |
| Low-Level Input Voltage | $V_{IL}$ | 0 | | 0.3 $V_{DD1}$ | V |
| γ -Corrected Voltage | $V_0$ to $V_9$ | $V_{SS2}$ + 0.1 | | $V_{DD2}$ – 0.1 | V |
| Driver Part Output Voltage | $V_O$ | $V_{SS2}$ + 0.1 | | $V_{DD2}$ – 0.1 | V |
| Clock Frequency | $f_{CLK}$ | | | 55 | MHz |

**Electrical Characteristics ($T_A$ = –10 to +75 °C, $V_{DD1}$ = 3.3 V ± 0.3 V, $V_{DD2}$ = 11.0 V $^{+2.5}_{-2.0}$V, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

| Parameter | Symbol | Condition | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input Leak Current | $I_{IL}$ | | | | | ±1.0 | μA |
| High-Level Output Voltage | $V_{OH}$ | STHR (STHL), $I_{OH}$ = 0 mA | | $V_{DD1}$ – 0.1 | | $V_{DD1}$ | V |
| Low-Level Output Voltage | $V_{OL}$ | STHR (STHL), $I_{OL}$ = 0 mA | | | | 0.1 | V |
| ★ γ-Corrected Supply Current | $I_\gamma$ | $V_{DD2}$ = 13 V, | $V_0$ pin, $V_5$ pin | | 0.31 | 0.8 | mA |
| | | $V_0$ to $V_4$ = $V_5$ to $V_9$ = 6.0 V | $V_4$ pin, $V_9$ pin | –0.8 | –0.31 | | mA |
| Driver Output Current | $I_{VOH}$ | $V_X$ = 8.0 V, $V_{OUT}$ = 6.0 V | | | | –0.25 | mA |
| | $I_{VOL}$ | $V_X$ = 1.0 V, $V_{OUT}$ = 3.0 V | | 0.25 | | | mA |
| Output Voltage Deviation | $\Delta V_O$ | Input data | | | | ±20 | mV |
| Average Output Voltage Variation | $\Delta V_{AV}$ | Input data | | | ±10 | | mV |
| Output Voltage Range | $V_O$ | Input data | | $V_{DD2}$ +0.1 | | $V_{DD2}$ – 0.1 | V |
| Logic Part Dynamic Current Consumption | $I_{DD1}$ | $V_{DD1}$ = 3.6 V, $T_A$ = 25°C | | | 1.5 | 8 | mA |
| Driver Part Dynamic Current Consumption | $I_{DD2}$ | $V_{DD1}$ = 3.0 V, $V_{DD2}$ = 13.5 V, No loads, $T_A$ = 25°C | | | 3.5 | 8 | mA |

**Cautions 1. The output voltage deviation refers to the voltage difference between adjoining output pins when the display data is the same (within the chip).**

**2. The average output voltage variation refers to the average output voltage difference between chips. The average output voltage refers to the average voltage between chips when the display data is the same.**

**3. The STB cycle is defined to be 20 μs at $f_{CLK}$ = 33 MHz.**

**4. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.**

**5. Refers to the current consumption per driver when cascades are connected under the assumption of XGA single-sided mounting (8 units).**

**Switching Characteristics ($T_A$ = –10 to +75 °C, $V_{DD1}$ = 3.3 V ± 0.3 V, $V_{DD2}$ = 11.0 V $^{+2.5}_{-2.0}$V, $V_{SS1}$ = $V_{SS2}$ = 0 V)**

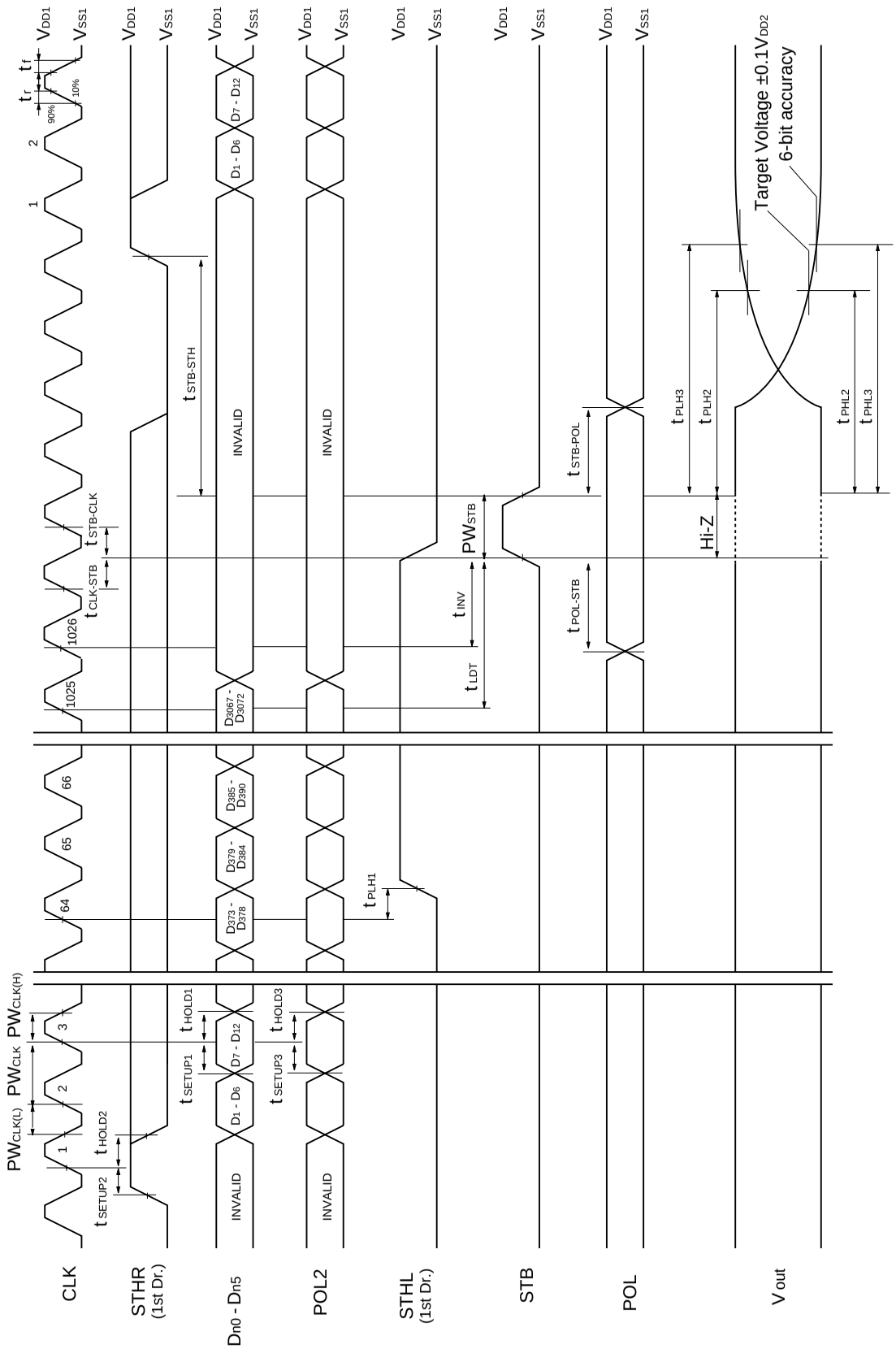
| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Start Pulse Delay Time | $t_{PLH1}$ | $C_L$ = 25 pF | | 9.1 | 14 | ns |
| Driver Output Delay Time | $t_{PLH2}$ | $C_L$ = 50 pF, $R_L$ = 50 kΩ | | 5.2 | 11 | μs |
| | $t_{PLH3}$ | | | 9.9 | 17 | μs |
| | $t_{PHL2}$ | | | 5.3 | 11 | μs |
| | $t_{PHL3}$ | | | 10.4 | 17 | μs |
| Input Capacitance | $C_{I1}$ | STHR (STHL) excluded, $T_A$ = 25°C | | 5.8 | 15 | pF |
| | $C_{I2}$ | STHR (STHL), $T_A$ = 25°C | | 5.7 | 15 | pF |

**Timing Requirement ($T_A$ = –10 to +75 °C, $V_{DD1}$ = 3.3 V ± 0.3 V, $V_{SS1}$ = $V_{SS2}$ = 0 V, $t_r$ = $t_f$ = 8.0 ns)**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock Pulse Width | $PW_{CLK}$ | | 18 | | | ns |
| Clock Pulse High Period | $PW_{CLK(H)}$ | | 5 | | | ns |
| Clock Pulse Low Period | $PW_{CLK(L)}$ | | 5 | | | ns |
| Data Setup Time | $t_{SETUP1}$ | | 0 | | | ns |
| Data Hold Time | $t_{HOLD1}$ | | 8 | | | ns |
| Start Pulse Setup Time | $t_{SETUP2}$ | | 4 | | | ns |
| Start Pulse Hold Time | $t_{HOLD2}$ | | 5 | | | ns |
| POL2 Setup Time | $t_{SETUP3}$ | | 0 | | | ns |
| POL2 Hold Time | $t_{HOLD3}$ | | 8 | | | ns |
| STB Pulse Width | $PW_{STB}$ | | 500 | | | ns |
| Data Invalid Period | $t_{INV}$ | | 1 | | | CLK |
| Last Data Timing | $t_{LDT}$ | | 2 | | | CLK |
| CLK-STB Time | $t_{CLK-STB}$ | CLK ↑ → STB ↑ | 5 | | | ns |
| STB-CLK Time | $t_{STB-CLK}$ | STB ↑ → CLK ↑ | 5 | | | ns |
| Time Between STB and Start Pulse | $t_{STB-STH}$ | STB ↑ → STHR(STHL) ↑ | 50 | | | ns |
| POL-STB Time | $t_{POL-STB}$ | POL ↑ or ↓ → STB ↑ | –7 | | | ns |
| STB-POL Time | $t_{STB-POL}$ | STB ↓ → POL ↓ or ↑ | 9 | | | ns |

## ★ 9. SWITCHING CHARACTERISTICS WAVEFORM (R,/L = H)

**(Unless otherwise specified, the input level is defined to be $V_{IH}$ =0.5 $V_{DD1}$.)**



## 7. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for soldering conditions of the μPD16715A.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case the soldering is done under different conditions.

**Type of Surface Mount Device**

**μPD16715AN-×××: TCP (TAB package)**

| Mounting Condition | Mounting Method | Condition |
|---|---|---|
| Thermocompression | Soldering | Heating tool 300 to 350°C, heating for 2 to 3 seconds: pressure 100g (per solder) |
| | ACF (Adhesive Conductive Film) | Temporary bonding 70 to 100°C: pressure 3 to 8 kg/cm$^2$ : time 3 to 5 seconds. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm$^2$ : time 30 to 40 seconds. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.) |

**Caution To find out the detailed conditions for packaging the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more packaging methods at a time.**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference Documents**

**NEC Semiconductor Device Reliability / Quality Control System (C10983E)**

**Quality Grades to NEC's Semiconductor Devices (C11531E)**

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  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
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