FEATURES

- 2.5GHz min F_{MAX}
- 2.3V to 5.7V power supply
- Provides for any logic function of 2 variables
- Provides for 2-input muxing
- Fully differential
- Source terminated CML outputs for fast edge rates
- Accepts LVDS, PECL, PECL, CML, TTL, LVPECL, input logic levels
- Available in a tiny 10-pin MSOP

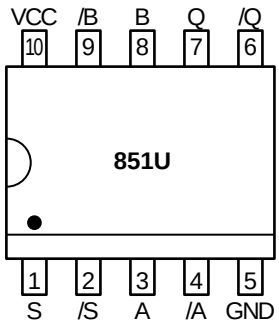
DESCRIPTION

The SY55851U is a highly flexible, universal logic gate capable of upto 2.5GHz operation. It's differential inputs and outputs will produce any of 9 possible logic functions of two Boolean variables. It can be configured as any of the following gates: AND, NAND, OR, NOR, XOR, XNOR, DELAY, NEGATION (NOT). Also, the SY55851U can function as a 2-input multiplexer.

SY55851U inputs can be terminated with a single resistor between the true and the complement pins of a given input.

The SY55851U is a member of Micrel's new Super-Lite™ family of high-speed logic devices. This family features very small packaging, high signal integrity, and operation at many different supply voltages.

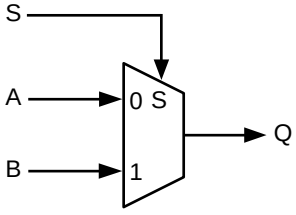
PIN CONFIGURATION



APPLICATIONS

- Port bypass
- Data communication systems
- Wireless communication systems
- Telecom systems

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

Pin	Function
A, /A	Input Data
B, /B	Input Data
Q, /Q	Output Data
S, /S	Input Selector
GND	Ground
V_{CC}	V_{CC}

PIN DESCRIPTIONS

A, /A – CML Input (Differential)

This is one of the inputs to the logic block. For a 2-variable logic function, it is either a constant value or a Boolean input. For a 2-input mux, this signal represents the output when S is set to logic zero.

B, /B – CML Input (Differential)

This is one of the inputs to the logic block. For a 2-variable logic function, it is either a constant value or a Boolean input. For a 2-input mux, this signal represents the output when S is set to logic one.

Q, /Q – CML Output (Differential)

This is the output of the logic block.

S, /S – CML Input (Differential)

This is one of the inputs to the logic block. It represents either one Boolean input for a 2-variable logic function, or the select input for a 2-input mux.

FUNCTIONAL DESCRIPTION

Establishing Static Logic Inputs

The true pin of an input pair is internally biased to ground through a 75kΩ resistor. The complement pin of an input pair is internally biased halfway between V_{CC} and ground by a voltage divider consisting of two 75kΩ resistors. To keep an input at static logic zero at V_{CC} > 3.0V, leave both inputs unconnected. For V_{CC} ≤ 3.0V, connect the complement input to V_{CC} and leave the true input unconnected. To make an input static logic one, connect the true input to V_{CC}, leave the complement input unconnected. These are the only two safe ways to cause inputs to be at a static value. In particular, no input pin should be directly connected to ground. All NC (no connect) pins should be unconnected.

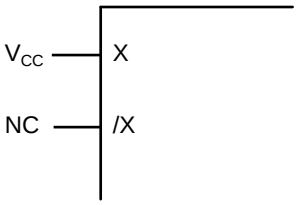
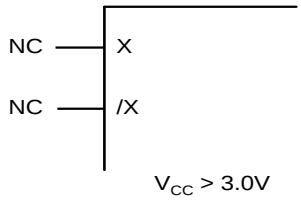


Figure 1. Hard Wiring A Logic "1" (1)



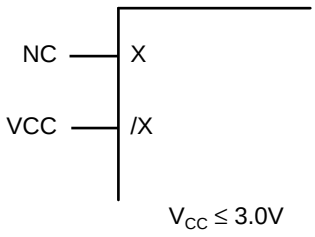
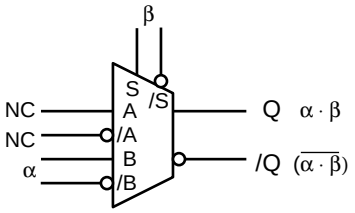


Figure 2. Hard Wiring A Logic "0" (1)

NOTE:

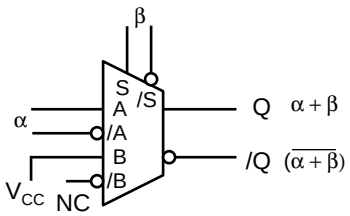
1. X is either A, B, S input. /X is either /A, /B, /S input.

TRUTH TABLES



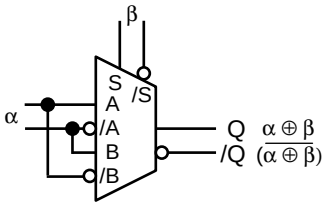
AND/NAND

A	α B	β S	α·β Q	$(\overline{\alpha \cdot \beta})$ /Q
L	L	L	L	H
L	H	L	L	H
L	L	H	L	H
L	H	H	H	L



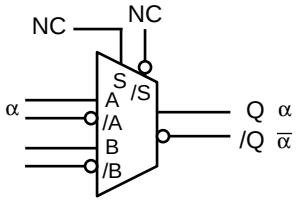
OR/NOR

α A	B	β S	α + β Q	$(\overline{\alpha + \beta})$ /Q
L	H	L	L	H
H	H	L	H	L
L	H	H	H	L
H	H	H	H	L



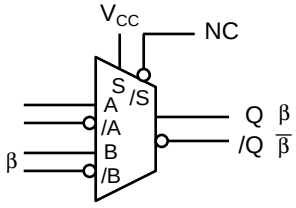
XOR/XNOR

α A	B	β S	α ⊕ β Q	$(\overline{\alpha \oplus \beta})$ /Q
L	H	L	L	H
L	H	H	H	L
H	L	L	H	L
H	L	H	L	H

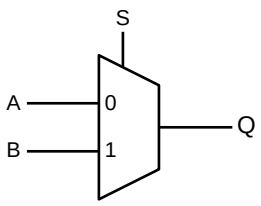


DELAY/NEGATION

α A	B	S	α Q	$\overline{\alpha}$ /Q
L	X	L	L	H
H	X	L	H	L



A	β B	S	β Q	$\overline{\beta}$ /Q
X	L	H	L	H
X	H	H	H	L



2:1 MUX

S	Q
H	B
L	A

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	–0.5 to +6.0	V
V_I	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	CML Output Voltage	V_{CC} –1.0 to V_{CC} +0.5	V
T_A	Operating Temperature Range	–40 to +85	°C
T_{store}	Storage Temperature Range	–65 to +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

CML TERMINATION

All inputs accept the output from any other member of this family. All outputs are source terminated 100Ω CML differential drivers as shown in Figures 3 and 4. SY55851U expects the inputs to be terminated, and that good high speed design practices be adhered to. SY55851U inputs are designed to accept a termination resistor between the true and complement inputs of a differential pair. 0402 form factor chip resistors will fit with some trace fanout.

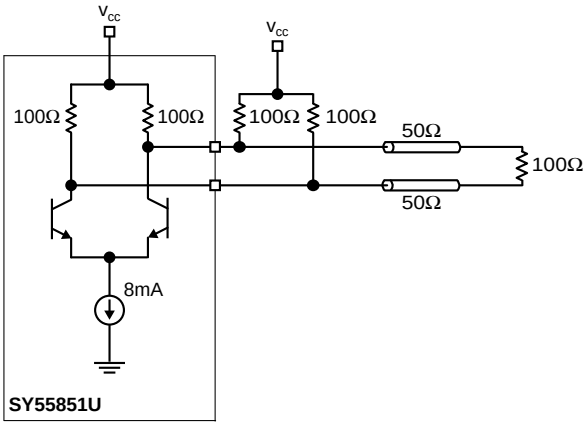


Figure 3a. Differentially Terminated (50Ω Load CML Output)

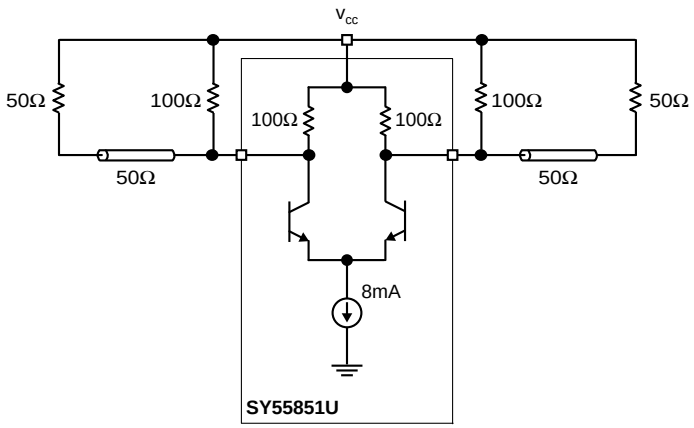


Figure 3b. Individually Terminated (50Ω Load CML Output)

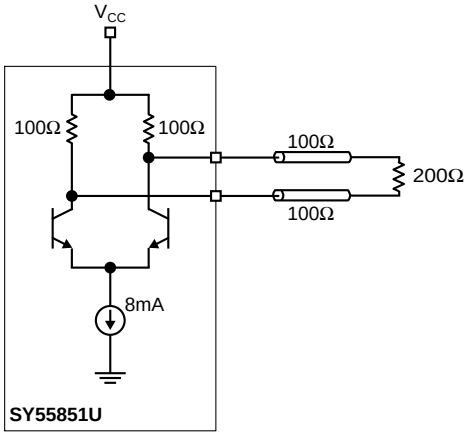


Figure 4. 100Ω Load CML Output

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.3V to 5.7V; GND = 0V

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{CC}	Power Supply Voltage	2.3	5.7	2.3	5.7	2.3	5.7	2.3	5.7	mA
I_{CC}	Power Supply Current	—	40	—	40	—	40	—	40	mA

CML DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{ID}	Differential Input Voltage	100	—	—	mV	
V_{IH}	Input HIGH Voltage	1.6	—	V_{CC}	V	
V_{IL}	Input LOW Voltage	1.5	—	V_{CC} – 0.1	V	
V_{OH}	Output HIGH Voltage	V_{CC} – 0.020	V_{CC} – 0.010	V_{CC}	V	No Load
V_{OL}	Output LOW Voltage	V_{CC} – 0.97	V_{CC} – 0.825	V_{CC} – 0.700	V	No Load
V_{OS}	Output Voltage Swing[2]	0.700	0.800 0.400 0.200	0.950	V	No Load 100Ω Environment[4] 50Ω Environmnet[3]
R_{DRIVE}	Output Source Impedance	80	100	120	Ω	

NOTES:

1. Equilibrium temperature.
2. Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400mV swing is available in the 100Ω environment and a 200mV swing in the 50Ω environment. Refer to the “CML Termination” diagram for more details.
3. See Figure 3a and 3b.
4. See Figure 4.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.3V to 5.7V; GND = 0V; T_A = –40°C to +85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition[1]
f_{MAX}	Max. Operating Frequency	2.5	—	—	GHz	
t_{PIN0}	Propagation Delay, S to Q	—	—	350	ps	
t_{PIN1}	Propagation Delay, A to Q	—	—	350	ps	
t_{PIN2}	Propagation Delay, B to Q	—	—	350	ps	
t_r t_f	CML Output Rise/Fall Times (20% to 80%)	TBD	—	110	ps	

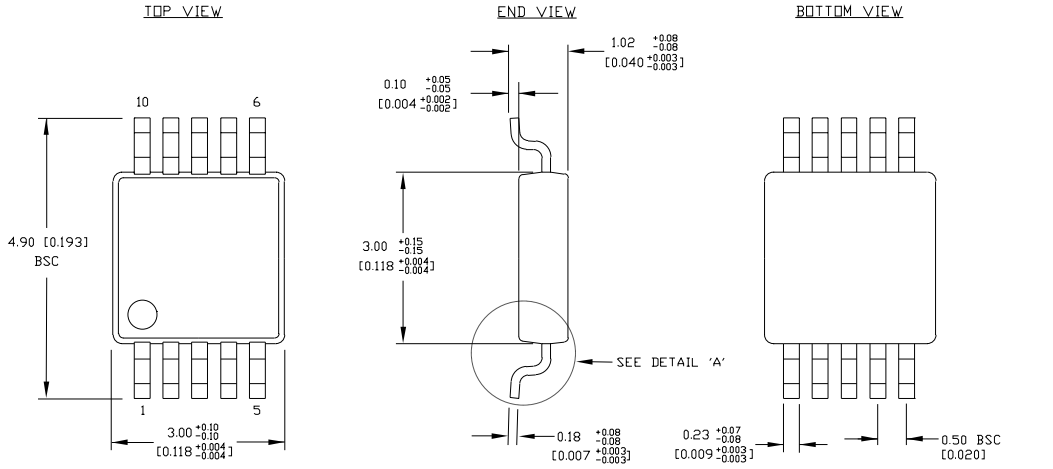
NOTE:

1. Tested using environment of Figure 3b, 50Ω load CML output.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY55851UKC	K10-1	Commercial

10 LEAD MSOP (K10-1)



Rev. 00

MICREL-SYNERGY 3250 SCOTT BOULEVARD SANTA CLARA CA 95054 USA

TEL + 1 (408) 980-9191 FAX + 1 (408) 914-7878 WEB http://www.synergysemi.com http://www.micrel.com