Nordic VLSI ASA

10-Bit 20MSPS Sampling Analog-to-Digital Converter

nAD1020-25

FEATURES

- 2.5V power supply
- SNR typ 60dB for (f_{in} = 10MHz)
- Low power (37mW@2.5V)
- Sample rate:10 - 20MSPS
- Frequency dependent biasing
- Internal/sample hold
- Differential input
- Low input capacitance
- Evaluation Board Available

APPLICATIONS

- Imaging
- Test equipment
- Computer scanners
- Communications
- Set top boxes
- Video products

GENERAL DESCRIPTION

The nAD1020-25 is a compact, high-speed, low power 10-bit monolithic analog-to-digital converter, implemented in the TSMC Mixed-Signal MiM CMOS process. It has 10-bit resolution with 9.5 effective bits, and close to 11 bit dynamic range for video frequency signals. The converter includes a high bandwidth sample and hold. The full scale range is ±1V. The full scale range can be set between ±0.5V and ±1V. It operates from a single 2.5V supply. Its low distortion and high dynamic range offers the performance needed for demanding imaging, multimedia, telecommunications and instrumentation applications.

The bias current level for the ADC is automatically adjusted based on the clock input frequency. Hence, the power dissipation of the device is continuously minimised for the current operation frequency.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	supply voltage		2.25	2.5	2.75	V
I_{DD}	supply current (20 MSPS)			15		mA
P_D	power dissipation (20 MSPS)	Except digital output drivers		37		mW
P_D	power dissipation (10 MSPS)	Except digital output drivers		20		mW
P_D	power dissipation (sleep mode)	Except digital output drivers		1.5		mW
DNL	differential nonlinearity	f_{IN}=0.9991MHz			±0.5	LSB
INL	integral nonlinearity	f_{IN}=0.9991MHz			±1	LSB
f_S	conversion rate		10		20	MHz
N	resolution				10	bit

Table 1. Quick reference data

GENERAL DESCRIPTION (Continued)

The nAD1020-25 has a pipelined architecture - resulting in low input capacitance. Digital error correction of the 9 most significant bits ensures good linearity for input frequencies approaching Nyquist. The nAD1020-25 is compact. The core occupies less than 1mm^2 of die area in TSMC Mixed Signal MiM 0.25µm CMOS process. The fully differential architecture makes it insensitive to substrate noise. Thus it is ideal as a mixed signal ASIC macro cell.

BLOCK DIAGRAM

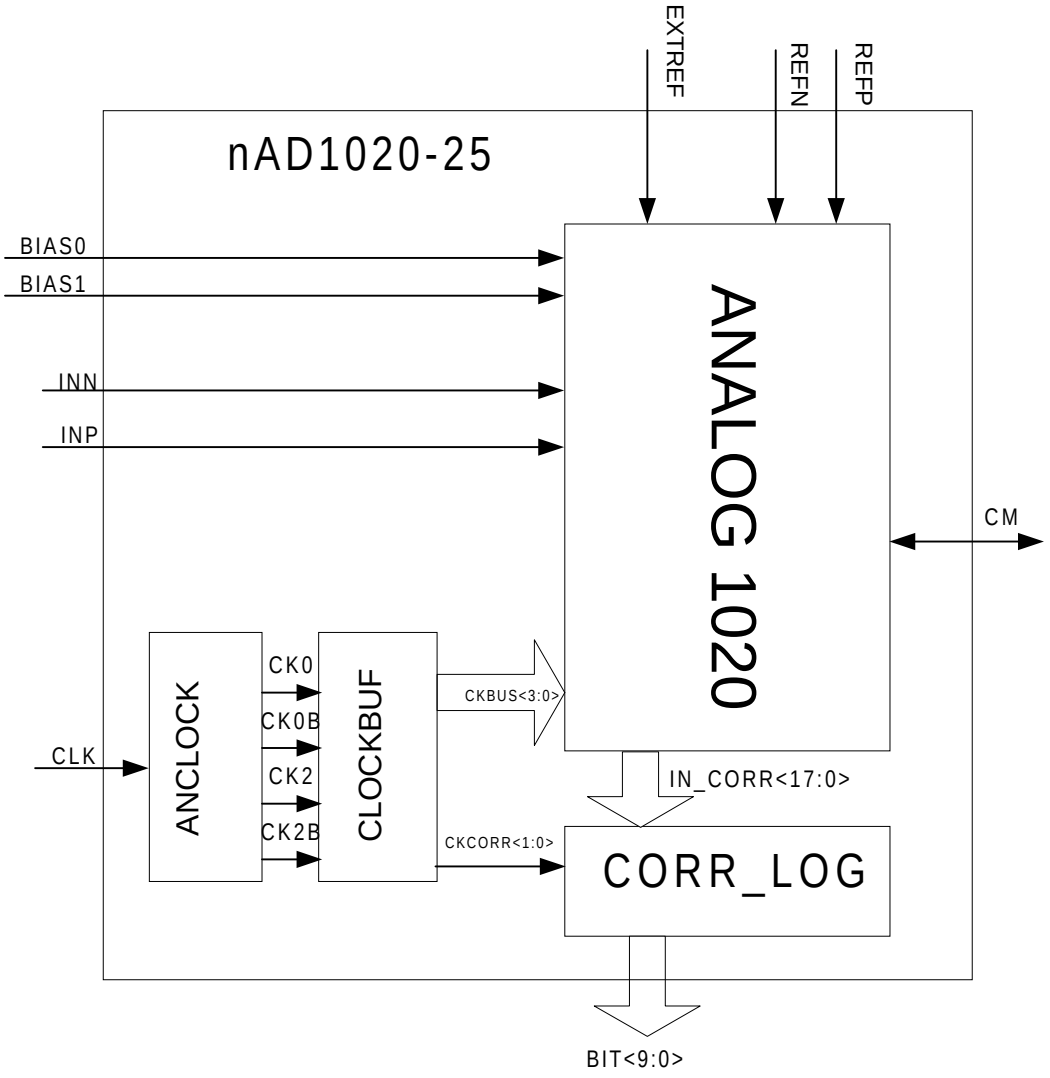

Figure 1. Block diagram nAD1020-25

ELECTRICAL SPECIFICATIONS

(At T_A = 25°C, V_{DD} = 2.5V, Sampling Rate = 20MHz, Input frequency = 10MHz dBFS, Differential input signal, 50% duty cycle clock unless otherwise noted).

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Units
	DC Accuracy					
DNL	Differential Nonlinearity					
	f_{IN} = 0.9991 MHz	III		±0.5	±1.0	LSB
INL	Integral Nonlinearity					
	f_{IN} = 0.9991 MHz	III		±1.0	±3.0	LSB
V_{OS}	Midscale offset	III		± 5.9		mV
CMRR	Common Mode Rejection Ratio (of V_{OS})			-65		dB
	Dynamic Performance					
SINAD	Signal to Noise and Distortion Ratio					
	f_{IN} = 1 MHz	III	57	60		dBFS
	f_{IN} = 10 MHz	III	57	60		dBFS
SNR	Signal to Noise Ratio (without harmonics)					
	f_{IN} = 10 MHz	III	57	60		dBFS
SFDR	Spurious Free Dynamic Range					
	f_{IN} = 1 MHz	III	60	72		dBFS
	f_{IN} = 10 MHz	III	60	69		dBFS
PSRR	Power Supply Rejection Ratio (of V_{OS})	III		-55		dB
	Analog Input					
V_{FSR}	Input Voltage Range (differential)	IV	±0.5	±1.2		V
V_{CMI}	Common mode input voltage	III	1	1.2	1.35	V
C_{INA}	Input Capacitance (differential)	III		2.5		pF
	Reference Voltages					
V_{REFN}	Negative Input Voltage	III	0.7	0.85		V
V_{REFP}	Positive Input Voltage	III		1.60	1.7	V
V_{RR}	Reference input voltage range [1]	III	0.5	0.75	1	V
V_{CM}	Common mode output voltage	III		1.2		V
	Digital Inputs					
V_{IL}	Logic “0” voltage	IV			0.4	V
V_{IH}	Logic “1” voltage	IV	AV_{DD} -0.4			V
I_{IL}	Logic “0” current (V_I=V_{SS})	IV			±10	µA
I_{IH}	Logic “1” current (V_I=V_{DD})	IV			±10	µA
C_{IND}	Input Capacitance	IV		5		pF
	Digital Outputs					
V_{OL}	Logic “0” voltage (I = 2 mA)	IV		0.2	0.4	V
V_{OH}	Logic “1” voltage (I = 2 mA)	IV	85% OV_{DD}	90% OV_{DD}		V
t_H	Output hold time	V		1.9		ns
t_D	Output delay time	V		4.8		ns

(table continued on next page)

[1] See “Input Signal Range” section

	Switching Performance					
f_S	Conversion Rate	V	10	20		MSPS
	Pipeline Delay	IV		6		Clocks
σ_{AP}	Aperture jitter	V		TBD		ps
t_{AP}	Aperture delay	V		1.4		ns
	Power Supply					
V_{DD}	supply voltage	V	2.25	2.5	2.75	V
I_{DD}	supply current (except digital output)	IV		15		mA
P_D	power dissipation (except digital output) (20 MSPS)	IV		37		mW
P_D	power dissipation (except digital output) (10 MSPS)	IV		20		mW
P_D	power dissipation (except digital output) (sleep mode) [1)]	IV		1.5		mW
V_{SS}	supply voltage			GND		
AV_{DD}-DV_{DD1}	analog power – digital power pins		-0.2		+0.2	V
OV_{DD}	Output driver supply voltage	III	2.25	2.5/3.0	3.3	V
T	Ambient operating temperature	IV	-40		+85	°C

Table 3. Electrical specifications

[1)] Power Down Mode ("zero" power dissipation) available for IP version of nAD1020-25

Test Levels

Test Level I: 100% production tested at +25°C
Test Level II: 100% production tested at +25°C and sample tested at specified temperatures
Test Level III: Sample tested only
Test Level IV: Parameter is guaranteed by design and characterisation testing
Test Level V: Parameter is typical value only
Test Level VI: 100% production tested at +25°C. Guaranteed by design and characterisation testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply voltages

AV_{DD} .....- 0.3V to +3V
DV_{DD1}.....- 0.3V to V_{DD} + 0.3V
OV_{DD} .....- 0.3V to V_{DD} + 0.3V

Input voltages

Analog In.....- 0.3V to AV_{DD} + 0.3V
Digital In.....- 0.3V to V_{DD} + 0.3V
REF_P.....- 0.3V to AV_{DD} + 0.3V
REF_N.....- 0.3V to AV_{DD} + 0.3V
CLOCK .....- 0.3V to V_{DD} + 0.3V

Temperatures

Operating Temperature....-40 to +85°C
Storage Temperature…..-65 to +125°C

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
INP INN	Differential input signal pins. Common mode voltage: 1.2V
REFP REFN	Reference input pins. Bypass with 100nF ‖ 1nF capacitors close to the pins. See Application Information below.
BIAS0, BIAS1	Digital inputs for max. sampling rate programming. BIAS1=0, BIAS0=0: Sleep mode (power save) BIAS1=0, BIAS0=1: - 12.5% bias BIAS1=1, BIAS0=0: +12.5% bias BIAS1=1, BIAS0=1: Typ. Bias The bias current is automatically scaled based on the clock input frequency.
CLK	Clock input
CM	Common mode voltage output
BIT9 - BIT0	Digital outputs (MSB to LSB)
OUTEN	Enable digital outputs
EXTREF	Disable internal references
V_{DD}	Power pins for chip core
V_{SS}	Ground pins
OV_{DD}	Power pins for output drivers

Table 4. Pin functions

PIN ASSIGNMENT

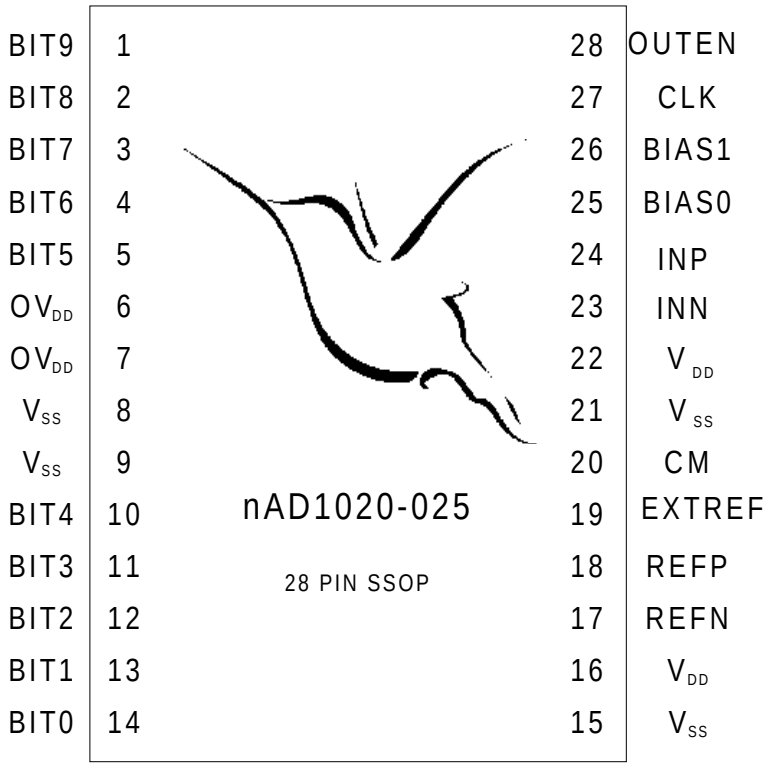

Figure 2. Pin assignment for the 28 pin package

TIMING DIAGRAM

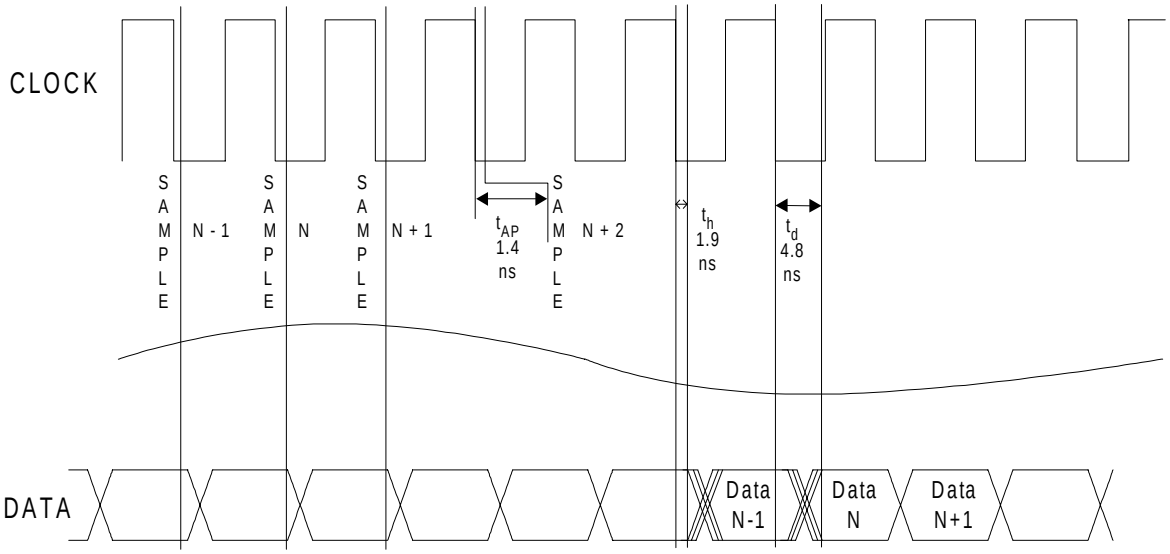

Figure 4. Timing diagram

INPUT SIGNAL RANGE

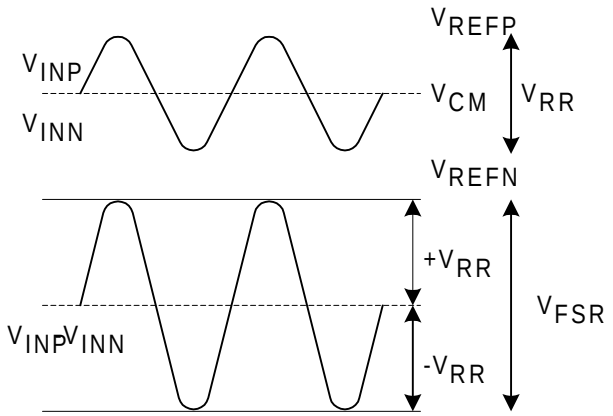

Figure 5. Definition of full scale range

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 5. Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION

References

The nAD1020-25 has a differential analog input. The input range is determined by the voltages on the reference pins REFP and REFN respectively, and is equal to ±(VREFP-VREFN). Externally generated reference voltages connected to REFP and REFN should be symmetric around 1.2V. The input range can be defined between ±0.5V and ±1.0V. The references should be bypassed as close to the converter pins as possible using 100nF capacitors in parallel with smaller capacitors (e.g. 1nF) (to ground). There should be decoupling between the reference, and from each reference to ground.

Analog input

The input of the nAD1020-25 can be configured in various ways - dependent upon whether a single ended or differential, AC- or DC-coupled input is wanted.

AC-coupled input is most conveniently implemented using a transformer with a centre tapped secondary winding. The centre tap is connected to the CM-node, as shown in figure 6. In order to obtain low distortion, it is important that the selected transformer does not exhibit core saturation at full-scale. Excellent results are obtained with the Mini Circuits T1-6T or T1-1T. Proper termination of the input is important for input signal purity. A small capacitor (typ. 21pF) across the inputs attenuates kickback-noise from the sample and hold. The CM-pin should be decoupled as close to the package as possible with a 100nF capacitor in parallel with a 1nF capacitor.

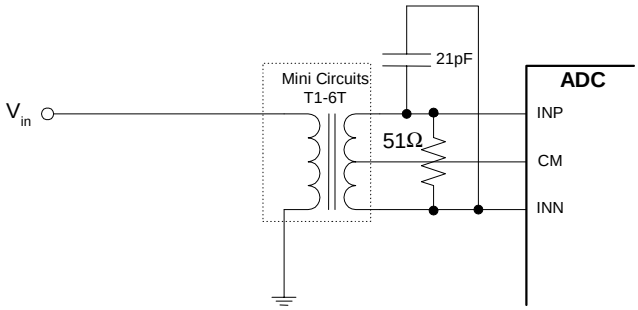

Figure 6. AC coupled input using transformer

If a DC-coupled single ended input is wanted, a solution based on operational amplifiers - as shown in Figure 7, is usually preferred. The AD826 is suggested for low distortion and video bandwidth. Lower cost operational amplifiers may be used if the demands are less strict. A good alternative for high performance applications is to use AD8138 single ended to differential amplifier.

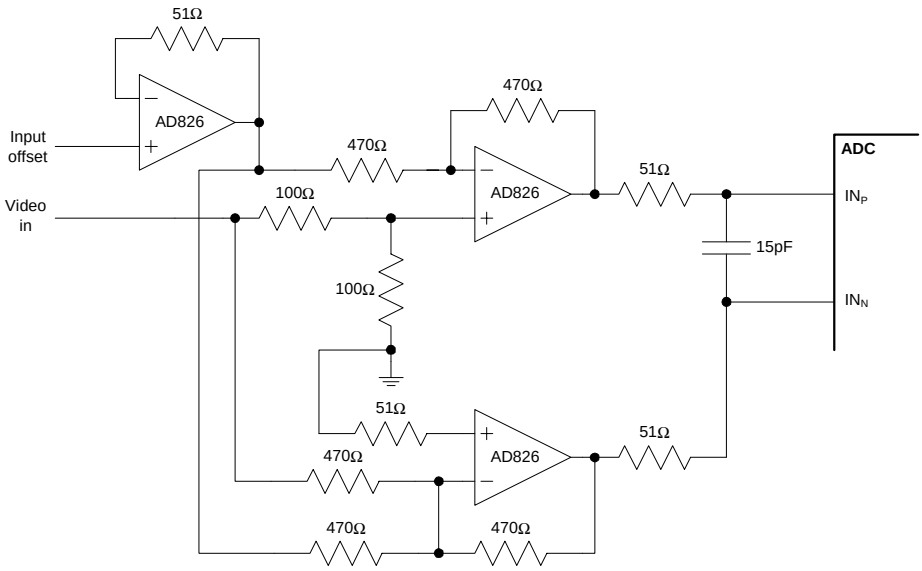

Figure 7. DC-coupled single ended to differential conversion (power supplies and bypassing not shown)

Clock

In order to preserve accuracy at high input frequency, it is important that the clock has low jitter and steep edges. Rise/fall times should be kept shorter than 2ns whenever possible. Overshoot should be avoided. Low jitter is especially important when converting high frequency input signals. Jitter causes the noise floor to rise proportionally to input signal frequency. Jitter may be caused by crosstalk on the PCB. It is therefore recommended that the clock trace on the PCB is made as short as possible.

Digital outputs

The digital output data appears in offset binary code. Full-scale negative input results in output code 000...0. Full-scale positive input results in output code 111...1. Output data are available 6 clock cycles after the data are sampled. The analog input is sampled one aperture delay (t_{AP}) after the high to low clock transition. Output data should be sampled as shown in the timing diagram.

PCB layout and decoupling

A well designed PCB is necessary to get good spectral purity from any high performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC are connected to the analog ground plane. It is our experience that this gives the best performance. The power supply pins should be bypassed using 100nF || 1nF surface mounted capacitors as close to the package pins as possible. Analog and digital supply pins should be separately filtered.

Dynamic testing

Careful testing using high quality instrumentation is necessary to achieve accurate test results on high speed A/D-converters. It is important that the clock source and signal source has low jitter. A spectrally pure, low noise RF signal generator - such as the HP8662A or HP 8644B is recommended for the test signal. Low pass filtering or band pass filtering of the input signal is usually necessary to obtain the required spectral purity (SFDR > 75dB). The clock signal can be obtained from either a crystal oscillator or a low-jitter pulse generator. Alternatively, a low-jitter RF-generator can be used as a clock source. At Nordic VLSI, the Marconi Instruments 2041A is used. The sinewave clock must then be applied to an ultra high-speed comparator (e.g. MAX961) before application to the converter. The most consistent results are obtained if the clock signal is phase locked to the input signal. Phase locking allows testing without windowing of output data. A logic analyser with deep memory - such as the HP16500-series, is recommended for test data acquisition.

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