



## MIC38300

### 3A SuperLNR™ Low Noise High Efficiency Regulator

#### ADVANCED INFORMATION

### General Description

The MIC38300 is a 3A peak, 2.2A continuous output current step down converter and the first device in a new generation of SuperLNR™ providing the benefits of LDOs in respect to ease of use, fast transient performance, high PSRR and low noise while offering the efficiency of a switching regulator.

As output voltages move lower, the output noise and transient response of a switching regulator become an increasing challenge for designers. By combining a switcher whose output is slaved to the input of a high performance LDO, high efficiency is achieved with a clean low noise output. The MIC38300 is designed to provide less than 5mV of peak to peak noise and over 70dB of PSRR at 1kHz. Furthermore, the architecture of the MIC38300 is optimized for fast load transients allowing to maintain less than 30mV of output voltage deviation even during ultra fast load steps, making the MIC38300 an ideal choice for low voltage ASICs and other digital ICs.

The MIC38300 features a fully integrated switching regulator and LDO combo, operates with input voltages from 3.0V to 5.5V input and offers adjustable output voltages down to 1.0V.

The MIC38300 is offered in the small 28-pin 4×6×0.9mm MLF® package and can operate from -40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com)

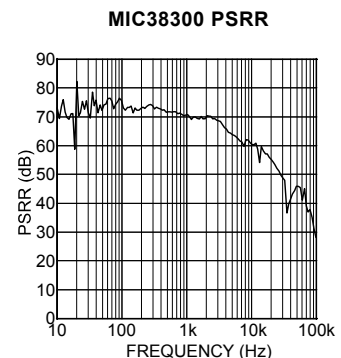
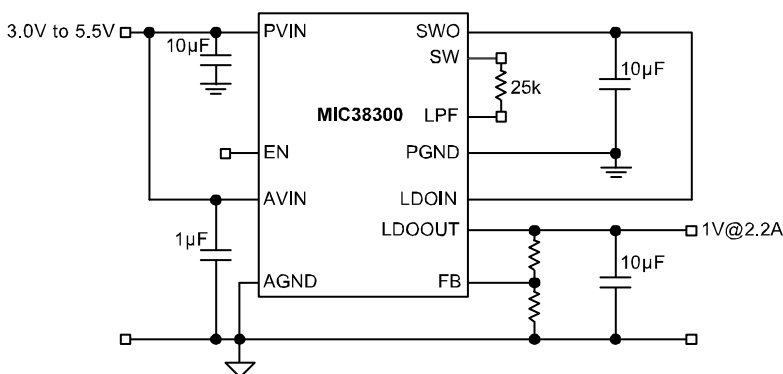
### Features

- 3A peak output current
- 2.2A continuous operating current
- Input voltage range: 3.0V to 5.5V
- Adjustable output voltage down to 1.0V
- Output noise less than 5mV
- Ultra fast transient performance
- Unique switcher plus LDO architecture
- Fully integrated MOSFET switches
- Micro-power shutdown
- Easy upgrade from LDO as power dissipation becomes an issue
- Thermal shutdown and current limit protection
- 4mm × 6mm × 0.9mm MLF® package

### Applications

- Point-of-load applications
- Networking, server, industrial power
- Wireless base-stations
- Sensitive RF applications

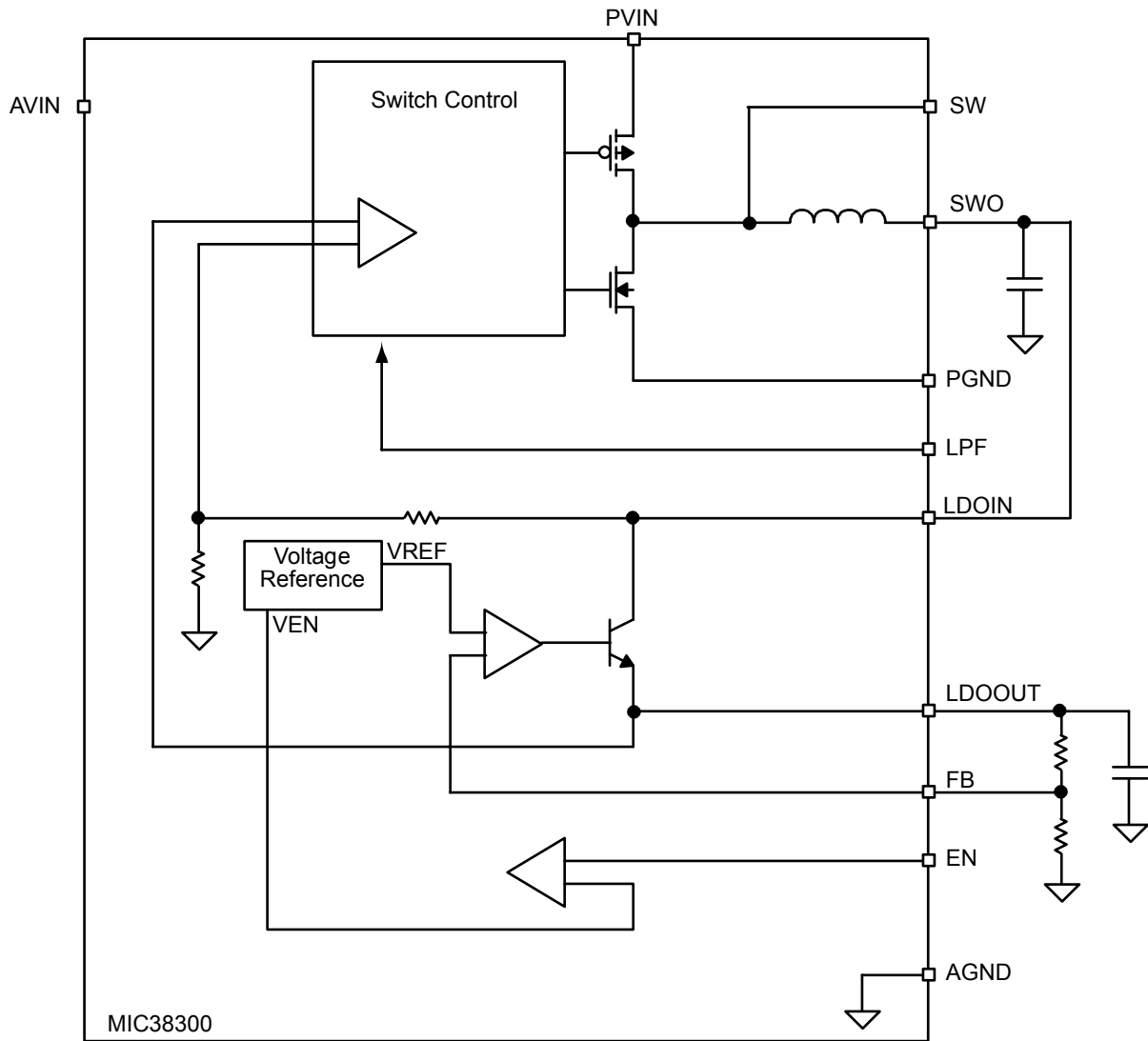
### Typical Application



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MLF and MicroLeadFrame are registered trademark of Amkor Technologies

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### Block Diagram

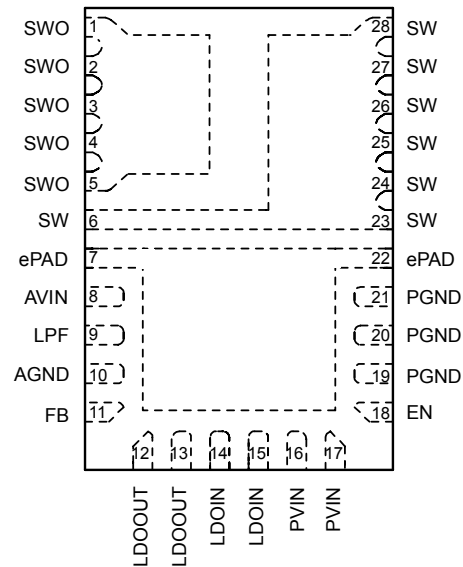


### Ordering Information

Part Number	Output Current	Voltage <sup>(1)</sup>	Junction Temperature Range	Package
MIC38300HYHL	3.0A	ADJ	-40°C to +125°C	PB-Free 28-Pin 4x6 MLF <sup>®</sup>

**Note:** For additional voltage options, contact Micrel.

## Pin Configuration



**28-Pin 4mm x 6mm MLF<sup>®</sup> (ML)**  
(Top View)

## Pin Description

Pin Number MIC38300HYHL	Pin Name	Pin Name
1, 2, 3, 4, 5	SWO	Switch (Output): This is the output of the PFM Switcher.
6, 23, 24, 25, 26, 27, 28	SW	Switch Node: Floating for typical applications. Attach external resistor from LPF to increase hysteretic frequency.
7, 22	ePAD	Exposed heat-sink pad. Recommend to connect to PGND.
8	AVIN	Analog Supply Voltage: Supply for the analog control circuitry. Requires bypass capacitor to ground.
9	LPF	Low Pass Filter: Floating for typical applications. Attach external resistor from SW to increase hysteretic frequency.
10	AGND	Analog Ground.
11	FB	Feedback: Input to the error amplifier. Connect to the external resistor divider network to set the output voltage.
12, 13	LDOOUT	LDO Output (Output): Output of voltage regulator. Place capacitor to ground to bypass the output voltage. Nominal bypass capacitor is 10 $\mu$ F.
14, 15	LDOIN	LDO Input: Connect to SW output. Requires a bypass capacitor to ground.
16, 17	PVIN	Input Supply Voltage (Input): Requires bypass capacitor to GND.
18	EN	Enable (Input): Logic low will shut down the device, reducing the quiescent current to less than 50 $\mu$ A. This pin can also be used as an under-voltage lockout function by connecting a resistor divider from EN/UVLO pin to VIN and GND.
19, 20, 21	PGND	Power Ground.

**Note:** Prefix **H** indicates  $V_{OUT} > 1V$ , prefix **L** indicates  $V_{OUT}$  is between 0.7V to 1V.

**Absolute Maximum Ratings<sup>(1)</sup>**

Supply Voltage ( $V_{IN}$ )	6V
Output Switch Voltage ( $V_{SW}$ )	6V
Output Switch Current ( $I_{SW}$ )	8A
LDO Output Voltage ( $V_{OUT}$ )	6V
Logic Input Voltage ( $V_{EN}, V_{LQ}$ )	$V_{IN}$ to $-0.3V$
Power Dissipation	Internally Limited <sup>(3)</sup>
Storage Temperature ( $T_S$ )	$-65^{\circ}C \leq T_J \leq +150^{\circ}C$
ESD Rating <sup>(4)</sup>	2kV

**Operating Ratings<sup>(2)</sup>**

Supply voltage ( $V_{IN}$ )	3.0V to 5.5V
Junction Temperature Range	$-40^{\circ}C \leq T_J \leq +125^{\circ}C$
Enable Input Voltage ( $V_{EN}$ )	0V to $V_{IN}$
Package Thermal Resistance	
4mm × 6mm MLF-28 ( $\theta_{JA}$ )	40°C/W

**Electrical Characteristics<sup>(5)</sup>**

$T_A = 25^{\circ}C$  with  $V_{IN} = V_{EN} = 5V$ ;  $V_{EN} = V_{IN}$ ;  $I_{OUT} = 10mA$ ,  $V_{OUT} = 1.8V$ . **Bold** values indicate  $-40^{\circ}C \leq T_J \leq +125^{\circ}C$ , unless noted.

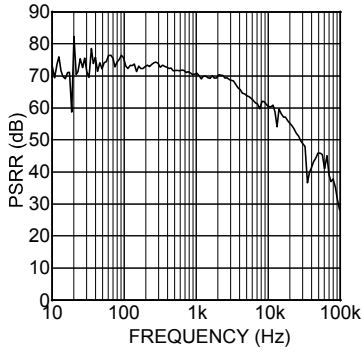
Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage Range		<b>3.0</b>		<b>5.5</b>	V
Under-Voltage Lockout Threshold	Turn-on		2.75		V
UVLO Hysteresis			100		mV
LDO Quiescent Current	$I_{OUT} = 0A$ ,		1		mA
Turn-on Time	$V_{OUT}$ to 5% of regulation, $I_{LOAD} = 3A$		200	350	$\mu s$
Shutdown Current	$V_{EN} = 0V$		35	<b>50</b>	$\mu A$
Feedback Voltage	$\pm 1\%$ $\pm 2.5\%$	0.99 <b>0.975</b>	1 1	1.01 <b>1.025</b>	V V
Feedback Current				1	$\mu A$
$V_{IN} - V_O$ ; Dropout Voltage	$I_{LOAD} = 3.0A$			<b>1.2</b>	V
Current Limit	$V_{FB} = 0.9 \times V_{NOM}$	4.5	6		A
Output Voltage Load Regulation	$V_{OUT} = 1.8V$ , 10mA to 3A		0.3	1	%
Output Voltage Line Regulation	$V_{OUT} = 1.8V$ , $V_{IN}$ from 3.0V to 5.5V		0.35	0.5	%/V
Output Ripple	$I_{LOAD} = 2A$ , $C_{OUTLDO} = 20\mu F$ , $C_{OUTSW} = 20\mu F$ LPF=25k $\Omega$		5		mV
Over-Temperature Shutdown			150		$^{\circ}C$
Over-Temperature Shutdown Hysteresis			20		$^{\circ}C$
<b>Enable Input</b>					
Enable Input Threshold	Regulator enable	<b>0.90</b>	1	<b>1.1</b>	V
Enable Hysteresis		<b>20</b>	120	<b>200</b>	mV
Enable Input Current			0.01		$\mu A$

**Notes:**

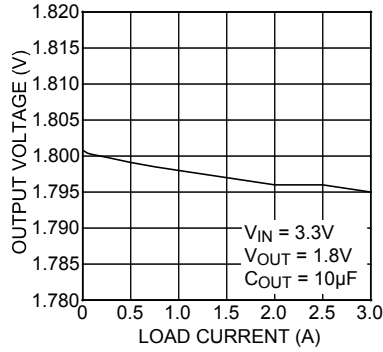
- Exceeding the absolute maximum rating may damage the device.
- The device is not guaranteed to function outside its operating rating.
- The maximum allowable power dissipation of any  $T_A$  (ambient temperature) is  $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
- Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
- Specification for packaged product only.

## Typical Characteristics

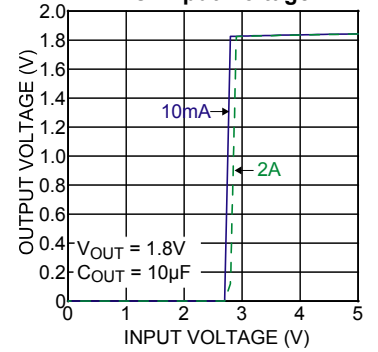
**MIC38300 PSRR**



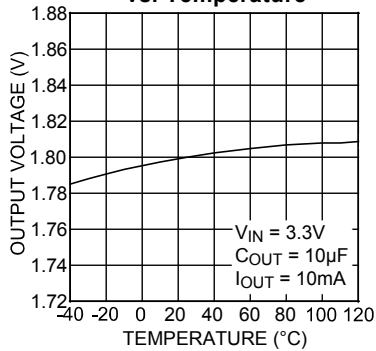
**Load Regulation**



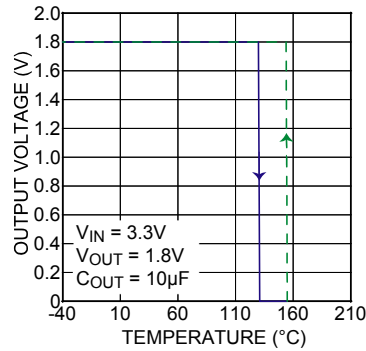
**Output Voltage vs. Input Voltage**



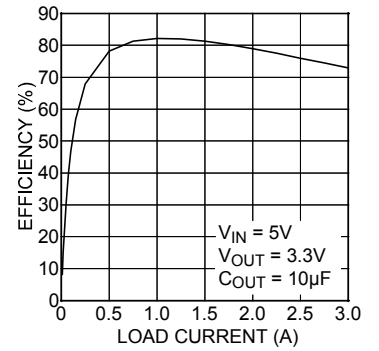
**Output Voltage vs. Temperature**



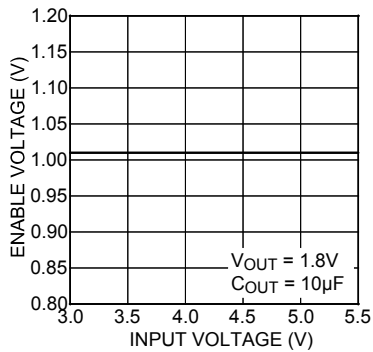
**Thermal Shutdown**



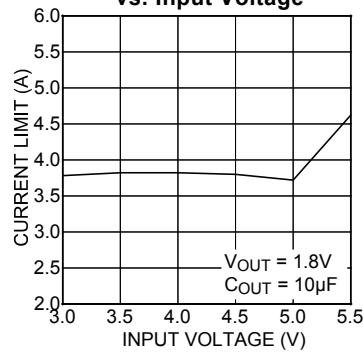
**MIC38300 Efficiency**



**Enable Threshold**



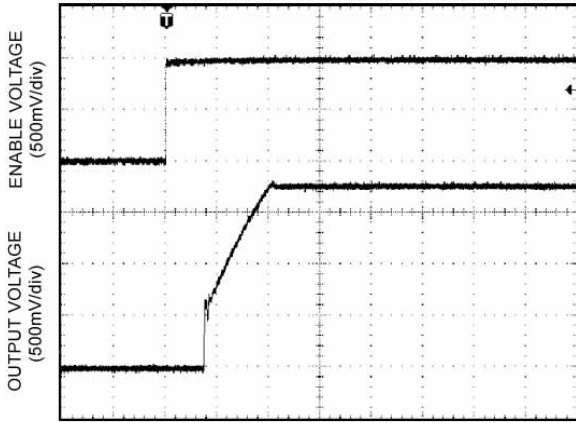
**Current Limit vs. Input Voltage**



### Functional Characteristics

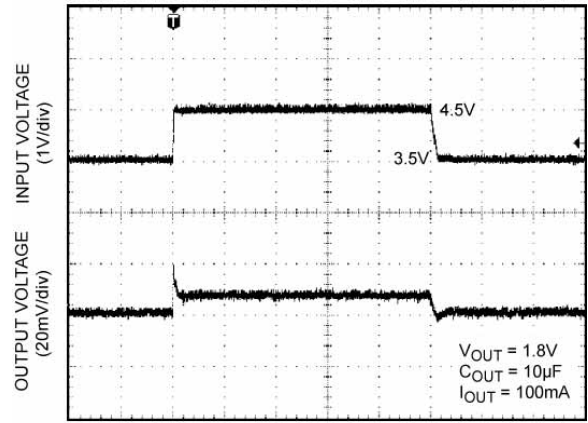
$V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  $C_{OUT} = 10\mu F$ , Inductor = 470nH

Enable Turn-On



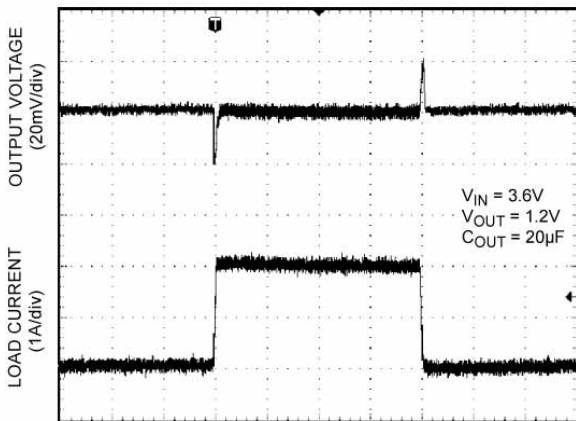
Time (100µs/div)

Line Transient



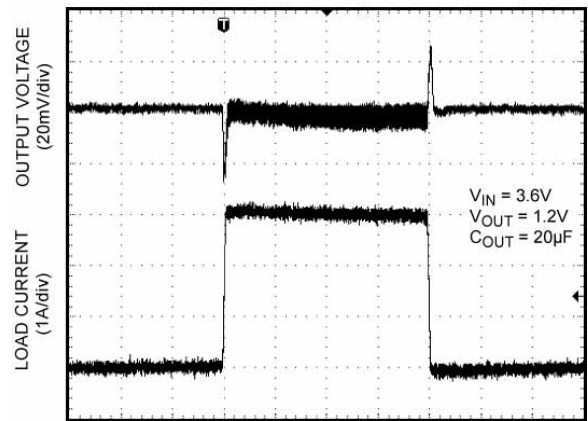
Time (200µs/div)

Load Transient 2A



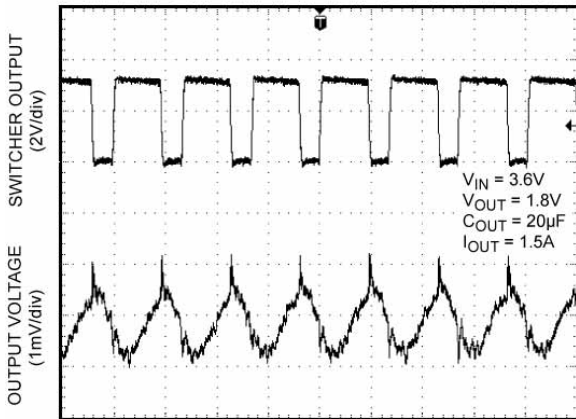
Time (100µs/div)

Load Transient 3A



Time (100µs/div)

Output Noise



Time (400ns/div)

## Application Information

### Enable Input

The MIC38300 features a TTL/CMOS compatible positive logic enable input for on/off control of the device. High enables the regulator while low disables the regulator. In shutdown the regulator consumes very little current (only a few microamperes of leakage). For simple applications the enable (EN) can be connected to  $V_{IN}$  (IN).

### Input Capacitor

$V_{IN}$  provides power to the MOSFETs for the switch mode regulator section, along with the current limiting sensing. Due to the high switching speeds, a  $10\mu\text{F}$  capacitor is recommended close to  $V_{IN}$  and the power ground (PGND) pin for bypassing.

Analog  $V_{IN}$  (AVIN) provides power to the analog supply circuitry. AVIN and  $V_{IN}$  must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by  $V_{IN}$  is reduced before reaching AVIN. A  $1\mu\text{F}$  capacitor as close to AVIN as possible is recommended.

### Output Capacitor

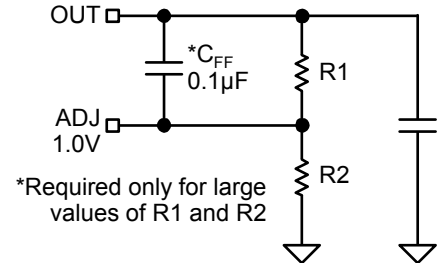
The MIC38300 requires an output capacitor for stable operation. As a  $\mu\text{Cap}$  LDO, the MIC38300 can operate with ceramic output capacitors of  $10\mu\text{F}$  or greater. Values of greater than  $10\mu\text{F}$  improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Larger output capacitances can be achieved by placing tantalum or aluminum electrolytics in parallel with the ceramic capacitor. For example, a  $100\mu\text{F}$  electrolytic in parallel with a  $10\mu\text{F}$  ceramic can provide the transient and high frequency noise performance of a  $100\mu\text{F}$  ceramic at a significantly lower cost. Specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

For less than 5mV noise performance at higher current loads,  $20\mu\text{F}$  capacitors are recommended at LDOIN and LDOOUT.

### Low Pass Filter Pin

The MIC38300 features a Low Pass Filter (LPF) pin for adjusting the switcher frequency. By tuning the frequency, the user can further improve output ripple without losing efficiency.

### Adjustable Regulator Design



#### Adjustable Regulator with Resistors

The adjustable MIC38300 output voltage can be programmed from 1V to 5.0V using a resistor divider from output to the SNS pin. Resistors can be quite large, up to  $100\text{k}\Omega$  because of the very high input impedance and low bias current of the sense amplifier. For large value resistors ( $>50\text{k}\Omega$ ) R1 should be bypassed by a small capacitor ( $C_{FF} = 0.1\mu\text{F}$  bypass capacitor) to avoid instability due to phase lag at the ADJ/SNS input.

The output resistor divider values are calculated by:

$$V_{OUT} = 1V \left( \frac{R1}{R2} + 1 \right)$$

### Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$\text{Efficiency} \text{ \%} = \left( \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of  $I^2R$ . Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET  $R_{DS(ON)}$  multiplied by the Switch Current<sup>2</sup>. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss.

Over  $100\text{mA}$ , efficiency loss is dominated by MOSFET  $R_{DS(ON)}$  and inductor losses. Higher input supply voltages will increase the Gate to Source threshold on the internal MOSFETs, reducing the internal  $R_{DS(ON)}$ . This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which

case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L\_P_D = I_{OUT}^2 \times DCR$$

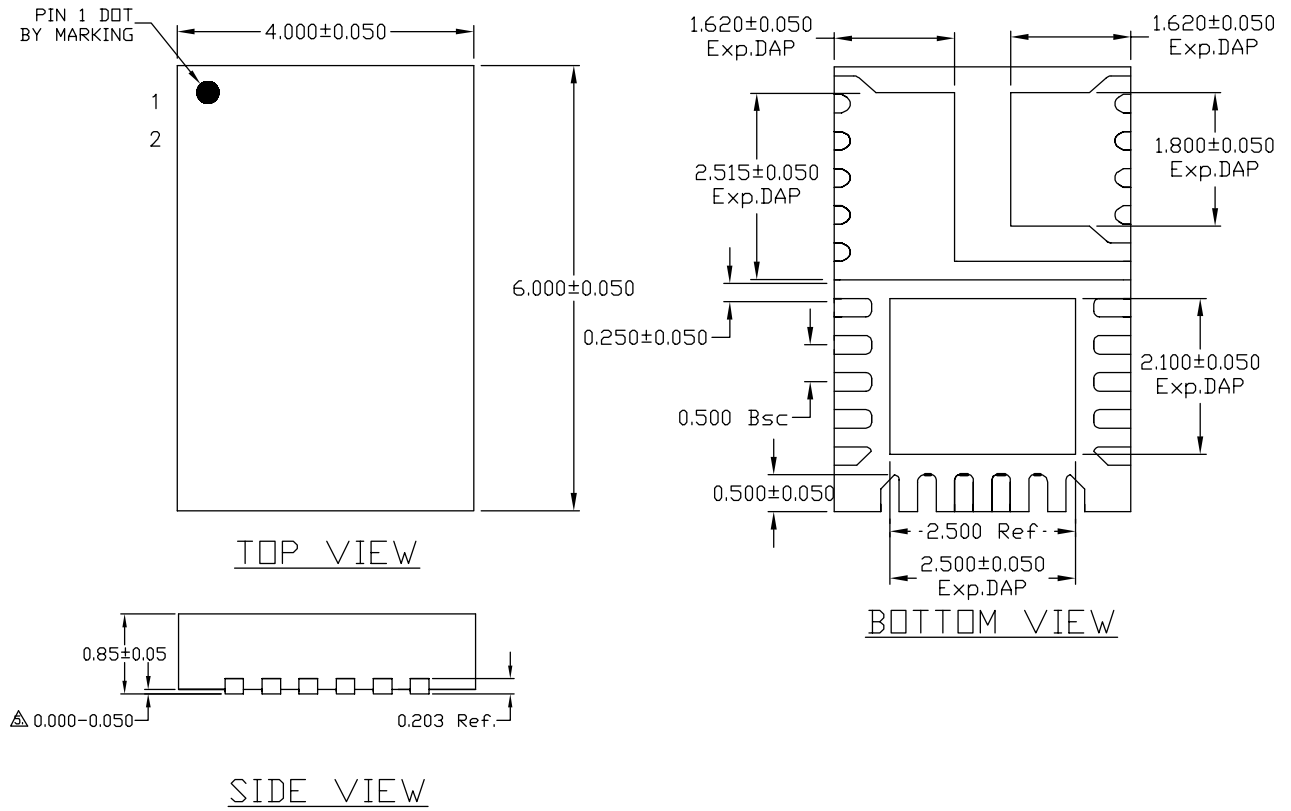
From that, the loss in efficiency due to inductor resistance can be calculated as follows;

$$Efficiency\_Loss = \left[ 1 - \left( \frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L\_P_D} \right) \right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.



**Package Information**

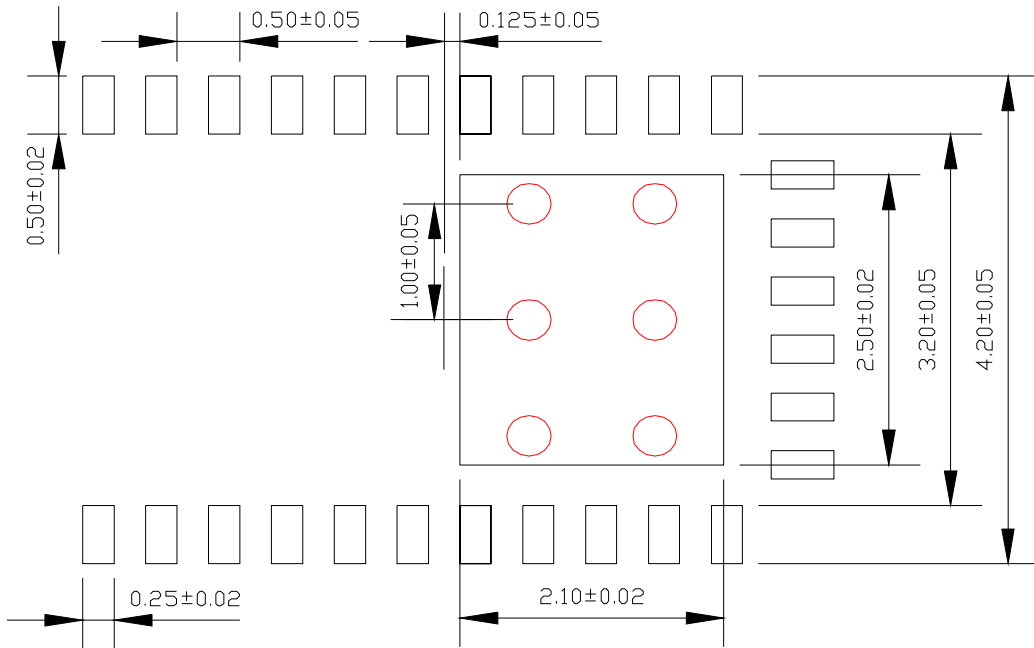


- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
  4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- $\Delta$  APPLIED ONLY FOR TERMINALS.

**28-Pin 4mm x 6mm MLF (ML)**

**Recommended Landing Pattern**

**LP # HMLF46T-28LD-LP-1**  
 All units are in mm  
 Tolerance  $\pm 0.05$  if not noted



Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter and it should be connected to GND plane for maximum thermal performance.

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