National Semiconductor

DP8482A 100k ECL to TTL Level Translator with Latch

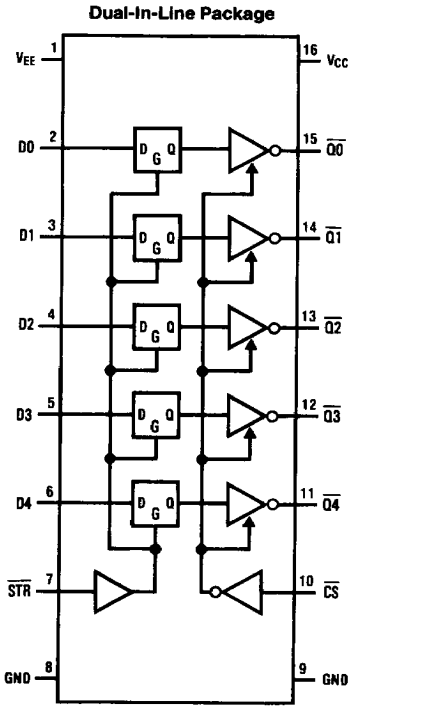
General Description

This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive standard 50 pF loads. The strobe and chip select inputs operate at ECL levels.

Features

- 16-pin DIP or S.O.
- TRI-STATE outputs
- ECL control inputs
- 8 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 100k ECL input compatible

Logic and Connection Diagram



Top View

Truth Table

D	$\overline{Q}$	$\overline{STR}$	$\overline{CS}$
H	L	L	L
L	H	L	L
X	$\overline{Q}$	H	L
X	Hi-Z	X	H

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8482AJ, DP8482AM or DP8482AN
See NS Package Number J16A, N16A or M16B

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage	GND to V_{EE}
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−4.5V ± 7%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 12 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = −10 mA	V_{CC} −2V			V
I_{AV}	Output Low Drive Current	Force 2.5V	70	150		mA
I_{OS}	Output High Drive Current	Force 0V	−70	−150	−350	mA
I_{OZ}	TRI-STATE Output Current		−50	1	+50	μA
I_{CC}	Supply Current				35	mA

Electrical Characteristics (ECL Logic) (Notes 2 and 3)

Symbol	Parameter	Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −4.5V		−1810		−1475	mV
V_{IH}	Input High Voltage	V_{EE} = −4.5V		−1165		−880	mV
I_{IL}	Input Low Current	V_{IN} = V_{IL} Max			50	100	μA
I_{IH}	Input High Current	V_{IN} = V_{IH} Max			75	750	μA
I_{EE}	Supply Current					−55	mA

Switching Characteristics (Notes 2 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD1}	Strobe to Output Delay	C_L = 50 pF	4	9	15	ns
t_{PD2}	Data to Output Delay	C_L = 50 pF	3.5	8	15	ns
t_S	Data Set-Up Time	(Note 6)	3.0	1.0		ns
t_H	Data Hold Time	(Note 6)	3.0	1.0		ns
t_{PW}	Strobe Pulse Width	(Note 6)	5.0	3.0		ns
t_{ZE}	Delay from Chip Select to Active State from Hi-Z State	C_L = 50 pF	6	15	25	ns
t_{EZ}	Delay from Chip Select to Hi-Z State from Active State	C_L = 50 pF	4.5	12	22	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for T_A = 25°C and nominal supply. Maximum propagation delays are specified with all outputs switching simultaneously.

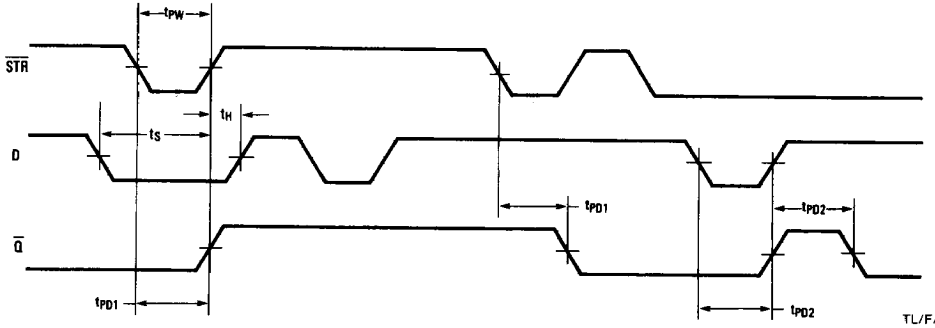
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: When DC testing I_{AV} or I_{OS}, only one output should be tested at a time and the current limited to 120 mA max.

Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 0.7 ns ± 0.1 ns from 20% to 80%.

Note 6: Caution should be used when latching data while the outputs are switching. TTL outputs generate severe ground noise when switching. This noise can be sufficient to cause the ECL latch to lose data. Board mounting and good supply decoupling are desirable. The worst case conditions are with all outputs switching low simultaneously, the maximum capacitive loading on the outputs and the maximum V_{CC} supply voltage applied.

Switching Time Waveforms



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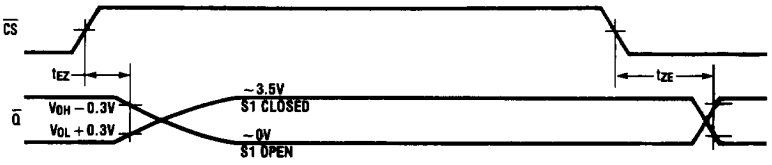
S1 open



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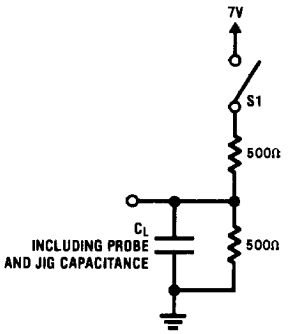
Test Load



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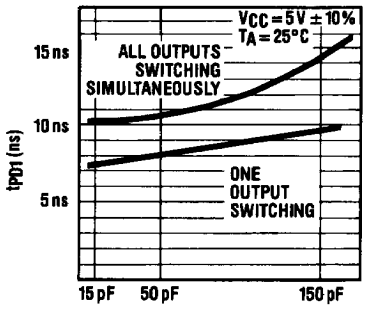
Typical Performance Versus C_L



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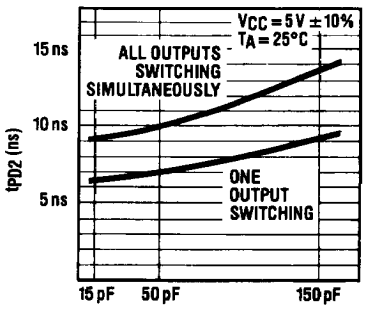

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