National Semiconductor

MICROCIRCUIT DATA SHEET

MNCLC400A-X REV 2A0

Original Creation Date: 11/24/98
Last Update Date: 03/09/99
Last Major Revision Date: 2/16/99

FAST SETTLING, WIDEBAND LOW-GAIN MONOLITHIC OP AMP

General Description

The CLC400 is a high-speed, fast-settling operational amplifier designed for low-gain applications. Constructed using a unique, proprietary design and an advanced complementary bipolar process, the CLC400 offers performance far beyond that normally offered by ordinary monolithic operational amplifiers. In addition, unlike many other high-speed operational amplifiers the CLC400 offers both high performance and stability without the need for compensation circuitry - even at a gain of +1.

The fast 12ns settling to 0.05% and its ability to drive capacitive loads makes the CLC400 an ideal flash A/D driver. The wide bandwidth of 200 MHz and the very linear phase ensure unsurpassed signal fidelity. Systems employing digital to analog converters also benefit from the use of the CLC400 - especially if linearity and drive levels are important to system performance.

The CLC400 provides a simple, high-performance solution for video distribution and line driving applications. The 50mA output current and guaranteed specifications for 100 ohm loads provide ample drive capability and assured performance.

Industry Part Number

CLC400A

NS Part Numbers

CLC400AE-QML*
CLC400AJ-MLS
CLC400AJ-QML**

Prime Die

UB1363B

Controlling Document

5962-8997001PA**, 2A*

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- -3dB bandwidth of 270MHz
- 0.05% settling in 12ns
- Low power, 150mW
- Low distortion, -60dBc at 20MHz
- Stable without compensation
- Overload and short circuit protection
- ±1 to ±8 closed-loop gain range

Applications

- Flash, precision A/D conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications
- Line drivers
- Video distribution
- High-speed communications

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (Vs)	±7V dc
Output Current (Iout)	±70mA
Maximum Power Dissipation (Pd) (Note 2)	1.2W
Junction Temperature (Tj)	+175 C
Storage Temperature Range	-65 C to +150 C
Lead Temperature (soldering, 10 seconds)	+300 C
Thermal Resistance	
Junction-to-ambient (ThetaJA)	
Ceramic DIP (Still Air)	134 C/W
Ceramic DIP (500 LFPM)	82 C/W
LCC (Still Air)	TBD
LCC (500 LFPM)	TBD
Junction-to-case (ThetaJC)	
Ceramic DIP	28 C/W
LCC	TBD
Package Weight (typical)	
Ceramic DIP	1070 mg
LCC	TBD
ESD Tolerance (Note 3)	
ESD Rating	1000 V

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Human body model, 100pF discharged through 1.5K Ohms.

Recommended Operating Conditions

Supply Voltage (Vs)	±5V dc
Closed Loop Gain Range	±1 to ±8
Ambient Operating Temperature Range (Ta)	-55 C to +125 C

Electrical Characteristics

DC PARAMETERS: Open Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5V dc. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (noninverting)	RS = 50Ohm			-20	+20	uA	1, 2
					-36	+36	uA	3
-Iin	Input Bias Current (Inverting)	RS = 50Ohm			-20	+20	uA	1
					-30	+30	uA	2
					-36	+36	uA	3
Vio	Input Offset Voltage	RS = 50Ohm			-5	5	mV	1
					-9	9	mV	2
					-8.2	8.2	mV	3
ROL	Transimpedance	TA = +25C	1		30		V/mA	1
IS	Supply Current	No Load				±23	mA	1, 2, 3
PSRR	Power Supply Rejection Ratio	+VS = +4.5V to +5.5V -VS = -4.5V to -5.5V			45		dB	1, 2, 3
+RIN	Input Resistance		1		100		kOhm	1, 2
			1		50		kOhm	3
Iout	Output Current		1		50		mA	1, 2
			1		355		mA	3
CMRR	Common Mode Rejection Ratio	VCM = ±2.0V	1		45		dB	1
		VCM = ±1.2V	1		45		dB	2, 3
Vout	Output Voltage Swing	No Load	1		2.8		V	1, 2
			1		2.3		V	3

Electrical Characteristics

AC PARAMETERS: Closed Loop Characteristics

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, Rf = 250 Ohms, Vs = ±5V dc, and Av = +2. -55 C ≤ Ta ≤ +125 C (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
SSBW	Small Signal Bandwidth	-3dB bandwidth, Vout < 0.5VPP			150		MHz	4
			2		120		MHz	5
			2		150		MHz	6
GFPL	Gain Flatness Peaking	.1 to 40 MHz				0.3	dB	4
			2			0.4	dB	5, 6
GFPH	Gain Flatness Peaking	No peaking over 40MHz				0.5	dB	4
			2			0.7	dB	5, 6
GFR	Gain Flatness Rolloff	.1 to 75 MHz				1.0	dB	4
			2			1.3	dB	5
			2			1.0	dB	6
HD2	2nd Harmonic Distortion	2 VPP at 20 MHz				-45	dB	4
			2			-45	dB	5
			2			-40	dB	6
HD3	3rd Harmonic Distortion	2 VPP at 20 MHz				-50	dB	4
			2			-50	dB	5, 6

AC PARAMETERS: Time Domain Response

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Rl = 100 Ohms, Rf = 250 Ohms, Vs = ±5V dc. -55 C ≤ Ta ≤ +125 C (Note 3)

SR	Slew Rate	Av= +2, measured ±1V with ±3V step	1		430		V/uS	9, 10, 11
TRS	Rise Time	0.5V Step	1			2.4	nS	9, 10, 11
TRL	Fall Time	5V Step	1			10	nS	9, 10, 11
TS	Settling Time	2V Step at 0.1% of fixed value	1			13	nS	9, 10, 11
		2V Step at 0.05% of fixed value	1			15	nS	9, 10, 11
OS	Overshoot	0.5V Step	1			10	%	9
			1			15	%	10, 11

Electrical Characteristics

DC PARAMETERS: Drift Values

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Rl = 100 Ohms, Vs = ±5V dc. -55 C ≤ Ta ≤ +125 C "Deltas not required on B-Level product. Deltas required for S-Level (-MLS) product as specified on Internal Processing Instructions (IPI)." (Note 3)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
+Iin	Input Bias Current (noninverting)	Rs = 50Ohm			-1.5	1.5	uA	1
-Iin	Input Bias Current (inverting)	Rs = 50Ohm			-1.5	1.5	uA	1
Vio	Input Offset Voltage	Rs = 50Ohms			-1.0	1.0	mV	1
IS	Supply Current	No Load			-2.0	2.0	mA	1

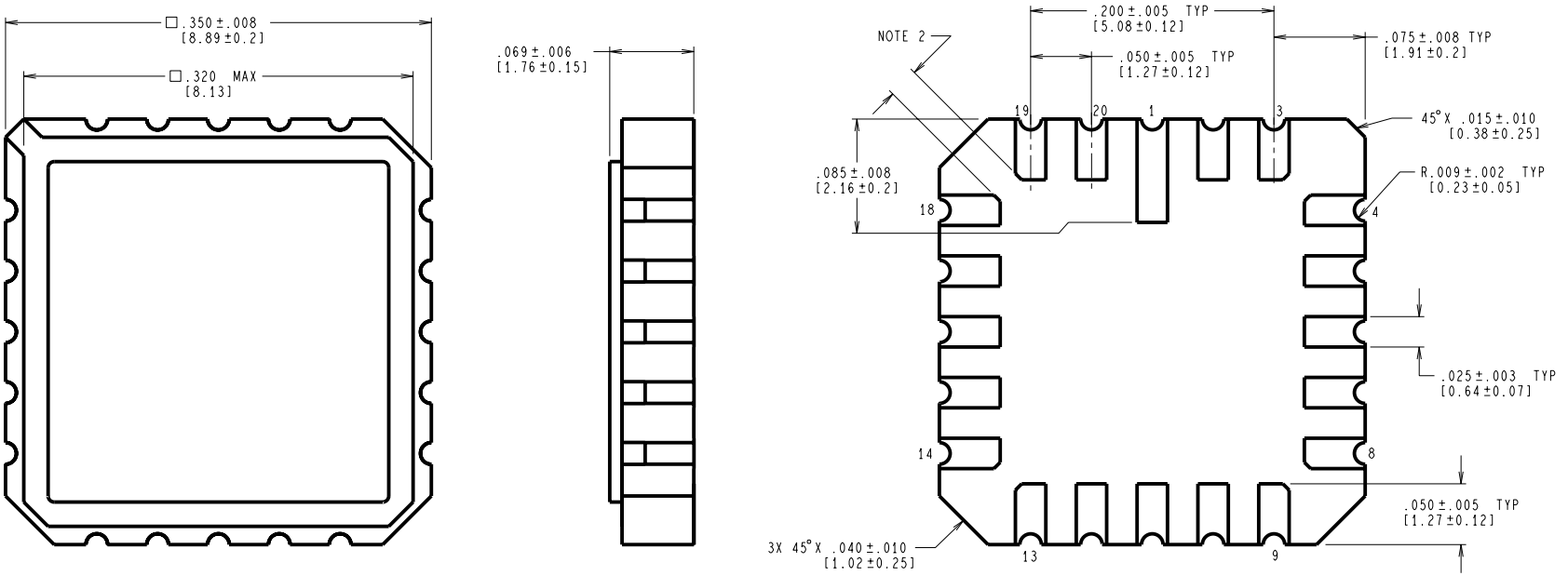
Note 1: If not tested, shall be guaranteed to the limits specified in Table 1
Note 2: Group A testing only.
Note 3: The algebraic convention, whereby the most negative value is a minimum and most positive is a maximum, is used in this table. Negative current shall be defined as convential current flow out of a device terminal.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
07081HRA3	CERDIP (J), 8 LEAD (B/I CKT)
07086HRA2	LCC (E), TYPE C, 20 TERMINAL (B/I CKT)
E20ARE	LCC (E), TYPE C, 20 TERMINAL(P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000427A	CERDIP (J), 8 LEAD (PINOUT)
P000445A	LCC (E), TYPE C, 20 TERMINAL (PINOUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
E	REVISE AND REDRAW.	10005	02/10/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/12.7 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CB, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/10/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH [MM]

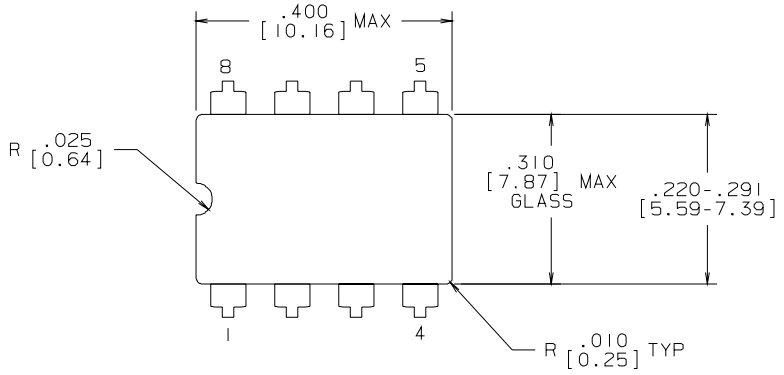
NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

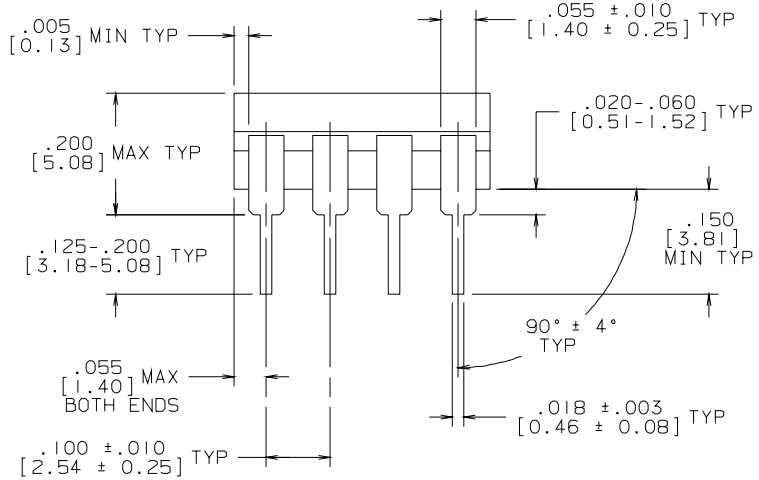
LEADLESS CHIP CARRIER, TYPE C, 20 TERMINAL

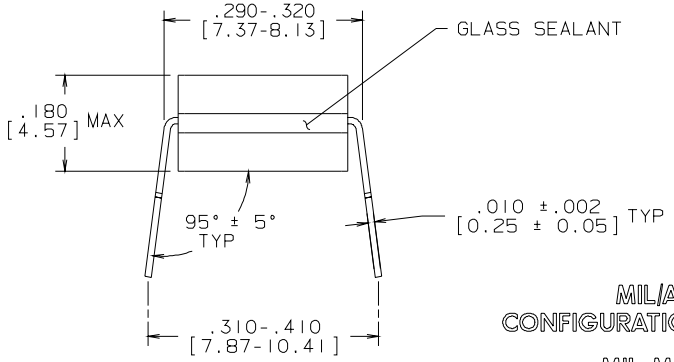
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E20A	E

DO NOT SCALE DRAWING | SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

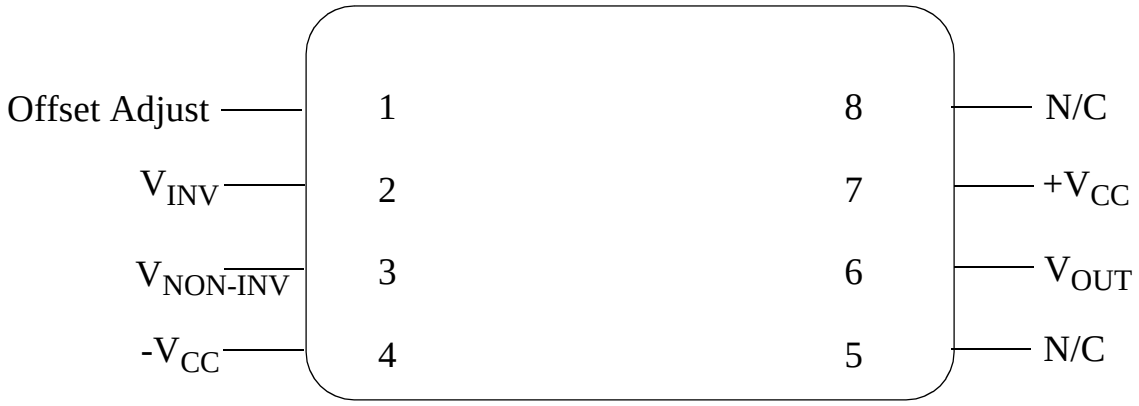
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



CLC400J

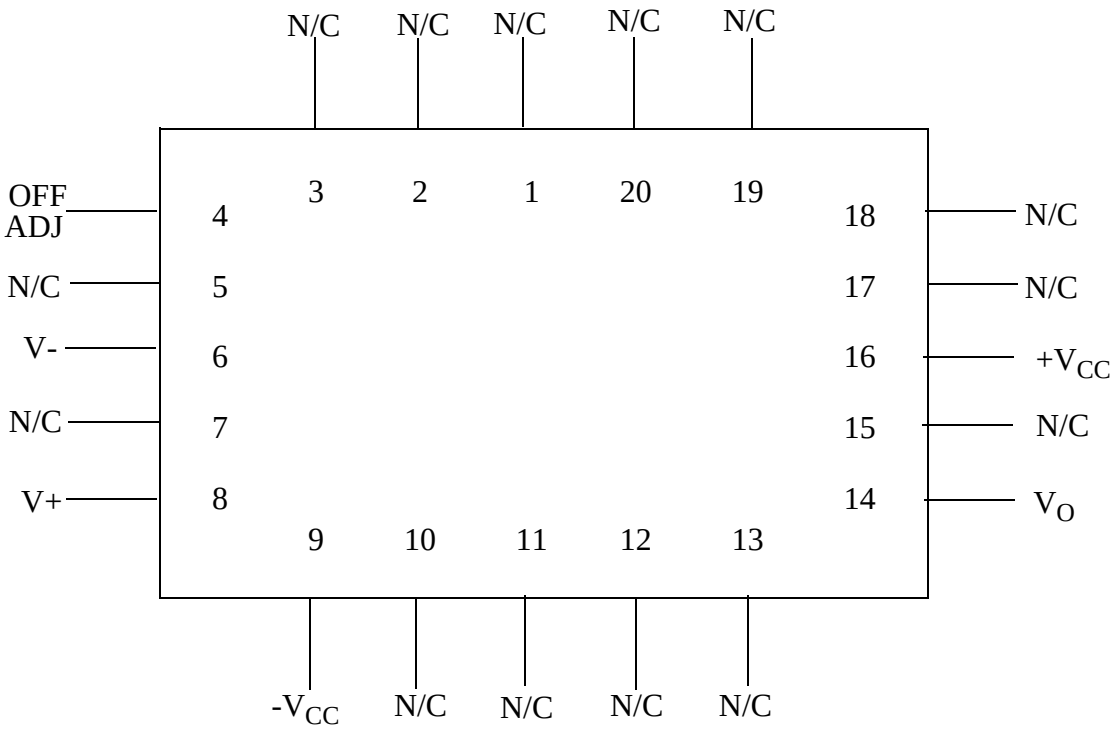
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000427A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



CLC400E
20 - LEAD LCC
CONNECTION DIAGRAM
TOP VIEW
P000445A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003157	02/18/99	Shaw Mead	Initial MDS Release
1A0	M0003241	03/09/99	Shaw Mead	Thermal data for Ceramic DIP added. Package weight for Ceramic DIP added. Gain Range in Recommended Op. Cond. corrected. CMRR subgroups corrected. Closed loop gain in AC conditions corrected. Rf = 250 Ohms added to AC conditions.
2A0	M0003273	03/09/99	Shaw Mead	Processing and QCI document reference added. Conditions for SR added.