



aptek microsystems

AMS 2039/2040/2041/2042

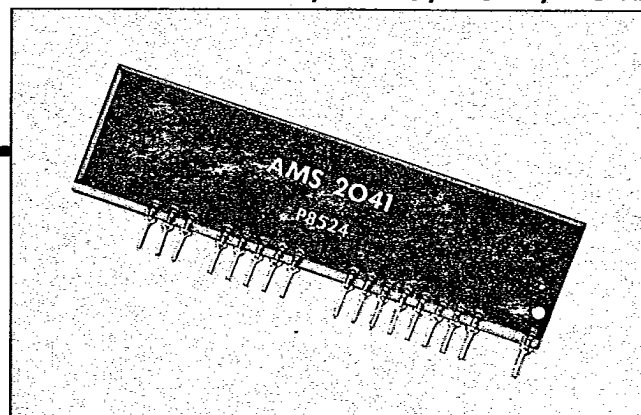
Reverse Line Interface Circuits

DESCRIPTION

The Reverse Line Interface Circuit (RLIC) is a device that allows the user to terminate a telephone line from a telephone Central Office (CO) or Private Branch Exchange (PBX) for the purpose of connecting auxiliary equipment that adds features or changes transmission methods. The RLIC must be located where it shares a common ground with the CO or PBX.

FEATURES

- Terminates the telephone line with proper AC impedance
- Draws correct loop current for DC termination
- Performs hybrid function; i.e., speech from CO/PBX appears on transmit output, speech to CO/PBX is inserted at receive input
- Provides for detection of Ringing and Battery Reversal
- Provides loop seizure
- Passes dial pulses with minimum distortion



BLOCK DIAGRAM

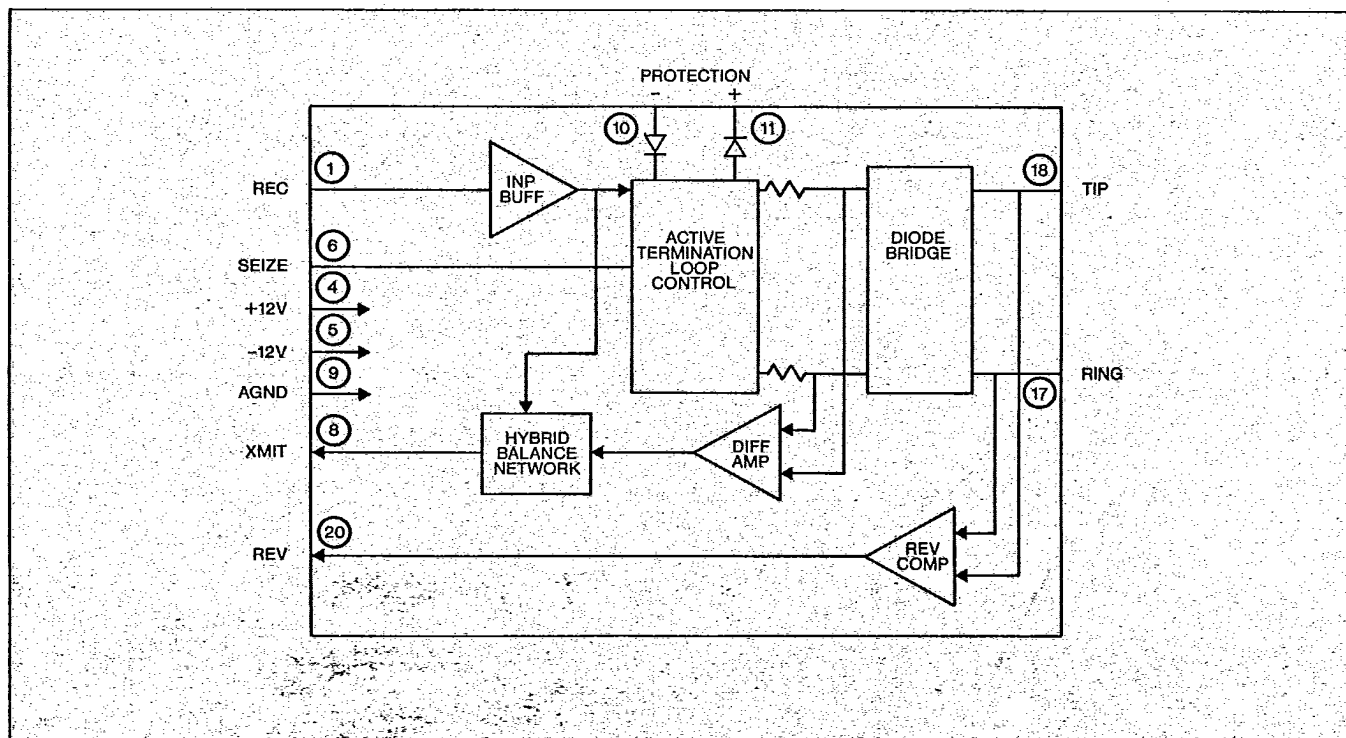


Figure 1. RLIC Block Diagram

AMS 2039/2040/2041/2042

Overview

In operation, the RLIC assumes the various roles of a telephone set; that is, it generates an off-hook or loop seizure, provides an active termination, provides two-to-four wire conversion and passes dial pulses with minimal distortion. Additionally, the RLIC detects a supervisory condition by the presence of reverse battery on tip and ring; i.e., ring more positive than tip. When ringing is present, the RLIC provides a logic level representation of the ring signal at the REVERSE output.

Theory of Operation

Figure 1 shows a block diagram of the RLIC. It consists of a receive buffer, diode bridge, active termination, reverse battery comparator, differential amplifier and hybrid network. Tip and ring are connected to the reverse battery comparator which will produce a high-level signal when ring is more positive than tip. This comparator includes sufficient hysteresis to produce a clean output during reverse battery transitions.

The tip and ring connections go through a diode bridge that guarantees that current will flow through the active termination in only one direction. At the output of the diode bridge, a differential amplifier detects analog audio signals present across the active termination. The output of this differential amplifier is connected to the hybrid network.

Within the hybrid balance network, the signals from receive and the differential amplifier are combined with an analog of the assumed termination impedance, such that when tip and ring are terminated in this impedance, any signal appearing across the active termination due to a signal on receive is removed from the transmit output. This effectively performs the two-to-four wire conversion function.

The active termination performs two functions. When the SEIZE input is low, the active termination presents a high impedance between tip and ring, blocking current flow. When SEIZE is at a high logic level, the active termination presents an impedance of 600/900 Ohms between tip and ring and controls the current to 25mA. In this state, an AC signal present at the receive input is transformed into a modulating current in the active termination such

that the voltage gain from the receive input to tip and ring is unity when tip and ring are terminated by 600/900 Ohms. The gain through the differential amplifier and hybrid balance network is likewise set at unity.

2039, 2040, 2041, 2042

The differences between the 2039, 2040, 2041 and 2042 are outlined in the table below.

Part Type	Internal Hybrid Balance Network	Tip-Ring Impedance
2039	900 ohm	900 ohm
2040	900 ohm + 2 μ F	900 ohm
2041	600 ohm	600 ohm
2042	600 ohm + 2 μ F	600 ohm

Transient Protection

For those applications where the TIP and RING terminals are subject to high transient surges, protection for the RLIC is provided through Pins 10 and 11 (see Figure 2). For additional information on transient protection, please contact the factory.

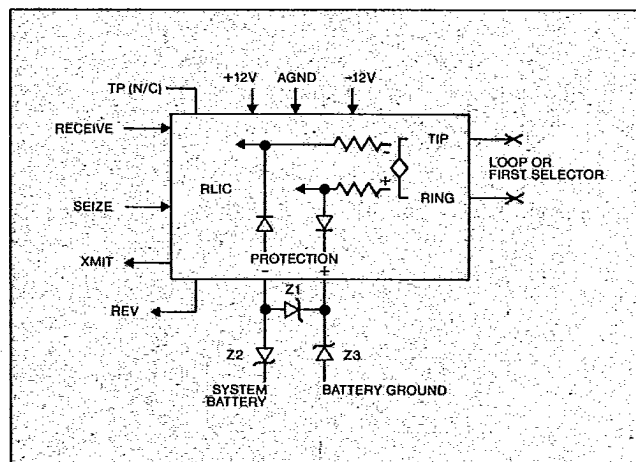


Figure 2.

Protection Level	Normal Switching Transients	Lightning - Induced Surges
Z ₁ Device (Metallic)	Open	200V Mov or 200V Transzorb or 200V ZENER
Z ₂ , Z ₃ (Longitudinal)	200 V ZENER	200 V ZENER

Select devices for peak power commensurate with peak surge voltage and application diagram, above.

AMS 2039/2040/2041/2042

Electrical Characteristics

All performance specifications are at $\pm 12\text{VDC}$ and -50VDC over a temperature range of 0°C to $+70^\circ\text{C}$ unless otherwise specified.
AC parameters from 300Hz to 3400 Hz.

Parameter	Conditions	Minimum	Maximum	Units
Gain - Receive to Tip-Ring	Appropriate 600/900 ohm Termination Tip-Ring	-2	+2	dB
Gain - Tip-Ring to XMIT	Appropriate Tip-Ring Impedance	-2	+2	dB
Max Signal Level No Clipping	XMIT or Receive		1.37	Volts RMS
Impedance	2039, 2040 2041, 2042	850 570	950 630	Ω
Dial Pulse Distortion		-2.0	+2.0	mS
Trans Hybrid Loss	Receive Input to XMIT Output. Appropriate Termination on Tip and Ring	35		dB
Loop Current	Loop Resistance Less Than 500 ohms $V_{\text{BATT}} = 50$	23	27	mA
Common Mode Tolerance	RLIC Ground to Battery Ground	12		Volts
Longitudinal to Metallic Balance		60		dB
Power Supply Rejection	± 12 Volt Supplies Receive Pin Grounded 300 - 3400 Hz	30		dB
Supply Current	± 12 Volt Supplies		10	mA
V_{IH}	Seize Pin	2.0		Volts
V_{IL}	Seize Pin		.8	Volts
V_{OH}	Reverse Pin ($I_{\text{SOURCE}} = 400\mu\text{A}$)	2.4		Volts
V_{OL}	Reverse Pin ($I_{\text{LOAD}} = 1.6\text{mA}$)		.4	Volts
Input Impedance Receive		450	500	k Ω
Longitudinal Impedance T and R to Ground		100		k Ω
Output Impedance XMIT			200	Ω
XMIT Peak Voltage		-6	+6	VDC
Seize Pin Currents	Logic Low: I_{SINK} Logic High: I_{SOURCE}		200 100	μA μA
Supply Voltage +12 -12		+10.8 -13.2	+13.2 -10.8	VDC VDC

3

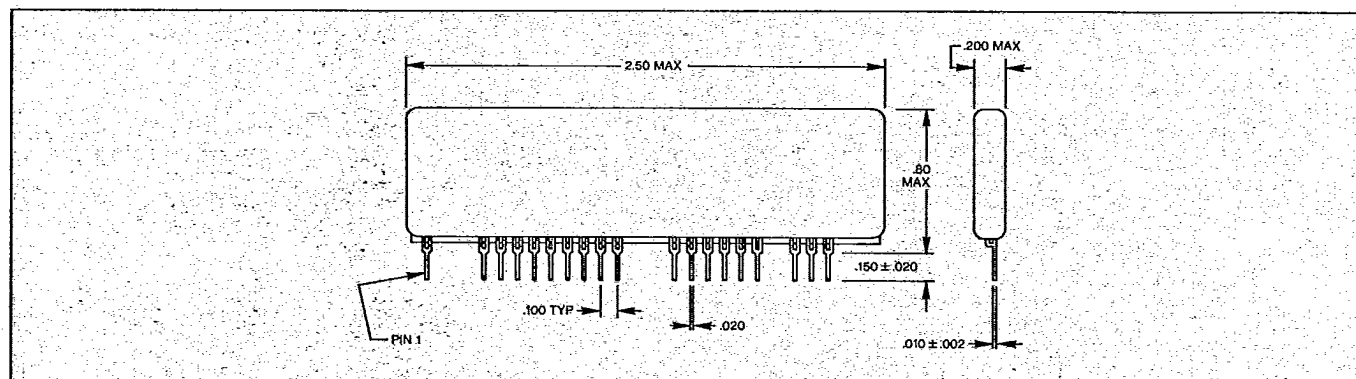
AMS 2039/2040/2041/2042

Pin Description

Pin#	Signals	Description
1	Receive	Analog input pin, input impedance is 470K ohms.
6	Seize	A TTL compatible input which when at a high level allows current to flow between tip & ring.
8	XMIT	The analog output corresponding to the signal appearing at tip & ring. The loss from receive input to XMIT will be at least 35dB when tip & ring look into the appropriate source impedance.
20	Reverse	A supervisory output which is high when tip & ring have reverse battery. This signal will be low when tip & ring are in their normal state; i.e., tip more positive than ring. Ringing may be detected by monitoring this pin.
18 17	Tip and Ring	These inputs have protection against normal transient conditions but should be further protected by 250V transient absorbers, such as GE MOV varistors.

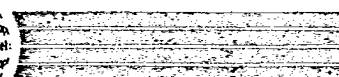
Pin#	Signals	Description
7	TP	Test point, connected to the internal balance network.
4	+12 Volts	Positive supply voltage.
5	-12 Volts	Negative supply voltage.
9	Analog Ground	Analog reference signal. There must be a metallic connection between this pin and CO/PBX battery ground.
10 11	Protection - Protection +	These are part of the transient protection circuitry & should be returned to CO/PBX battery & ground through protective devices (see Figure 2).
14	AG	Internally tied to Pin 9
15	-12 Volts	Internally tied to Pin 5
16	+12 Volts	Internally tied to Pin 4
21	Tip	Internally tied to Pin 18
22	Ring	Internally tied to Pin 17

PACKAGE DESCRIPTION



For more information contact: Aptek Microsystems, 700 N.W. 12th Avenue, Deerfield Beach, Florida 33441. (305) 421-8450 TLX 441020

Information furnished by Aptek Microsystems is believed to be accurate and reliable. However, no responsibility is assumed by Aptek Microsystems for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Aptek Microsystems. Aptek Microsystems reserves the right to make changes at any time and without notice.



aptek microsystems