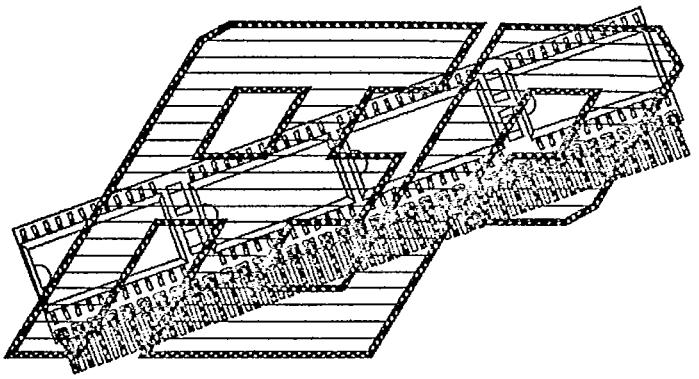
T-46-07-27

- >> *32 bit high speed parallel and serial scan register.*
- >> *High density .070 center spaced ZIP leads for maximum I/O in minimum area.*
- >> *Space saving vertical mounting orientation.*
- >> *Convenient "in one side, out the other" broadside pin-out.*
- >> *TTL compatible*
- >> *Uses single +5V power supply*



32 LINE SCAN REGISTER MODULE

DESCRIPTION:

The AEPSRZ32 is a high speed, high density 32-line scan register module ideal for use with 16 or 32-bit wide data paths or Writable Control Store (WCS) sub-systems. It combines the advantages of the 818 type diagnostic scan register ICs with very large data widths and a board-space saving configuration. The vertical mounting orientation and compact I/O pin footprint make it superb for projects with tight space constraints.

Physically the module consists of an FR4 PC material substrate mounted with four 818 type octal register ICs, four 0.10 microfarad decoupling capacitors, and 75 I/O pins in a staggered ZIP package format. It can be ordered with any 818 type register made by any manufacturer producing them in a 24 pin SOP package.

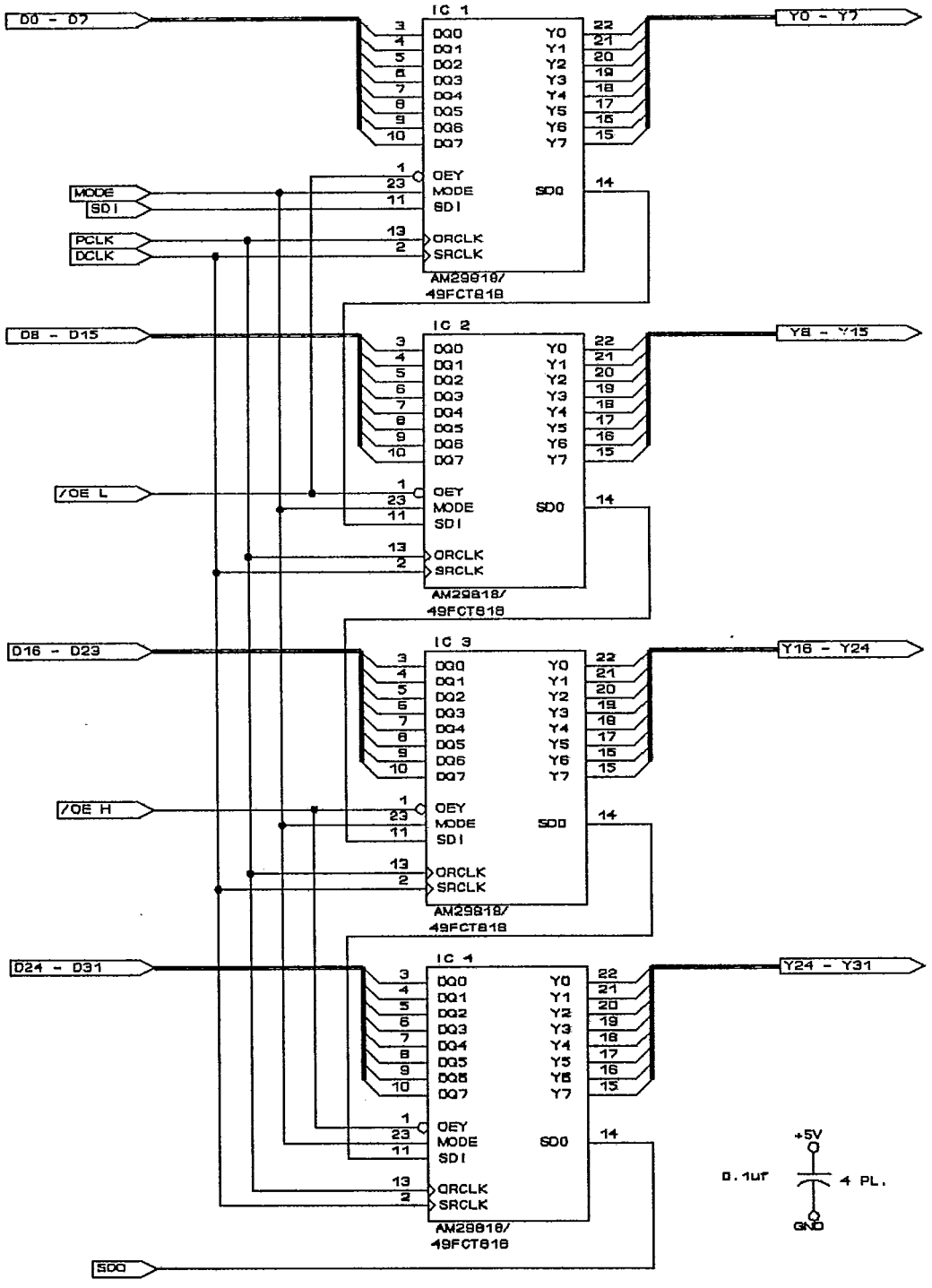
The module control lines are configured as follows: the parallel clock (PCLK), the serial clock (DCLK) and the MODE switch are connected in common to all four ICs. The active LOW output enables ($\overline{OEY}$ and $\overline{OEY_H}$) control 16 parallel lines each. The ICs' serial inputs (SDI) and outputs (SDO) are interconnected to form a 32 bit right-shift register using DCLK. Expansion to word widths greater than 32 bits is possible with additional modules.

Performance specifications, function tables, and electrical characteristics are determined by the particular IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors' data sheets, like those attached, or from their data books.

Mechanical dimensions are 0.505 inch high by 2.66 inches long by 0.22 inch wide. The I/O pins are in two rows which are 0.1 inch apart and offset longitudinally 0.035 inch. In each row the pins are on 0.070 inch center spacing. See included specification drawing.

32 LINE SCAN REGISTER MODULE
AEPSRZ32
FUNCTIONAL DIAGRAM

T-46-07-27



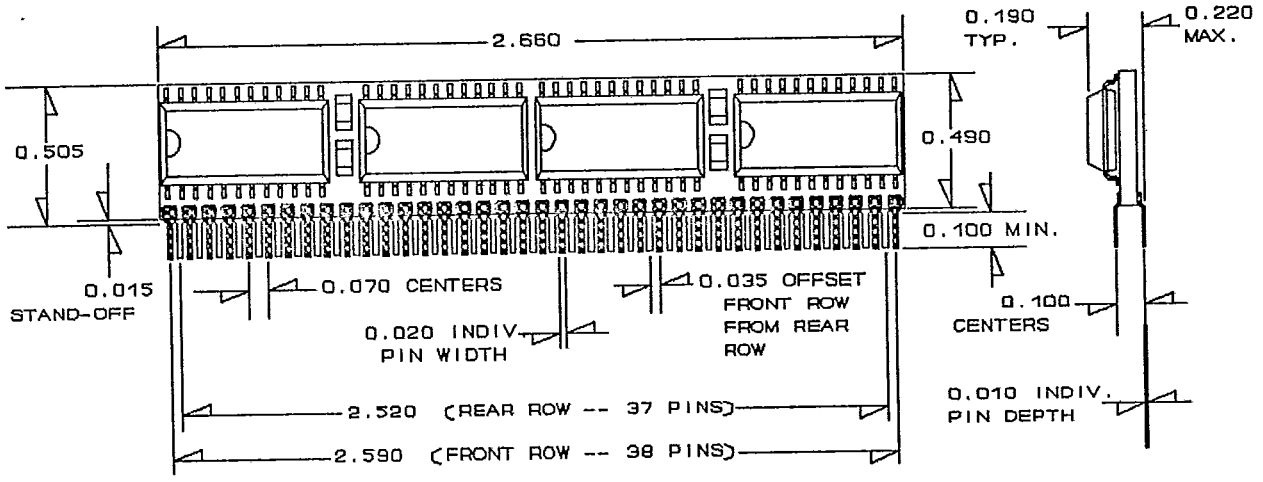
T-90-20

AEP 32 LINE MODULE SERIES PACKAGING INFORMATION

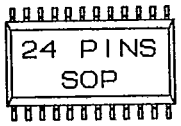
SPECIFICATION DRAWING

APPLY TO: BZ, LZ, RZ, TZ, SRZ, TRZ, CZ

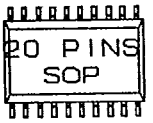
DIMENSIONS IN INCHES, TOLERANCE: +/- 0.010 UNLESS SPECIFIED.



75 PINS TOTAL

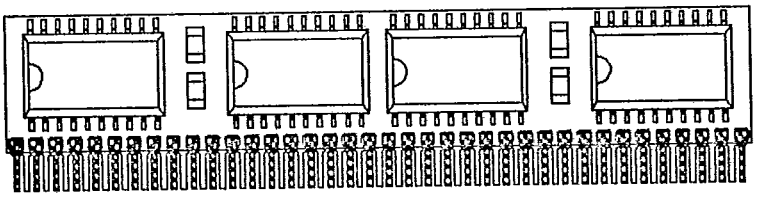


IC FOR LZ
RZ
SRZ
TRZ



IC FOR BZ
CZ
TZ

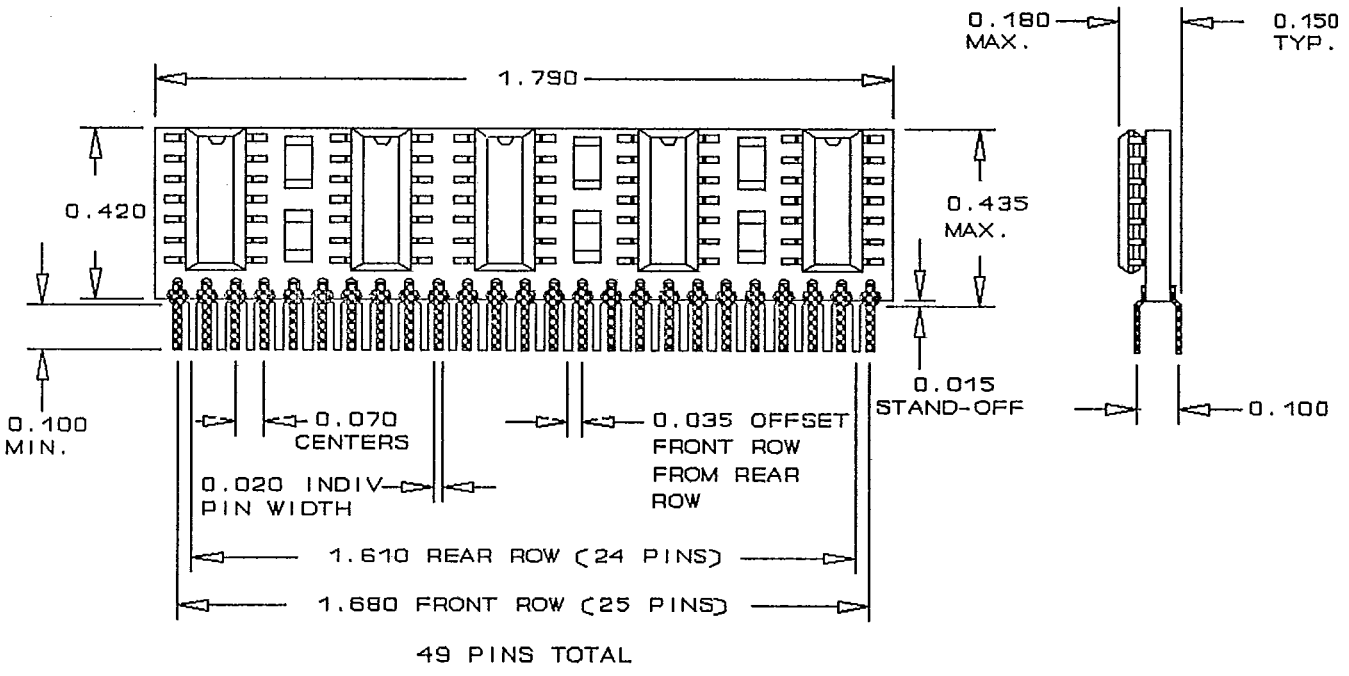
** MODULE DIMENSIONS REMAIN UNCHANGE.



AEP 32 LINE SUPPORT MODULE SERIES
PARITY GENERATOR/CHECKER
PACKAGING INFORMATION

APPLY TO: PZ-286, PZ-280

DIMENSIONS IN INCHES, TOLERANCE: +/- 0.010 UNLESS SPECIFIED.



The AEPPZ32-280 uses only one pull up resistor and 3 capacitors.
The AEPPZ32-286 uses three pull up resistors and 3 capacitors.