

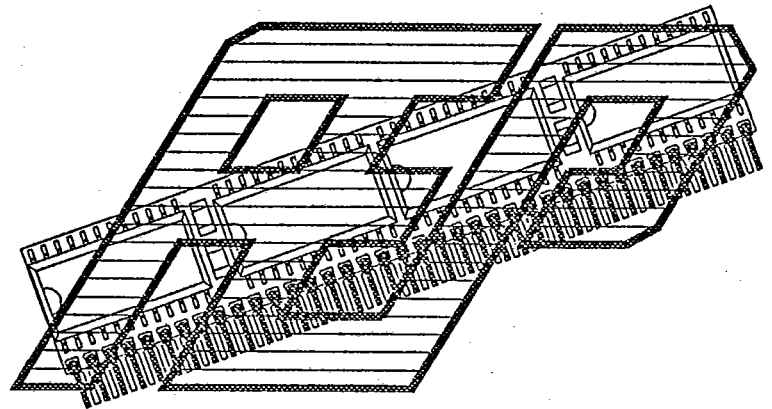
July 31, 1990

AEPRZ32

32 LINE REGISTER MODULE

T-52-09

- >> 32 bit bus interface register,
non-inverting or inverting.
- >> High density .070 center
spaced ZIP leads for maximum
I/O in minimum area.
- >> Space saving vertical
mounting orientation.
- >> Convenient "in one side, out
the other" broadside pin-out.
- >> TTL compatible
- >> Uses single +5V power supply



32 LINE REGISTER MODULE

DESCRIPTION:

The AEPRZ32 is a high speed, high density 32-line register module ideal for use with 16 or 32-bit wide address/data paths or buses. It combines the advantages of the 825 (non-inverting) or 826 (inverting) type buffered register ICs with very large data widths and a board-space saving configuration. The vertical mounting orientation and compact I/O pin footprint make it superb for projects with tight space constraints.

Physically the module consists of an FR4 PC material substrate mounted with four 825 or 826 type register ICs, four 0.10 microfarad decoupling capacitors, and 75 I/O pins in a staggered ZIP package format. It can be ordered with any 825 or 826 type register made by any manufacturer producing them in a 24 pin SOP package. The module features two Clock Enables, EN, and two Output Enables, OE, controlling two sets of sixteen outputs. An overall Output Enable, a Master Reset and a Clock Input are also used. All control signals except the Clock input are active LOW.

Performance specifications and electrical characteristics are determined by the IC devices used. These items can vary according to the type and manufacturer of the components. The necessary information is obtained from the IC vendors' data sheets, like those attached, or from their data books.

Mechanical dimensions are 0.505 inch high by 2.66 inches long by 0.22 inch wide. The I/O pins are in two rows which are 0.1 inch apart and offset longitudinally 0.035 inch. In each row the pins are on 0.070 inch center spacing. See included specification drawing.

The AEPRZ32 is one of a family of digital circuit support function modules which includes a 32 line buffer, a 32 line transceiver, and a 32 line latch module. These are natural companions for AEP memory modules.

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PART NUMBERING CHART

RZ32 with non-inverting 74F825 register	AEPRZ32-F825
74FCT825 register	AEPRZ32-FCT825
74LS825 register	AEPRZ32-LS825
RZ32 with inverting 74F826 register	AEPRZ32-F826
74FCT826 register	AEPRZ32-FCT826
74LS826 register	AEPRZ32-LS826

Register notes:

The standard register used is the 74F825. Please contact AEP if a type that is not listed above is desired. If the pin out configuration is the same as the 74F825 or 74F826 and the desired type is available in a standard 24 pin SOP, there should be no problem using it on the module.

The "/A" at the end of the standard IC number is a "High Performance" speed indicator. AEP may use the "A" version of a device even if it is not explicitly specified unless requested not to. An exact specification (type and manufacturer) of the IC device desired is recommended. Please contact AEP for assistance if needed.

Vendor notes:

The IC device specification information included is typical and does not limit AEP to that vendor. The actual devices used will be equivalent depending on price, availability, and customer requirements. AEP will gladly use or exclude particular manufacturers upon request. However, this might affect module price.

Disclaimers:

The information in this document has been carefully checked and is believed to be reliable. However, Advanced Electronic Packaging Inc. assumes no responsibility for inaccuracies. AEP also reserves the right to change products or specifications without notice.

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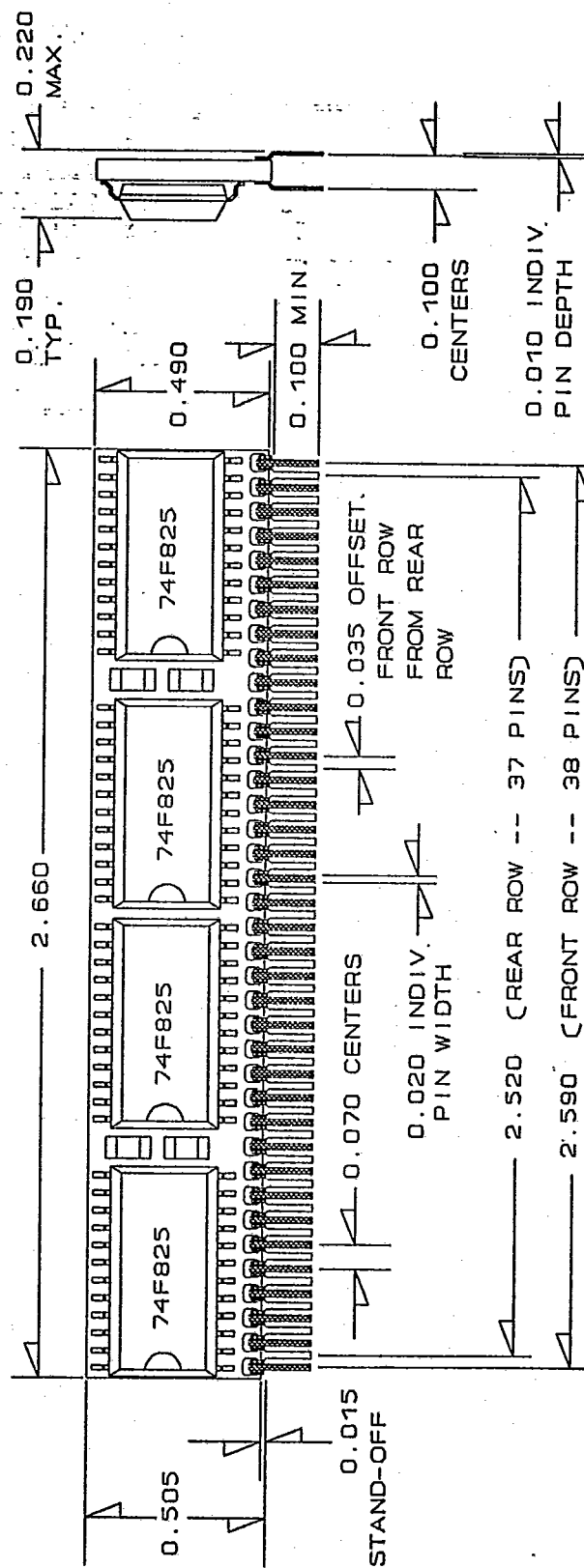
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AEPRZ32-825

32 LINE REGISTER MODULE

2-13-89

DIMENSIONS IN INCHES, TOLERANCE: ± 0.010 UNLESS SPECIFIED.

75 PINS TOTAL

E.S.



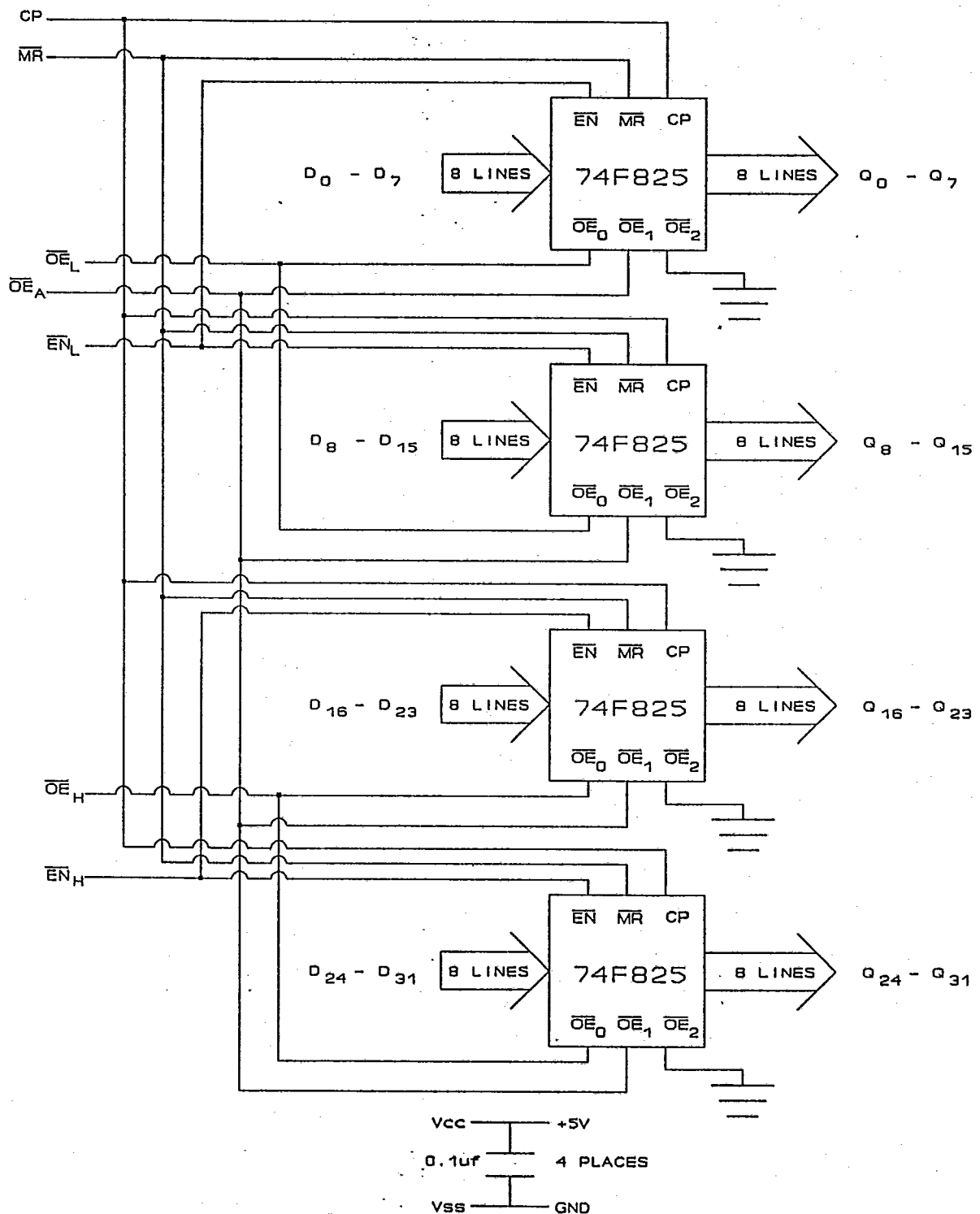
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32 LINE REGISTER MODULE FUNCTIONAL DIAGRAM


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26E D ■ 0254793 0000282 3 ■

AEPRZ32

32 LINE REGISTER MODULE

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32 LINE REGISTER MODULE PIN CONFIGURATION (TOP VIEW)

	PIN #s	
(DATA INPUTS)	D ₀ - 1	2 - Q ₀ (DATA OUTPUTS)
	D ₁ - 3	4 - Q ₁
	D ₂ - 5	6 - Q ₂
	D ₃ - 7	8 - Q ₃
	D ₄ - 9	10 - Q ₄
	D ₅ - 11	12 - Q ₅
	D ₆ - 13	14 - Q ₆
	D ₇ - 15	16 - Q ₇
(ENABLE _{LOW} *)	EN _L - 17	18 - OE _A (OUTPUT ENABLE _{ALL} *)
(OUTPUT ENABLE _{LOW} *)	OE _L - 19	(GROUND)
(DATA INPUTS)	D ₈ - 21	22 - Q ₈ (DATA OUTPUTS)
	D ₉ - 23	24 - Q ₉
	D ₁₀ - 25	26 - Q ₁₀
	D ₁₁ - 27	28 - Q ₁₁
	D ₁₂ - 29	30 - Q ₁₂
	D ₁₃ - 31	32 - Q ₁₃
	D ₁₄ - 33	34 - Q ₁₄
	D ₁₅ - 35	36 - Q ₁₅
(POWER)	V _{CC} - 37	38 - V _{CC} (POWER)
(DATA INPUTS)	D ₁₆ - 39	40 - Q ₁₆ (DATA OUTPUTS)
	D ₁₇ - 41	42 - Q ₁₇
	D ₁₈ - 43	44 - Q ₁₈
	D ₁₉ - 45	46 - Q ₁₉
	D ₂₀ - 47	48 - Q ₂₀
	D ₂₁ - 49	50 - Q ₂₁
	D ₂₂ - 51	52 - Q ₂₂
	D ₂₃ - 53	54 - Q ₂₃
(GROUND)	V _{SS} - 55	56 - MR (MEMORY RESET*)
(OUTPUT ENABLE _{HIGH} *)	OE _H - 57	58 - EN _H (ENABLE _{HIGH} *)
(DATA INPUTS)	D ₂₄ - 59	60 - Q ₂₄ (DATA OUTPUTS)
	D ₂₅ - 61	62 - Q ₂₅
	D ₂₆ - 63	64 - Q ₂₆
	D ₂₇ - 65	66 - Q ₂₇
	D ₂₈ - 67	68 - Q ₂₈
	D ₂₉ - 69	70 - Q ₂₉
	D ₃₀ - 71	72 - Q ₃₀
	D ₃₁ - 73	74 - Q ₃₁
(CLOCK)	CP - 75	

*ACTIVE LOW



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