PRELIMINARY

5 VOLT VALUE SERIES 200 FLASH MEMORY CARD

iMC008FLSG, iMC016FLSG, iMC024FLSG
iMC032FLSG, iMC048FLSG, iMC064FLSG

- **Low-Cost Linear Flash Card**
  - **Intel® StrataFlash™ Memory Technology**
- **High-Performance Writes**
  - **6 µs Typical Byte Write**
- **Fast Read Performance**
  - **200 ns Max Access Time**
- **Low-Cost Linear Flash Card**
- **32 Byte Write Buffer**
  - **Frees CPU to Perform Other Tasks**
- **Single Supply Operation**
  - **5 V Read/Write**
- **x16 Data Interface**
- **Automated Write and Erase Algorithms**
  - **CFI and SCS Compliant**
- **Enhanced Automated Suspend Options**
  - **Block Erase Suspend to Write**
  - **Block Erase Suspend to Read**
- **Enhanced Data Protection Features**
  - **Flexible Block Locking**
- **100,000 Erase Cycles per Block**
- **128-Kbyte Erase Blocks**
- **Compact Form Factor**
  - **Type 1 PC Card**

The Intel® 5 Volt Series 200 Flash Memory Cards deliver the benefits of Intel® StrataFlash™ memory to users of portable electronic systems. Intel StrataFlash memory benefits include: more density in less space, lowest cost-per-bit NOR devices, support for code and data storage, and easy migration to future devices. Providing 2X the bits in 1X the space, Intel StrataFlash memory devices are the first to bring reliable, two-bit-per-cell storage technology to the flash memory market.

Using the same NOR-based ETOX™ technology as Intel's one-bit-per-cell products, Intel StrataFlash memory devices take advantage of 400 million units of manufacturing experience since 1988. Manufactured on Intel's 0.4 micron ETOX V process technology, Intel StrataFlash memory provides the highest levels of quality and reliability. As a result, Intel StrataFlash components are ideal for code or data applications where high density and low cost are required. Examples include networking, telecommunications, audio recording, and digital imaging.

Intel StrataFlash memory components provide a new generation of forward-compatible software support built upon the Intel® FlashFile™ memory architecture. By using the Common Flash Interface (CFI) and the Scaleable Command Set (SCS), customers can take advantage of density upgrades and optimized write capabilities of future Intel StrataFlash memory devices.

5 Volt Value Series 200 Flash Memory Cards, based on the PCMCIA PC Card Specification, employ Intel StrataFlash components to provide the ultimate in convenient, low-cost data storage for users of portable electronics systems. The flash memory card provides the lowest cost, highest performance nonvolatile read/write solution for solid-state storage applications. These applications are enhanced further with the product's symmetrically-blocked architecture, extended MTBF, and 5 Volt operation. Card memory is organized as a x16 linear array of flash memory devices. Host-based filing system software, such as Flash Translation Layer (FTL) eliminates the need for expensive card-based microcontrollers and ASICs.

The cards offer the PC Card industry-standard pinout in the most compact PC Card form factor (Type 1), a removable linear flash memory medium, the ability to upgrade system memory software without board layout changes, and compatibility over a wide range of MS-DOS* and Windows* 95-based PCs systems.

NOTE: This document formerly known as *Value Series 200 Flash Memory Card 8—64 Megabytes.*

December 1998 Order Number: 290621-005

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

The iMC008FLSG, iMC016FLSG, iMC024FLSG, iMC032FLSG, iMC048FLSG, iMC064FLSG may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 5937
Denver, CO 80217-9808

or call 1-800-548-4725
or visit Intel's website at http://www.intel.com

COPYRIGHT © INTEL CORPORATION 1998 CG-041493

*Third-party brands and names are the property of their respective owners

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
12/01/97	-001	Original version
4/01/98	-002	Updated front cover sheet highlights: eliminated 40- and 56-Mbyte density offerings; changed write speed to 7 µs; changed number of erase cycles per block to 100,000 In third paragraph of legal statement on page 2, eliminated iMC040FLSG and iMC056FLSG references In Paragraph 2.0, *Product Overview,* reworded the first sentence of the first paragraph to eliminate the implied availability of all multiples of 8-Mbytes for memory densities offered in the range from 8- to 64-Mbytes In Table 3, *Card Signal Values for the Card's Bus Operations and Modes,* changed conditions for Word Read, Word Write and Standby operations In first sentence of Paragraph 4.1.3, *Standby*, re-defined standby mode entry conditions In Table 10, *Value Series 200 Card Tuples,* eliminated entries not related to products actually offered: eliminated 40- and 56-Mbyte references and 150 ns speed references In Paragraph 7.2, *Power-Up/Down Protection*, reworded the second sentence of the third paragraph for the requirement that WE# must be low and CE_1# or CE_2# must be low for a command write

REVISION HISTORY (Continued)

4/01/98	-002	In Paragraph 8.4, *DC Characteristics*, changed the minimum limit for V_{IH} to 0.7 V_{CC} (from 2.0) In Paragraph 8.4, *DC Characteristics*, eliminated I_{CCS} and I_{CCD} entries for 40- and 56-Mbyte cards In note 1 of paragraph 8.5.2, *Write Operations*, restated the "CE# deasserted" conditions to be both CE#s (CEL# and CEH#) instead of either one of the CEs (CEL# or CEH#) In paragraph 8.6, *Block Erase, Write, and Lock-Bit Configuration Performance*, changed the "Typ" entries for first 3 parameters (pertaining to write time) to increase write times by 16.67%; added note 6 to describe expected write time performance relative to the specified maximum and typical values, and to suggest use of RDY/BSY# to maximize system performance. In Paragraph 10.0, *Ordering Information,* deleted density codes for 40- and 56-Mbytes
05/01/98	-003	Updated front cover sheet highlights: changed write speed to 6.3 µs
05/15/98	-004	Updated front cover sheet highlights: changed write speed to 12 µs In Table 8.5.1, *Read Operations—Common Memory*, changed IEEE symbol t_{GHQZ} to t_{EHQZ} In Paragraph 8.6 *Block Erase, Write, and Lock-Bit Configuration Performance,* changed typical values for the following parameters: Write Buffer Word Write Time, Word Write Time (Using Word Write Command), and Block Write Time (Using Write to Buffer Command)
12/22/98	-005	8-,16-,24-, and 32-Mbyte cards use 28F320J5 components Updated I_{CCS} and I_{CCD} Specifications Updated Table 8.6, *Block Erase, Write and Lock-Bit Configuration Performance* Name of document changed from *Value Series 200 Flash Memory Card 8—64 Megabytes.*

1.0 SCOPE OF DOCUMENT

This datasheet describes an Intel StrataFlash™ memory card architecture, AC and DC characteristics and command definitions. Refer to the *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet, order number 290606.

2.0 PRODUCT OVERVIEW

The Intel 5 Volt Value Series 200 family of flash memory PC Cards offers a lowest cost selection of memory card products ranging in memory density from 8- to 64-Mbytes. Each card contains a flash memory array made up of Intel StrataFlash memory components. The 8-, 16-, 24-, or 32-Mbyte cards consist of between two and eight 4-Mbyte components (Intel® 28F320J5) configured for x16 (word-wide) operation. The 48- or 64-Mbyte cards consist of multiple 8-Mbyte components (Intel® 28F640J5) also configured for x16 (word-wide) operation. Intel StrataFlash memory can store more than one bit per flash memory cell, reducing the size and cost of large flash memory arrays. Figure 1 presents a 8-Mbyte card block diagram as an example illustration of the functional layout and user interface of a 5 Volt Value Series 200 card.

A Command User Interface (CUI) serves as the interface between the system processor and internal operation of the card's memory device(s). A valid command sequence written to the CUI initiates device automation. An internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for block erase, write, and lock-bit configuration operations.

Each Intel StrataFlash memory device incorporates a 16-word (32-byte) write buffer. This dramatically improves write performance by optimizing a flash memory device's programming algorithm, thereby freeing the CPU from writing data and polling status on a word-by-word basis. The 32-byte buffer can be loaded at full bus speed; then a single command can be issued to transfer the buffer into the flash memory array. While the Write State Machine (WSM) is handling all of the flash memory programming details for a memory write operation, the host CPU is free to perform other tasks.

The 28F640J5 or E28F320J5 components forming a card's memory array each contain 64/32 separate 128-Kbyte erase blocks. The number of erase blocks on a card range from 64 erase blocks for a 8-Mbyte card to 512 erase blocks for a 64-Mbyte card. A block erase operation erases one of the 128-Kbyte blocks typically within one second—independent of other blocks. Each block can be independently erased 10,000 times. Block erase suspend mode allows system software to suspend block erase to read data from or write data to any other block.

3.0 CARD ARCHITECTURE

The 5 Volt Value Series 200 Flash Memory PC Card implements the functionality of the PCMCIA PC Card Specification with X16 (word-wide) data transfers. The card does not support individual 8-bit (byte) wide memory data transfers as the card's memory devices(s) and data bus interface are structured word-wide.

Various information about the card is contained in a Card Information Structure (CIS) as defined in the PCMCIA PC Card Specification. The CIS is stored in Block 0 of the card's memory array. The high byte of the CIS is always FFH, the low byte contains the actual CIS data.

The Card information Structure (CIS) for the 5 Volt Value Series 200 card is stored in Block 0 of the flash memory to reduce the attribute memory cost overhead of an EEPROM or ASIC. In embedded applications, a CIS may not be required by the system and the entire memory array can be used by the system.

The CIS is stored in Block 0 of the flash memory to reduce the attribute memory cost overhead of an EEPROM or ASIC. In embedded applications, a CIS may not be required by the system and the entire memory array can be used by the system.

3.1 Card Signal Description

The signals for the 5 Volt Value Series 200 Flash Memory PC Card are listed in Table 1. They comply with the *PC Card Specification*.

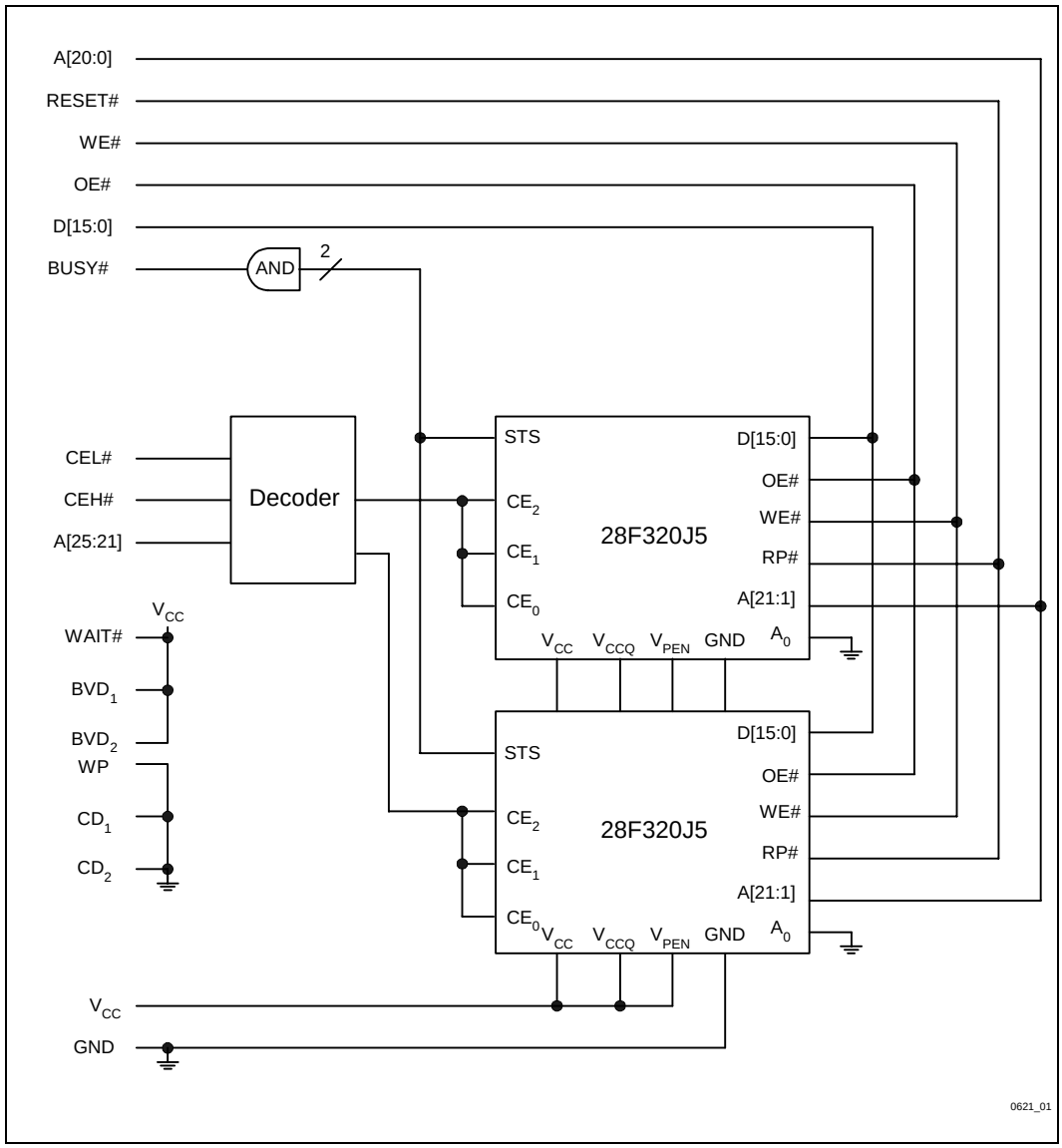


Figure 1. 8-Mbyte Flash Memory Card Block Diagram Showing Major Functional Elements

Table 1. 5 Volt Value Series 200 Flash Memory PC Card Definitions

Pin	Signal	I/O	Function	Active
1	GND		Ground	
2	DQ_3	I/O	Data Bit 3	
3	DQ_4	I/O	Data Bit 4	
4	DQ_5	I/O	Data Bit 5	
5	DQ_6	I/O	Data Bit 6	
6	DQ_7	I/O	Data Bit 7	
7	CE_1#	I	Card Enable 1	LOW
8	A_{10}	I	Address Bit 10	
9	OE#	I	Output Enable	LOW
10	A_{11}	I	Address Bit 11	
11	A_9	I	Address Bit 9	
12	A_8	I	Address Bit 8	
13	A_{13}	I	Address Bit 13	
14	A_{14}	I	Address Bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Supply Voltage	N.C.
19	A_{16}	I	Address Bit 16	
20	A_{15}	I	Address Bit 15	
21	A_{12}	I	Address Bit 12	
22	A_7	I	Address Bit 7	
23	A_6	I	Address Bit 6	
24	A_5	I	Address Bit 5	
25	A_4	I	Address Bit 4	
26	A_3	I	Address Bit 3	

Pin	Signal	I/O	Function	Active
27	A_2	I	Address Bit 2	
28	A_1	I	Address Bit 1	
29	A_0	I	Address Bit 0	
30	DQ_0	I/O	Data Bit 0	
31	DQ_1	I/O	Data Bit 1	
32	DQ_2	I/O	Data Bit 2	
33	WP	O	Write Protect	HIGH
34	GND		Ground	
35	GND		Ground	
36	CD_1#	O	Card Detect 1	LOW
37	DQ_{11}	I/O	Data Bit 11	
38	DQ_{12}	I/O	Data Bit 12	
39	DQ_{13}	I/O	Data Bit 13	
40	DQ_{14}	I/O	Data Bit 14	
41	DQ_{15}	I/O	Data Bit 15	
42	CE_2#	I	Card Enable 2	LOW
43	VS_1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address Bit 17	
47	A_{18}	I	Address Bit 18	
48	A_{19}	I	Address Bit 19	
49	A_{20}	I	Address Bit 20	
50	A_{21}	I	Address Bit 21	
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Supply Voltage	N.C.

Table 1. 5 Volt Value Series 200 Flash Memory PC Card Definitions (Continued)

Pin	Signal	I/O	Function	Active
53	A_{22}	I	Address Bit 22	
54	A_{23}	I	Address Bit 23	
55	A_{24}	I	Address Bit 24	
56	A_{25}	I	Address Bit 25	N.C.
57	VS_2	O	Voltage Sense 2	N.C.
58	RST	I	Reset	HIGH
59	WAIT#	O	Extend Bus Cycle	LOW
60	RFU		Reserved	

Pin	Signal	I/O	Function	Active
61	REG#	I	Attribute Memory Select	
62	BVD_2	O	Battery Voltage Detect 2	
63	BVD_1	O	Battery Voltage Detect 1	
64	DQ_8	I/O	Data Bit 8	
65	DQ_9	I/O	Data Bit 9	
66	DQ_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

Table 2. 5 Volt Value Series 200 Flash Memory PC Card Interface Signal Description

Symbol	Type	Name and Function
A_0–A_{25}	INPUT	**ADDRESS INPUTS:** A_0 through A_{25} enable direct addressing of up to 64 MB of memory on the card. Signal A_0 is not decoded since the card is x16 only. The memory will wrap at the card density boundary. The system should **not** try to access memory beyond the card's density, since the upper addresses are not decoded.
DQ_0–DQ_{15}	INPUT/ OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 through DQ_{15} constitute the bi-directional data bus. DQ_{15} is the most significant bit.
CE_1#, CE_2#	INPUT	**CARD ENABLE 1 & 2:** CE_1# enables accesses on the low byte of the data bus $D_{0–7}$. CE_2# enables accesses on the high byte of the data bus $D_{8–15}$. Both CE_1# and CE_2# are active low signals. A host is expected to assert both CE_1# and CE_2# as the card's memory provides for word-wide data transfers but not byte-wide data transfers.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal enabling read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or write activities. A high output indicates the memory card is ready to accept accesses.
CD_1#, CD_2#	OUTPUT	**CARD DETECT 1 & 2:** These signals provide for card insertion detection. The signals are connected to ground internally on the memory card, and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.

Table 2. 5 Volt Value Series 200 Flash Memory PC Card Interface Signal Description (Continued)

Symbol	Type	Name and Function
WP	OUTPUT	**WRITE PROTECT:** This signal is pulled LOW for PC Card Standard compatibility. The flash memory card has no WP signal functionality.
V_{PP1},V_{PP2}	N.C.	**PROGRAM/ERASE POWER SUPPLY:** These power signals are not connected on the card as the card's memory devices use V_{CC} for program (write) and erase power.
V_{CC}		**CARD POWER SUPPLY:** 5.0 V for all internal circuitry.
GND		**GROUND** for all internal circuitry.
REG#	INPUT	**REGISTER SELECT:** The memory card has no separate attribute memory. The CIS is located in common memory. REG# is unconnected on the card.
RST	INPUT	**RESET:** Active high signal for placing card in Power-On Default State. RESET can be used as a POWER-DOWN signal for the memory array.
WAIT#	OUTPUT	**WAIT:** (Extended Bus Cycle) This signal is pulled high for PC Card Standard compatibility. The flash memory card has no WAIT# signal functionality.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS_1, VS_2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1 and VS_2 are OPEN to indicate a 5 V V_{CC} card has been inserted.
RFU		**RESERVED FOR FUTURE USE**
N.C.		**NO INTERNAL CONNECTION TO CARD** pin may be driven or left floating.

4.0 MEMORY CONTROL LOGIC

4.1 Bus Operations

The host executes memory read, write and erase operations by issuing the appropriate command to the Flash memory's Command User Interface (CUI). The CUI, which supports the command set of the card's memory devices, serves as the interface between the host processor and internal operation of a flash device. Commands can be issued to the CUI using standard microprocessor bus cycles.

Table 3 lists the PC Card's bus operations and modes. For each listed bus operation or mode the table defines the value of the card's relevant bus and control signals.

4.1.1 READ ARRAY

The host enables reads from the card by writing the appropriate read command to the CUI. The memory devices automatically reset to read array mode upon initial card power-up or after card reset. CE_1#, CE_2#, and OE# must be logically active to obtain 16 data bits at the outputs. The Card Enable (CE_1# and CE_2#) inputs together with the card's address inputs are used to select the addressed devices. Output Enable (OE#) is the data input/output (D_0–D_{15}) direction control, and when active, drives data from the selected memory onto the data bus. WE# must be driven to V_{IH} (inactive) during a read access.

4.1.2 OUTPUT DISABLE

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Outputs (D_0–D_{15}) are placed in a high-impedance state.

Table 3. Card Signal Values for the Card's Bus Operations and Modes

Bus Operation/Mode	RESET#	CE_1#	CE_2#	OE#	WE#	A1	D8–15	D0–7	Notes
Word Read	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	High	Low	1, 2, 3
	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	High	Low	1, 2, 3, 4
	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	High	Low	1, 2, 3, 4
Word Write	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	High	Low	1, 2, 3
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	High	Low	1, 2, 3, 5
	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	High	Low	1, 2, 3, 5
Manufacturer ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	00H	89H	
Device ID	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00H	14H	
							00H	15H	
Standby	V_{IH}	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z	
Output Disable	V_{IH}	X	X	V_{IH}	V_{IH}	X	High-Z	High-Z	
Reset/Power-Down	V_{IL}	X	X	X	X	X	High-Z	High-Z	

NOTES:

1. X can be V_{IL} or V_{IH} for control signals and address.
2. BUSY# is V_{OL} when the WSM is executing internal write or block erase algorithms. It is V_{OH} when the WSM is not busy, in erase suspend mode, or deep power-down mode.
3. High indicates high byte data, low indicates low byte data.
4. Both memory bytes will be read from memory as the card's memory component data bus is word-wide and does not provide for individual byte access. The bus operation is non-compliant with the *PCMCIA PC Card Standard* as *the PC Card Standard* specifies a byte read operation instead of a word read operation for the listed signal conditions.
5. Both memory bytes will be written to memory as the card's memory component data bus is word-wide and does not provide for individual byte access. The bus operation is non-compliant with the *PCMCIA PC Card Standard* as *the PC Card Standard* specifies a byte write operation instead of a word write operation for the listed signal conditions. If a host system desires a byte write operation instead of a word write operation, then the host system must write V_{IH} to the unwanted active byte (which should be inactive according the *PC Card Standard*) in order to prevent the unwanted active byte from being written to card memory.

4.1.3 STANDBY

If both CE_1# and CE_2# are at a logic-high level (V_{IH}), the card enters standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (D_0–D_{15}) are placed in a high-impedance state independent of the status of OE#. If the host deselects the card during a write or erase, the card continues to function and consume normal active power until the operation completes.

4.1.4 RESET/POWER-DOWN

RESET# at V_{IL} initiates the reset/power-down mode.

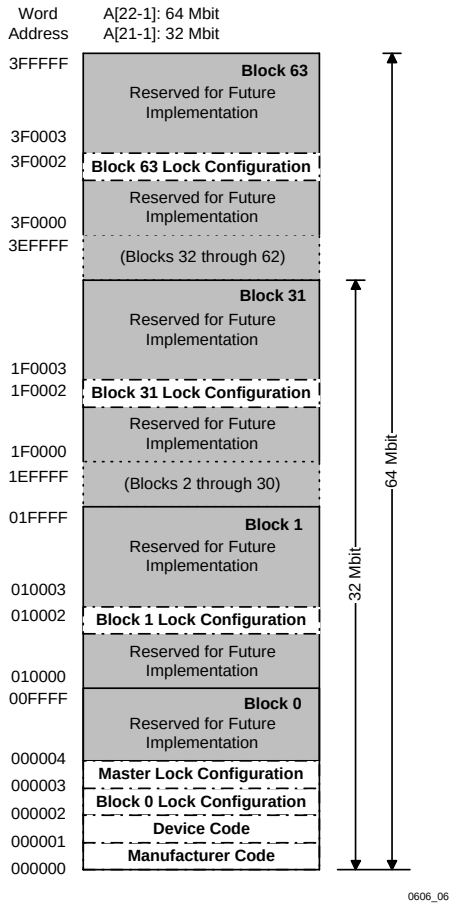
In read modes, RESET#-low deselects the card's memory, places output drivers in a high-impedance state, and turns off numerous internal memory circuits. RESET# must be held low for a minimum of t_w. Time t_{su} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and all memory device status registers are set to 80H.

During block erase, write, or lock-bit configuration modes, RESET#-low will abort the operation BUSY# transitions low and remains low for a maximum time of $t_w + t_{su}$ until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially corrupted after a write operation or partially altered after an erase or lock-bit configuration operation. Time t_{su} is required after RESET# goes to logic-high (V_{IH}) before another command can be written.

As with any automated device, it is important to assert RESET# during system reset. When the system comes out of reset, it expects to read data from the flash memory. Automated flash memories provide status information when accessed during block erase, write, or lock-bit configuration modes. If a CPU reset occurs with no flash memory reset, proper initialization may not occur because the flash memory may be providing status information instead of array data. Intel's flash memories allow proper initialization following a system reset through the use of the RESET# input. In this application, RESET# is controlled by the same signal that resets the system CPU.

4.1.5 READ IDENTIFIER CODES

The read identifier codes operation outputs the manufacturer code, device code, block lock configuration codes for each block, and the master lock configuration code (see Figure 2). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms. The block lock and master lock configuration codes identify locked and unlocked blocks and master lock-bit setting.



NOTES:

1. Data is always given on the low byte (upper byte contains 00h).
2. Memory shown is accessed by the Read Identifier Codes command only and is physically distinct from the card's Flash memory array.
3. Master Lock function of the card's underlying memory devices is not a card function. The Master Lock Configuration information identified in the above memory map is shown only for the sake of consistency between the illustrated memory map and a corresponding memory map shown in the datasheet for the memory devices.

Figure 2. Device Identifier Code Memory Map

4.1.6 WRITE

Writing commands to the CUI enables reading of device data, query, identifier codes, inspection and clearing of the status register, as well as block erasure, writing of data and lock-bit configuration.

The Block Erase command requires appropriate command data and an address within the block to be erased. The Word Write command requires the command and address of the location to be written. The Write to Buffer command requires the command, starting address of the memory region to be written and the number of words to be written to the write buffer. Set Master and Block Lock-Bit commands require the command and address within the device (Master Lock) or block within the device (Block Lock) to be locked. The Clear Block Lock-Bits command requires the command and address within the device.

The CUI does not occupy an addressable memory location. It is part of each memory device and is written when the device is enabled and WE# is active. The address and data needed to execute a command are latched on the rising edge of WE# or the first edge of CE_1# or CE_2# that disables the device. Write cycle timing is specified in Section 8.5.2, *Write Operations*.

4.2 Decode Logic

The card's decode logic enables the appropriate memory component during a read or write access of card memory. Unused upper addresses for the 5 Volt Value Series 200 Flash Memory PC Card will not be decoded. The address decoding will wrap around at the card's density.

5.0 COMMAND DEFINITION

The operations of the card's memory device(s) are selected by the writing of specific commands into the CUI. The 5 Volt Value Series 200 Flash Memory PC Card implements two command sets: the basic command set and the scaleable command set. The Basic Command Set is backward compatible with Value Series 100 Flash Memory PC Card with the exception that write (program) suspend is not supported in the Series 200. The Scaleable Command Set adds three capabilities to the PC Card in addition to the Basic Command Set:

1. Common Flash Interface (CFI);
2. buffered writes which employ a 32-byte write buffer to allow higher performance writes than available with the Basic Command Set; and
3. a configurable BUSY# output.

5.1 Basic Command Set

Table 4 presents the 5 Volt Value Series 200 PC Card's Basic Command Set. The table indicates that the commands require one or more bus cycles to implement. The table and notes following the table describe each bus cycle. Complete descriptions of the individual commands follow in subsections of the current document section.

5.1.1 READ ARRAY COMMAND

Upon initial device power-up and after exit from reset/power-down mode, the card's memory devices default to read array mode. This operation is also initiated by writing the Read Array command to a memory device. The device remains enabled for reads until another command is written. Once the internal WSM has started a block erase, write, or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation unless the WSM is suspended via an Erase Suspend command.

Table 4. Basic Command Set Definitions(9)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3,4)	Oper(1)	Addr(2)	Data(3,4)
Read Array	1		Write	X	XXFFH			
Read Identifier Codes	≥2	5	Write	X	XX90H	Read	IA	ID
Read Status Register	2		Write	X	XX70H	Read	X	SRD
Clear Status Register	1		Write	X	XX50H			
Word Write	2	6, 7	Write	X	XX40H or XX10H	Write	WA	WD
Block Erase	2	7	Write	X	XX20H	Write	BA	XXD0H
Block Erase Suspend	1	7	Write	X	XXB0H			
Block Erase Resume	1	7	Write	X	XXD0H			
Set Block Lock-Bit	2		Write	X	XX60H	Write	BA	XX01H
Clear Block Lock-Bits	2	8	Write	X	XX60H	Write	X	XXD0H

NOTES:

1. Card signal values for the identified bus operations are defined inTable 3.
2. X = Any valid address within the device.
   IA = Identifier Code Address:
   BA = Address within the block being erased or locked.
   WA = Address of memory location to be written.
3. SRD = Data read from Status Register.
   WD = Data to be written at location WA. Data is latched on the rising edge of WE#.
   ID = Data read from Identifier Codes.
4. The upper byte of the data bus during command writes is a "Don't Care" (X).
5. Following the Read Identifier Codes command, read operations access manufacturer, device, block lock, and master lock codes. See Read Identifier Section for read identifier code data.
6. Either XX40H or XX10H are recognized by the WSM as the word-write command setup.
7. The issue of a block erase or write-word command to a locked block will fail.
8. The clear block lock-bits operation simultaneously clears all block lock-bits.
9. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

5.1.2 READ IDENTIFIER CODES COMMAND

The identifier code operation is initiated by writing the Read Identifier Codes command to a memory device. Following the command write, read cycles from addresses shown in Figure 2 retrieve the manufacturer, device, block lock configuration and master lock configuration codes (see Table 5 for identifier code values). To terminate the operation, write another valid command. The Read Identifier Codes command is valid only when the WSM is off or the device is suspended. Following the Read Identifier Codes command, the following information can be read:

Table 5. Identifier Codes(1)

Code	Addr (1)	Data
Manufacture Code	00000	(00) 89
Device Code (28F640J5)	00001	(00) 15
Device Code (28F320J5)	00001	(00) 14
Block Lock Configuration	x0002(2)	
• Block Is Unlocked		$DQ_0 = 0$
• Block Is Locked		$DQ_0 = 1$
• Reserved for Future Use		$DQ_{1–7}$
Master Lock Configuration(3)	00003	
• Device Is Unlocked		$DQ_0 = 0$
• Device Is Locked		$DQ_0 = 1$
• Reserved for Future Use		$DQ_{1–7}$

NOTES:

1. Data is always presented on the low byte (upper byte contains 00h).
2. X selects the specific block's lock configuration code. See Figure 2 for the device identifier code memory map.
3. See the *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet for a description of Master Lock Configuration information. For 5 Volt Value Series 200 Flash Memory PC Cards the Master Lock Configuration byte should indicate that the device is unlocked ($DQ_0 = 0$).

5.1.3 READ STATUS REGISTER COMMAND

The status register may be read to determine when a block erase, write, or lock-bit configuration operation is complete and whether the operation completed successfully. Table 6 defines the content and format of the status register. The register may be read at any time by writing the Read Status Register command. After writing this command, all subsequent read operations output data from the status register until another valid command is written. The status register contents are latched on the falling edge of OE# or the first edge of CE_1# and CE_2# that enables the device (see Table 3, *Card Signal Values for the Card's Bus Operations and Modes*). OE# must toggle to V_{IH} or the device enter standby mode (see Table 3) before further reads to update the status register latch.

During a word write, write to buffer, block erase, set lock-bit, or clear lock-bit command sequence, only SR.7 is valid until the Write State Machine completes or suspends the operation. Device I/O pins DQ_0–DQ_6 and DQ_8–DQ_{15} are placed in a high-impedance state. When the operation completes or suspends (check status register bit 7), all contents of the status register are valid when read.

5.1.4 CLEAR STATUS REGISTER COMMAND

Status register bits SR.5, SR.4, SR.3, and SR.1 are set to "1"s by the WSM and can only be reset by the Clear Status Register command. These bits indicate various failure conditions (see Table 6). By allowing system software to reset these bits, several operations (such as cumulatively erasing or locking of multiple blocks or writing of several bytes in sequence) may be performed. The status register may be polled to determine if an error occurred during the sequence.

To clear the status register, the Clear Status Register command (50H) is written. The Clear Status Register command is only valid when the WSM is off or the device is suspended.

Table 6. Status Register Definitions(1)

WSMS	ESS	ECLBS	PSLBS	VPENS	R	DPS	R
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

High Z When Busy?	Status Register Bits	NOTES:
No	SR.7 = WRITE STATE MACHINE STATUS 1 = Ready 0 = Busy	Check BUSY# or SR.7 to determine block erase, write (program), or lock-bit configuration completion. SR.6–SR.0 are not driven while SR.7 = "0."
Yes	SR.6 = ERASE SUSPEND STATUS 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entered.
Yes	SR.5 = ERASE AND CLEAR LOCK-BITS STATUS 1 = Error in Block Erasure or Clear Lock-Bits 0 = Successful Block Erase or Clear Lock-Bits	SR.3 does not provide a continuous memory device (write) programming voltage level indication. The WSM interrogates and indicates the programming voltage level only after Block Erase, Word Write, Write to Buffer, Set Block/Master Lock-Bit, or Clear Block Lock-Bits command sequences.
Yes	SR.4 = WRITE AND SET LOCK-BIT STATUS 1 = Error in Write Operation or Set Master/Block Lock-Bit 0 = Successful Write Operation or Set Master/Block Lock Bit	SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RESET# (RP#) only after Block Erase, Write Word, Write to Buffer or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RESET# (RP#) is not V_{HH}. Read the block lock and master lock configuration codes using the Read Identifier Codes command to determine master and block lock-bit status.
Yes	SR.3 = PROGRAMMING VOLTAGE STATUS 1 = Low Programming Voltage Detected, Write Operation Aborted 0 = Programming Voltage OK	
Yes	SR.2 = RESERVED FOR FUTURE ENHANCEMENTS	
Yes	SR.1 = DEVICE PROTECT STATUS 1 = Master Lock-Bit, Block Lock-Bit and/or RESET# (RP#) Lock Detected, Operation Abort 0 = Unlock	
Yes	SR.0 = RESERVED FOR FUTURE ENHANCEMENTS	SR.2 and SR.0 are reserved for future use and should be masked when polling the status register.

NOTE:

1. See the *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet for a description of the master lock-bit. For 5 Volt Value Series 200 Flash Memory PC Cards the master lock-bit should always be = "0" and should not interfere with any of the card's write or erase operations. The bit is referenced in the table for consistency of definition between the card and card memory device datasheets as the card status register information is actually provided by whatever memory device receives the Read Status Register command.

Table 7. eXtended Status Register Definitions

WBS	Reserved
bit 7	bits 6–0

High Z When Busy?	Status Register Bits	NOTES:
No	XSR.7 = WRITE BUFFER STATUS 1 = Write buffer available 0 = Write buffer not available	After a Buffer-Write command, XSR.7 = 1 indicates that a Write Buffer is available.
Yes	XSR.6–XSR.0 = RESERVED FOR FUTURE ENHANCEMENTS	SR.6–SR.0 are reserved for future use and should be masked when polling the status register.

5.1.5 BLOCK ERASE COMMAND

Erase is executed one block at a time and initiated by a two-cycle command. A block erase setup is first written, followed by an block erase confirm. This command sequence requires an appropriate address within the block to be erased (erase changes all block data to FFH). Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). After the two-cycle block erase sequence is written, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the logic level of the STS pin or status register bit SR.7. Toggle OE#, CE_1# or CE_2# to update the status register.

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

This two-step command sequence of set-up followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in both status register bits SR.4 and SR.5 being set to “1.” Successful block erase requires that the corresponding block lock-bit be cleared. If block erase is attempted when the corresponding block lock-bit is set, SR.1 and SR.5 will be set to “1.”

5.1.6 BLOCK ERASE SUSPEND COMMAND

The Block Erase Suspend command allows block-erase interruption to read or write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. The device outputs status register data when read after the Block Erase Suspend command is written. Polling status register bit SR.7 then SR.6 can determine when the block erase operation has been suspended (both will be set to “1”). The BUSY# output will also transition to V_{OH}. Specification t_{WHRH} defines the block erase suspend latency.

At this point, a Read Array command can be written in order to read data from blocks other than that which is suspended. A word-write or write-to-buffer command sequence can also be issued during erase suspend to write data in other blocks. During a write operation with block erase suspended, status register bit SR.7 will return to “0” and the BUSY# output will transition to V_{OL}.

The only other valid commands while block erase is suspended are Read Query, Read Status Register, Clear Status Register, Configure, and Block Erase Resume. After a Block Erase Resume command is written to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and the BUSY# output will return to V_{OL}. After the Erase Resume command is written, the device automatically outputs status register data when read. Block erase cannot resume until write operations initiated during block erase suspend have completed.

5.1.7 WORD-WRITE COMMAND

Word-write commands are executed in a two-cycle command sequence. Word-write command setup (standard 40H or alternate 10H) is written in the first cycle and then followed in the next cycle by a second write that specifies the address and data (latched on the rising edge of WE#) to be written in memory. The WSM then takes over, controlling the word-write and word-write verify algorithms internally. After the word-write command sequence is written, the device automatically outputs status register data when read. The CPU can detect the completion of the write event by analyzing the logic state of the BUSY# output or status register bit SR.7.

When the word-write operation is complete, status register bit SR.4 should be checked. If a write error is detected, the status register should be cleared. The internal WSM verify only detects errors for “1”s that do not successfully program to “0”s. The CUI remains in read status register mode until it receives another command.

Successful write operations require that the corresponding block lock-bit be cleared. If a word write operation is attempted when the corresponding block lock-bit is set, SR.1 and SR.4 will be set to “1.”

5.1.8 SET BLOCK LOCK-BIT COMMAND

A flexible block locking and unlocking scheme is enabled via a combination of block lock-bits. The block lock-bits gate memory write and erase operations. Individual block lock-bits can be set using the Set Block Lock-Bit command. Set Block Lock-Bit commands are invalid while the WSM is running or the device is suspended.

Set block lock-bit commands are executed by a two-cycle sequence. The set block lock-bit setup along with appropriate block or device address is written followed by the set block lock-bit confirm (and an address within the block to be locked). The WSM then controls the set lock-bit algorithm. After the sequence is written, the device automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing the logic state of the BUSY# pin output or status register bit SR.7.

When the set lock-bit operation is complete, status register bit SR.4 should be checked. If an error is detected, the status register should be cleared. The CUI will remain in read status register mode until a new command is issued.

This two-step sequence of set-up followed by execution ensures that lock-bits are not accidentally set. An invalid Set Block Lock-Bit command will result in status register bits SR.4 and SR.5 being set to “1.”

5.1.9 CLEAR BLOCK LOCK-BITS COMMAND

All set block lock-bits are cleared in parallel via the Clear Block Lock-Bits command. This command is invalid while the WSM is running or the device is suspended.

Clear block lock-bits command is executed by a two-cycle sequence. A clear block lock-bits setup is first written followed by the clear block lock-bits confirm. The device automatically outputs status register data when read. The CPU can detect completion of the clear block lock-bits event by analyzing the logic state of the BUSY# pin output or status register bit SR.7.

When the operation is complete, status register bit SR.5 should be checked. If a clear block lock-bit error is detected, the status register should be cleared. The CUI will remain in read status register mode until another command is issued.

This two-step sequence of set-up followed by execution ensures that block lock-bits are not accidentally cleared. An invalid Clear Block Lock-Bits command sequence will result in status register bits SR.4 and SR.5 being set to “1.”

If a clear block lock-bits operation is aborted due to V_{CC} transitioning out of valid range or RESET# active transition, block lock-bit values are left in an undetermined state. A repeat of the Clear Block Lock-Bits command is then required to initialize block lock-bit contents to known values.

5.2 Scaleable Command Set

Table 8 presents the 5 Volt Value Series 200 PC Card's *Scaleable Command Set Definitions*. The table indicates that the commands require one or more bus cycles to implement. The table and notes following the table describe each bus cycle. Complete descriptions of the individual commands follow in subsections of the current document section.

Table 8. Scaleable Command Set Definitions(10)

Command	Bus Cycles Req'd.	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3,4)	Oper(1)	Addr(2)	Data(3,4)
Read Query	≥ 2		Write	X	XX98H	Read	QA	QD
Write to Buffer	> 2	5, 6, 7, 8, 9	Write	BA	XXE8H	Write	BA	N
— Confirm	1	6, 7	Write	X	XXD0H			
Configuration		9						

NOTES:

1. Card signal values for the identified bus operations are defined in Table 3.
2. X = Any valid address within the device.
   QA = QUERY database Address.
   BA = Block Address.
3. QD = Data read from QUERY database.
   CC = Configuration Code.
4. The upper byte of the data bus during command writes is a "Don't Care."
5. After the first bus cycle of the Write to Buffer command, check the Extended Status Register to make sure the write buffer is available for writing. If the buffer is available for writing, proceed with the second bus cycle; otherwise, continue repeating the first bus cycle and checking the extended status register in turn until the buffer becomes available; when the buffer becomes available, proceed with the second bus cycle of the Write to Buffer command.
6. The number of words to be written to the Write Buffer = N + 1, where N = word count argument. The word count range on this device is N = 0000H to N = 000FH. Writing a word count outside the buffer boundary causes unexpected results and should be avoided.

   The third and consecutive bus cycles of a Write to Buffer command sequence, as determined by N, are for writing data into the Write Buffer. In the third bus cycle a device start address is given along with the write buffer data. Subsequent write cycles provide additional device addresses and data. All subsequent addresses must lie within the start address plus the count. The Confirm command (XXD0H) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the write to buffer operation. Please see memory component data sheet for additional information on the Wirte to Buffer command.
7. The write buffer operation does not begin until a Confirm command is issued.
8. The issue of a Write to Buffer command to a locked block will fail.
9. The Configuration Command is not supported on the 5 Volt Value Series 200 Flash Memory PC Card. The Configuration Command serves to program the configurable status output (STS output pin) of a memory device. To satisfy the PCMCIA PC Card Specification the STS output pin for all card memory devices must be configured as a RY/BY# pin to generate the card's BUSY# output signal. At card power-up the STS output for all devices defaults to RY/BY# pin operation; thereafter, host software shall not issue the Configuration Command.
10. Commands other than those shown above are reserved for future use and should not be used.

5.2.1 BLOCK WRITE COMMAND

To write to the flash device write buffer, a Write to Buffer command sequence is initiated. A variable number of bytes, up to the buffer size, can be loaded into the buffer and written to the Flash device. First, the Write to Buffer Setup command is issued along with the Block Address of the memory device erase block to which the buffer content will be written. At this point, the eXtended Status Register (XSR) information (reference Table 7) is loaded into the register and XSR.7 reverts to reflecting "buffer available" status. Whenever the memory device is read immediately after receiving a Write to Buffer command, the XSR content will be presented by the memory. If XSR.7 = 0, the write buffer is not available for writing. When XSR.7 = "1," the memory device will allow data to be written to the write buffer. To determine when the write buffer can be written, continue to monitor XSR.7 until XSR.7 = 1 by repeating the sequence of first issuing the Write to Buffer Setup command along with the appropriate Block Address, and then reading the eXtended Status Register.

When the write buffer becomes available for writing, a word count (N) is given to the memory device with the Block Address of the memory device erase block to which the buffer content will be written. On the next write, a device start address is given along with the write buffer data. For maximum programming performance and lower power, align the start address at the beginning of a Write Buffer boundary. Subsequent writes provide additional device addresses and data. All subsequent addresses must lie within the start address plus the count.

After the final buffer data is given, a Write Confirm command is issued. This initiates the WSM (Write State Machine) to begin copying the buffer data to the flash memory. If a command other than Write Confirm is written to the device, an "Invalid Command/Sequence" error will be generated and status register bits SR.5 and SR.4 will be set to a "1." For additional buffer writes, issue another Write to Buffer Setup command and check XSR.7. The write buffers can be loaded while the WSM is busy as long as XSR.7 indicates that a buffer is available.

If an error occurs while a device is writing data to memory, the device will stop writing, and status register bit SR.4 will be set to a "1" to indicate a write operation failure. Any time a media failure occurs during a write or an erase (for which SR.4 or SR.5 is set, respectively), the device will not except any more buffered write commands. Additionally, if the user attempts to write past an erase block boundary with a Write to Buffer command, the device will abort the write. This will generate an "Invalid Command/Sequence" error ("botch") and status register bits SR.5 and SR.4 will be set to a "1." To clear SR.4 and/or SR.5 issue a Clear Status Register command.

Successful writing to an erase block requires that the block's associated Block Lock-Bit bit be reset. If the Block Lock-Bit is set, the erase block is locked. A Write to Buffer command which attempts to write data to the locked block will fail and result in SR.1 and SR.4 being set to "1."

5.2.2 CONFIGURATION COMMAND

The Configuration Command is not supported on the 5 Volt Value Series 200 PC Card. The Configuration Command serves to program the configurable status output (STS output pin) of a memory device. To satisfy the PCMCIA *PC Card Specification* the STS output pin for all card memory devices must be configured as a RY/BY# pin to generate the card's BUSY# output signal. At card power-up the STS output for all devices defaults to RY/BY# pin operation; thereafter, host software shall not issue the Configuration command.

5.2.3 READ QUERY COMMAND

The SCS (Scaleable Command Set) Read Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or "database." The Common Flash Interface provides a standard means for a flash memory to tell a host system about the memory's architecture, algorithms and characteristics. See *AP-646 Common Flash Interface (CFI) and Command Sets* (order number 292204) for a full description of CFI.

Writing the Read Query command to the memory puts it in read query mode. While in read query mode, the memory responds to read bus operations with data from a ROM instead of data from the flash array data. The data in the ROM describes the memory component to which the Ready Query command is addressed.

As the definition of CFI data presented by a card memory device is quite extensive, the definition is not repeated as part of the current document. Refer

to the *5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* (order number 290606) for a complete definition of the card memory's CFI data and the Read Query command by which the data is accessed.

6.0 CARD ATTRIBUTE INFORMATION

6.1 PC Card Information Structure

The Card Information Structure (CIS) begins at address 00000000H of the card's Common Memory Plane and resides sequentially in memory locations with **even** byte memory addresses. It contains a variable length chain of data blocks (tuples) that conform to the basic format described in Table 9. The CIS of the 5 Volt Value Series 200 Flash Memory PC card is found in Table 10.

CAUTION:

The CIS data in Block 0 is not write protected and should not be erased by the system software if the CIS is needed for card recognition.

Table 9. PC Card Tuple Format

Bytes	Data
0	Tuple Code: CISTPL_xxx. The tuple code 0FFH indicates no more tuples in the list.
1	Tuple Link: TPL_LINK. Link to the next tuple in the list. This can be viewed as the number of additional bytes in tuple, excluding this byte. A link field of zero indicates an empty tuple body. A link field containing 0FFH indicates the last tuple in the list.
2-n	Bytes specific to this tuple.

6.2 CIS Data

CIS data is located in memory and describes the 5 Volt Value Series 200 Flash Memory PC Card as illustrated in Table 10.

Table 10. 5 Volt Value Series 200 Card Tuples

Address	Value	Description
00H	01H	**CISTPL_DEVICE**
02H	03H	TPL_LINK
04H	52H	TYPE/SPEED FLASH/200 ns
06H	1EH 3EH 5EH 7EH BEH FEH	CARD SIZE: 8 MB 16 MB 24 MB 32 MB 48 MB 64 MB
08H	FFH	END OF DEVICE
0AH	1EH	**CISTPL DEVICEGEO**
0CH	06H	TPL_LINK
0EH	02H	DGTPL_BUS
10H	11H	DGTPL_EBS
12H	01H	DGTPL_RBS
14H	01H	DGTPL_WBS
16H	01H	DGTPL_PART = 1
18H	01H	FLASH DEVICE INTERLEAVE
1AH	20H	**CISTPL_MANFID**
1CH	04H	TPL_LINK (04H)
1EH	89H	TPLMID_MANF: LSB
20H	00H	TPLMID_MANF: MSB
22H	21H 31H 81H 51H 61H 91H	8MB - 200 ns 16 MB - 200 ns 24 MB - 200 ns 32 MB - 200 ns 48 MB - 200 ns 64 MB - 200 ns
24H	86H	TPLMID_CARD MSB Value Series 200 Card

Table 10. 5 Volt Value Series 200 Card Tuples

Address	Value	Description
26H	21H	**CISTPL_FUNCID**
28H	02H	TPL_LINK
2AH	01H	TPLFID_FUNCTION : Memory
2CH	00H	TPLFID_SYSINIT
2EH	12H	**CISTPL_LONGLINK_C**
30H	04H	TPL_LINK
32H	00H	LOWEST BYTE
34H	00H	
36H	02H	
38H	00H	HIGHEST BYTE
3AH	15H	**CISTPL_VERS1**
3CH	40H	TPL_LINK
3EH	05H	TPLLV1_MAJOR
40H	00H	TPLLV1_MINOR
42H	69H	TPLLV1_INFO i
44H	6EH	n
46H	74H	t
48H	65H	e
4AH	6CH	l
4CH	00H	END TEXT
4EH	56H	V
50H	41H	A
52H	4CH	L
54H	55H	U
56H	45H	E
58H	20H	SPACE
5AH	53H	S
5CH	45H	E
5EH	52H	R

Table 10. 5 Volt Value Series 200 Card Tuples

Address	Value	Description
60H	49H	I
62H	45H	E
64H	53H	S
66H	20H	SPACE
68H	32H	2
6AH	30H	0
6CH	30H	0
6EH	20H	SPACE
70H	00H	END TEXT
72H	30H 31H 32H 33H 34H 36H	8 MB 16 MB 24 MB 32 MB 48 MB 64 MB
74H	38H 36H 34H 32H 38H 34H	8 MB 16 MB 24 MB 32 MB 48 MB 64 MB
76H	20H	SPACE
78H	00H	END TEXT
7AH	43H	C
7CH	4FH	O
7EH	50H	P
80H	59H	Y
82H	52H	R
84H	49H	I
86H	47H	G
88H	48H	H
8AH	54H	T
8CH	20H	SPACE
8EH	49H	I
90H	4EH	N

Table 10. 5 Volt Value Series 200 Card Tuples

Address	Value	Description
92H	54H	T
94H	45H	E
96H	4CH	L
98H	20H	SPACE
9AH	43H	C
9CH	4FH	O
9EH	52H	R
A0H	50H	P
A2H	4FH	O
A4H	52H	R
A6H	41H	A
A8H	54H	T
AAH	49H	I
ACH	4FH	O
AEH	4EH	N
B0H	20H	SPACE
B2H	31H	1
B4H	39H	9
B6H	39H	9
B8H	37H	7

Table 10. 5 Volt Value Series 200 Card Tuples

Address	Value	Description
BAH	00H	END TEXT
BCH	FFH	END OF LIST
BEH	18H	**CISTPL_JEDEC_C**
C0H	02H	TPL_LINK
C2H	89H	MANUFACTURER ID
C4H	15H	JEDEC ID FOR MEMORY DEVICES
C6H	FFH	**CISTPL_END**
C8H	00H	INVALID ADDRESS

7.0 SYSTEM DESIGN CONSIDERATIONS

7.1 Power Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby, active and transient current peaks which are produced by rising and falling edges of CE_1# and CE_2#. The capacitive and inductive loads on the card and internal flash memory device pairs determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection suppress transient voltage peaks. The 5 Volt Value Series 200 cards contain on-card ceramic decoupling capacitors connected between V_{CC} and GND.

The card connector should also have a 4.7 µF electrolytic capacitor between V_{CC} and GND. The bulk capacitors overcome voltage slumps caused by printed-circuit-board trace inductance, and supply charge to the smaller capacitors as needed.

7.2 Power-Up/Down Protection

The PCMCIA/JEIDA-specified socket properly sequences the power supplies to the flash memory card via shorter and longer pins.

Each device in the memory card is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} (0.7 V_{CC}). Since WE# must be low and CE_1# or CE_2# must be low for a command write, driving either WE# to V_{IH} or both CE_1# and CE_2# to V_{IH} will inhibit writes. With its control register architecture, alteration of device contents only occurs after successful completion of the two-step command sequences.

7.3 RDY/BSY# and Write/Block Erase Status Polling

RDY/BSY# is a full CMOS output that provides a hardware method of detecting write and block erase completion. It transitions low time t_{WHRL} after a Write or Erase command sequence is written to a 28F640J5 memory device, and returns to V_{OH} when all the WSM has finished executing the internal algorithm.

RDY/BSY# can be connected to the interrupt input of the system CPU or controller. It is active at all times. RDY/BSY# is also V_{OH} when the device is in erase suspend or deep power-down modes.

8.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains preliminary information on new products in production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

8.1 Absolute Maximum Ratings*

Operating Temperature

During Read, Block Erase, Write, and Lock-Bit Configuration ..... 0 °C to +70 °C(1)

Temperature under Bias ..... –10 °C to +80 °C

Storage Temperature ..... –65 °C to +125 °C

Voltage on Any Pin ..... –2.0 V to +7.0 V(2)

Output Short Circuit Current ..... 100 mA(3)

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on V_{CC} pin. During transitions, this level may undershoot to –2.0 V for periods <20 ns. Maximum DC voltage on input/output pins and V_{CC} is V_{CC} +0.5 V which, during transitions, may overshoot to V_{CC} +2.0 V for periods <20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.

8.2 Operating Conditions

Temperature and V_{CC} Operating Conditions

Symbol	Parameter	Notes	Min	Max	Unit	Test Condition
T_A	Operating Temperature		0	+70	°C	Ambient Temperature
V_{CC}	V_{CC} Supply Voltage (5 V ± 10%)		4.75	5.25	V	

8.3 Capacitance(1)

T_A = +25 °C, f = 1 MHz

Symbol	Parameter	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V

NOTE:

1. Sampled, not 100% tested.

8.4 DC Characteristics

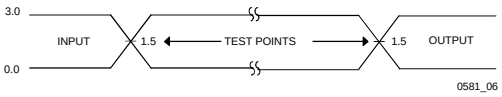
Symbol	Parameter	Notes	Typ	Max	Unit	Test Conditions
I_{LI}	Input Load Current	1,4		20	µA	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current	1		20	µA	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current				µA	$V_{CC} = V_{CC}$ Max
	• 8-Mbyte Card	1,3	180	320		$CE_1\# = CE_2\# = V_{CC} \pm 0.2V$
	• 16-Mbyte Card	1,3	340	620		CMOS Inputs
	• 24-Mbyte Card	1,3	500	920		
	• 32-Mbyte Card	1,3	660	1220		
	• 48-Mbyte Card	1,3	500	920		
	• 64-Mbyte Card	1,3	660	1220		
I_{CCD}	V_{CC} Deep Power-Down Current				µA	RESET, Control Signals =
	• 8-Mbyte Card	1	180	220		$V_{CC} \pm 0.2$ V
	• 16-Mbyte Card	1	340	520		I_{OUT} (READY) = 0 mA
	• 24-Mbyte Card	1	500	770		
	• 32-Mbyte Card	1	660	1020		
	• 48-Mbyte Card	1	500	770		
	• 64-Mbyte Card	1	660	1020		
I_{CCR}	V_{CC} Read Current	1	35	55	mA	$V_{CC} = V_{CC}$ Max, $CE_1\#/ CE_2\#$ = GND, f = 5 MHz, I_{OUT} = 0 mA
I_{CCW}	V_{CC} Word Write or Set Lock-Bit Current	1,3	35	60	mA	CMOS Inputs
I_{CCE}	V_{CC} Block Erase or Clear Lock-Bits Current	1,3	35	70	mA	CMOS Inputs
I_{CCES}	V_{CC} Block Erase Suspend Current	1,2		10	mA	$CE_1\# = CE_2\# = V_{IH}$

8.4 DC Characteristics (Continued)

Sym	Parameter	Notes	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage		–0.5	0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			0.45	V	V_{CC} = V_{CC} Min, I_{OL} = 5.8 mA
V_{OH}	Output High Voltage		0.85 V_{CC}		V	V_{CC} = V_{CC} Min, I_{OH} = –2.5 mA
			V_{CC} – 0.4			V_{CC} = V_{CC} Min, I_{OH} = –100 µA
V_{LKO}	V_{CC} Lockout Voltage		3.25		V	

NOTES:

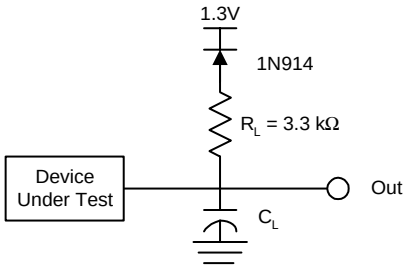
1. All currents are in RMS unless otherwise noted. These currents are valid for all product versions (speeds). Contact Intel's Application Support Hotline or your local sales office for information about typical specifications.
2. I_{CCES} is specified with the card's memory de-selected. If read or word write occurs while in erase suspend mode, the card's current draw is the sum of I_{CCES} and either I_{CCR} (read) or I_{CCW} (write).
3. CMOS inputs are either V_{CC} ± 0.2 V or GND ± 0.2 V.
4. Exceptions: With V_{IN} = GND, the leakage current on CE_1#, CE_2# will be < 50 µA each due to internal pull-up resistors.



NOTE:

1. AC test inputs are driven at 3.0V for a Logic "1" and 0.0 V for a Logic "0." Input timing begins, and output timing ends, at 1.5 V. Input rise and fall times (10% to 90%) < 10 ns.

Figure 3. Transient Input/Output Reference Waveform for V_{CC} = 5 V ± 5% (Standard Test Configuration)



NOTE:

C_L Includes Jig Capacitance

Figure 4. Transient Equivalent Testing Load Circuit

Test Configuration Capacitance Loading Value

Test Configuration	C_L (pF)
V_{CC} = 5.0 V ± 5%	100

8.5 AC Characteristics

AC timing diagrams and characteristics are designed to meet or exceed PCMCIA 2.1 specifications. No delay occurs when switching between the common and attribute memory planes.

8.5.1 READ OPERATIONS—COMMON MEMORY(1)

Symbol		Parameter	8 – 64-MB Cards		Unit
IEEE	PCMCIA		Min	Max	
t_{AVAV}	t_cR	Read Cycle Time	200		ns
t_{AVQV}	t_a (A)	Address Access Time		200	ns
t_{ELQV}	t_a (CE)	CE# Access Time		200	ns
t_{GLQV}	t_a (OE)	OE# Access Time		100	ns
t_{EHQZ}	t_{dis} (CE)	Output Disable Time from CE# Inactive		90	ns
t_{GHQZ}	t_{dis} (OE)	Output Disable Time from OE# Inactive		90	ns
t_{GLQX}	t_{en} (OE)	Output Enable Time from OE# Active(1)			ns
t_{ELQX}	t_{en} (CE)	Output Enable Time from CE# Active(1)			ns
t_{AXQX}		Data Hold from Address, CE#, or OE# Change (Whichever Occurs First)			ns
t_{ELGL}		CE# Setup Time to OE# Active			ns
t_{AVGL}		Address Setup Time to OE# Active			ns
t_{PHQV}		RDY/BSY# High to Output Delay		210	ns

NOTE:
1. Sampled, not 100% tested

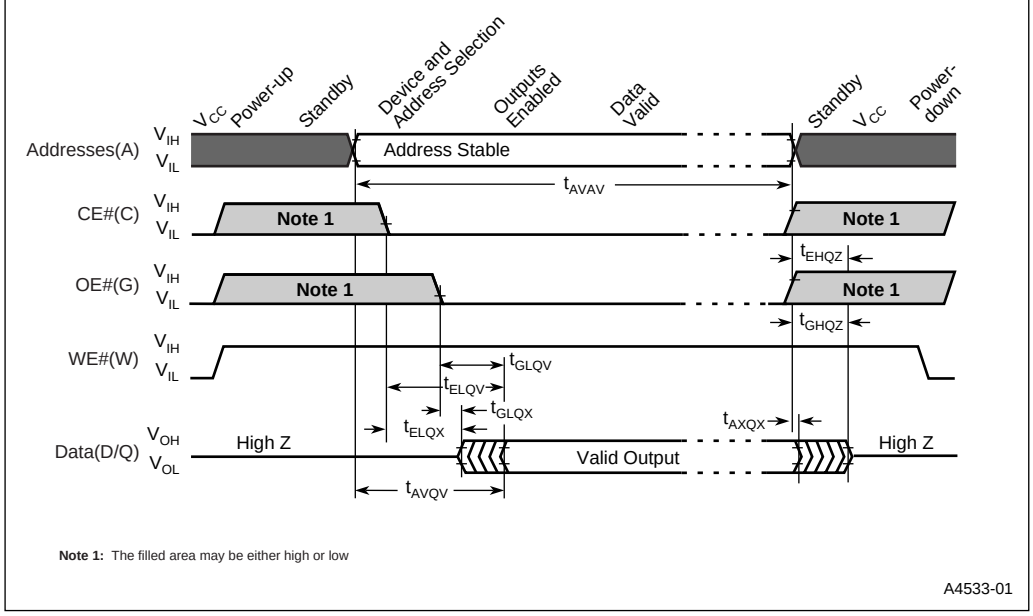


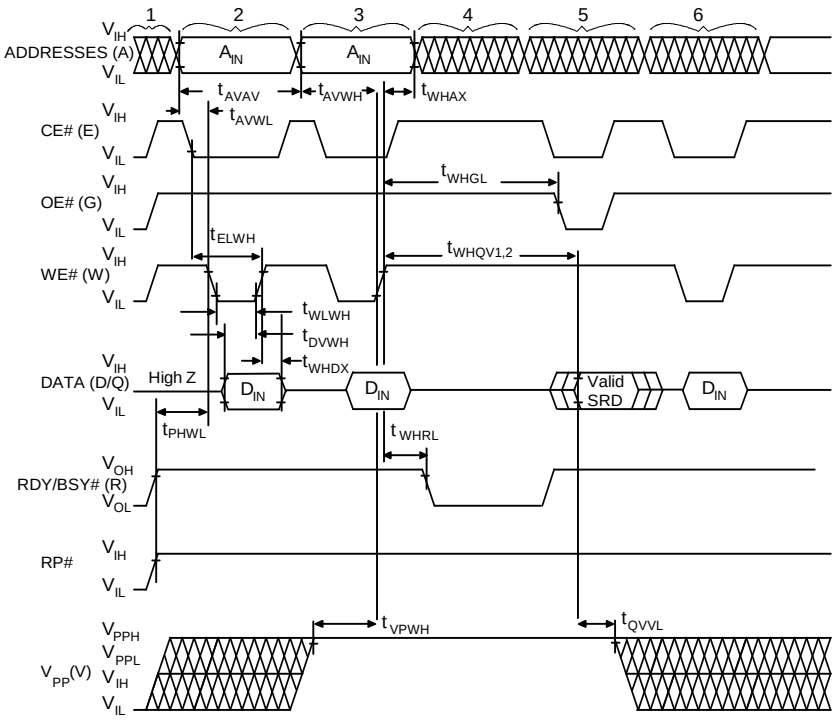
Figure 5. AC Waveforms for Read Operations

8.5.2 WRITE OPERATIONS(1, 2)

Symbol		Parameter	8 – 64-MB Cards		Unit
JEDEC	PCMCIA		Min	Max	
t_{AVAV}	t_cW	Write Cycle Time	200		ns
t_{WLWH}	t_w (WE)	WE# Pulse Width	120		ns
t_{AVWL}	t_{su} (A)	Address Setup Time to WE# Active	20		ns
t_{AVWH}	t_{su} (A-WEH)	Address Setup Time for WE#	140		ns
t_{ELWH}	t_{su} (CEWEH)	Card Enable Setup Time for WE#	140		ns
t_{DVWH}	t_{su} (D-WEH)	Data Setup Time for WE# Inactive	60		ns
t_{WHDX}	t_h (D)	Data Hold Time from WE# Inactive	30		ns
t_{WHAX}	t_{rec} (WE)	Write Recovery Time	30		ns
t_{WHGL}	t_h (OE-WE)	Output Enable Hold from WE#	10		ns
t_{WHRL}		WE# (CE#) Inactive Time to RDY/BSY# Active		90	ns

NOTES:

1. These timings apply only if both CE#s (CE_1# and CE_2#) are deasserted prior to WE# asserted.
2. Read timing characteristics during erase and write operations are the same as during read-only operations. Refer to *AC Characteristics* for read-only operations.



NOTES:

1. V_{CC} Power-Up and Standby
2. Write Program or Erase Setup Command
3. Write Valid Address and Program or Erase Confirm Command
4. Automated Program or Erase Delay
5. Read Status Register Data
6. Write Read Array Command

Figure 6. AC Waveforms for Write Operations

8.5.3 POWER-UP TIMING(1, 2)

Symbol	Parameter	Notes	Min	Max	Units
PCMCIA					
V_i (CE)	CE# Signal Level (0.0 V < V_{CC} < 2.0 V)	1	0	V_{iMAX}	V
	CE# Signal Level (2.0 V < V_{CC} < V_{IH})	1	V_{CC} – 0.1	V_{iMAX}	V
	CE# Signal Level (V_{IH} < V_{CC})	1	V_{IH}	V_{iMAX}	V
t_{su} (V_{CC})	CE# Setup Time		20		ms
t_{su} (RESET)	CE# Setup Time		20		ms
t_{rec} (V_{CC})	CE# Recover Time		1.0		µs
t_{pr}	V_{CC} Rising Time	2	0.1	300	ms
t_{pf}	V_{CC} Falling Time	2	3.0	300	ms
t_w (RESET)	RESET Width		10		µs
t_h (Hi-Z RESET)	RESET Width	3	36		µs
t_s (Hi-Z RESET)	RESET Width		0		ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0.0 V < V_{CC} < 2.0 V, V_i (CE#) is only 0.00 V ~ V_{iMAX}.
2. The t_{pr} and t_{pf} are defined as “linear waveforms” in the period of 10% to 90%, or vice-versa. Even if the waveform is not a “linear waveform,” its rising and falling time must meet this specification.
3. If RESET# is asserted while a block erase, write, or lock-bit configuration operation is not executing, then the minimum required RESET# Pulse Low Time is 1 µs.
4. A rest time, t_{PHQV} (reference Section 8.5.1) is required from BUSY# or RESET# going high until outputs are valid.

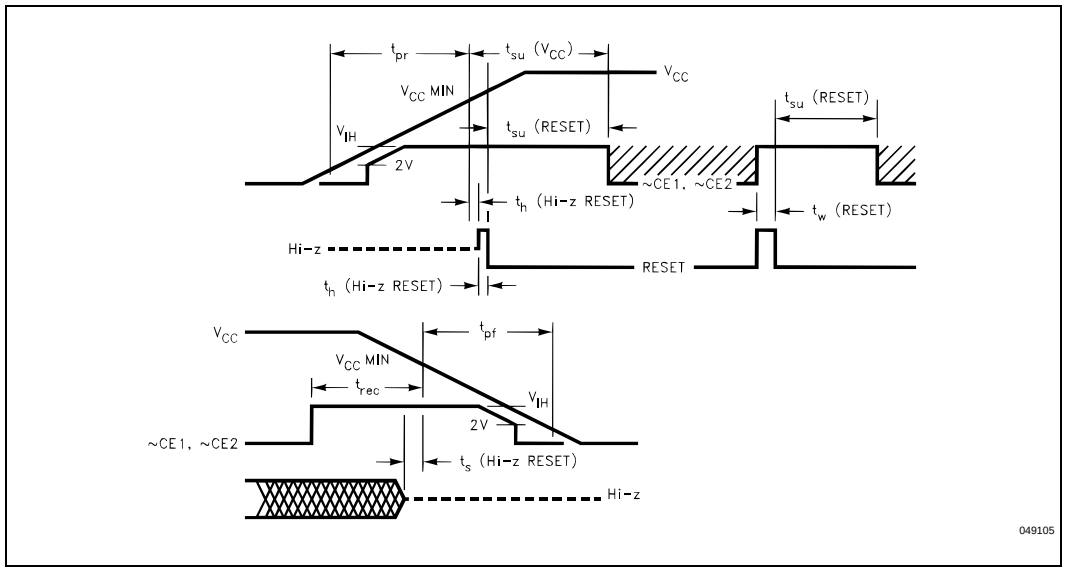


Figure 7. Power-Up Timing for Systems Supporting RESET#

8.6 Block Erase, Write, and Lock-Bit Configuration Performance(3,4)

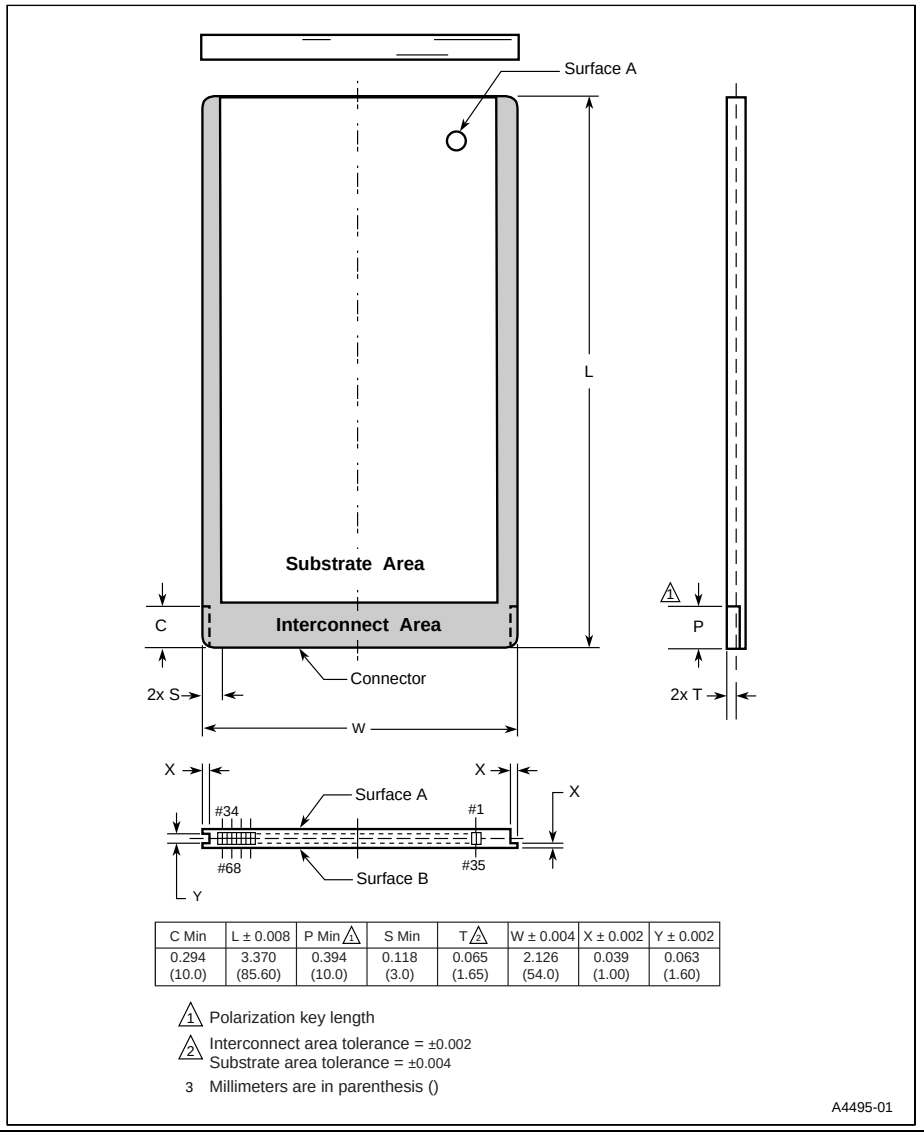
Sym	Parameter	Notes	Min	Typ(1)	Max	Units
t_{WHQV1} t_{EHQV1}	Write Buffer Word Write Time	2, 5, 6	TBD	6	TBD	µs
t_{WHQV2} t_{EHQV2}	Word Write Time (Using Word Write Command)	2, 6	TBD	180	TBD	µs
—	Block Write Time (Using Write to Buffer Command)	2, 6	TBD	0.8	TBD	sec
t_{WHQV4} t_{EHQV4}	Block Erase Time	2	TBD	0.7	TBD	sec
t_{WHQV5} t_{EHQV5}	Set Lock-Bit Time	2	TBD	32	TBD	µs
t_{WHQV6} t_{EHQV6}	Clear Block Lock-Bits Time	2	TBD	0.3	TBD	sec
t_{WHRH} t_{EHRH}	Erase Suspend Latency Time to Read			26	35	µs

NOTES:

1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. Excludes system-level overhead.
3. These performance numbers are valid for all speed versions.
4. Sampled but not 100% tested.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. The maximum write time is the absolute maximum time it takes the write algorithm to complete. The overwhelming majority of the bits are written within the typical value specified. To maximize system performance, the RDY/BSY# signal should be polled to determine the completion of a write operation.

9.0 PACKAGING

All 5 Volt Value Series 200 Flash Memory PC Cards have the PCMCIA Type 1 form factor. This figure shows the outside dimensions of a card. For complete mechanical drawings refer to the *PCMCIA PC Card Specification*.



C Min	L ± 0.008	P Min 1	S Min	T 2	W ± 0.004	X ± 0.002	Y ± 0.002
0.294 (10.0)	3.370 (85.60)	0.394 (10.0)	0.118 (3.0)	0.065 (1.65)	2.126 (54.0)	0.039 (1.00)	0.063 (1.60)

1 Polarization key length

2 Interconnect area tolerance = ±0.002
Substrate area tolerance = ±0.004

3 Millimeters are in parenthesis ()

A4495-01

10.0 ORDERING INFORMATION

iMC008FLSG, SBXXXXX

Where:

i	= INTEL
MC	= MEMORY CARD
008	= DENSITY IN MEGABYTES (008, 016, 024, 032, 048, 064 AVAILABLE)
FL	= FLASH TECHNOLOGY
S	= BLOCKED ARCHITECTURE
G	= REVISION
SBXXXXX	= CUSTOMER IDENTIFIER

11.0 ADDITIONAL INFORMATION

Order Number	Document
210830	*Flash Memory Databook*
290621	*5 Volt Value Series 200 Flash Memory Card Specification Update*
290606	*5 Volt Intel® StrataFlash™ Memory; 28F320J5 and 28F640J5* datasheet
292205	*AP-647 5 Volt Intel® StrataFlash™ Memory Design Guide*
292204	*AP-646 Common Flash Interface (CFI) and Command Sets*
292203	*AP-644 Migration Guide to Intel® StrataFlash™ Memory*
Note 3	*AP-374 Flash Memory Write Protection Techniques*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.intel.com for technical documentation and tools.
3. These documents can be located at the Intel World Wide Web support site, http://www.intel.com/support/flash/memory