Siliconix incorporated

D139
Monolithic 2-Channel FET Switch Driver

FEATURES

- Complementary Outputs
- 150 ns Propagation Time
- 30 V Output Swing
- Current Source Coupling
- TTL Compatible

BENEFITS

- Versatile
- Minimizes Switching Time
- Easily Interfaced

APPLICATIONS

- Interfaces Low Level Signal to FET Switches
- TTL to CMOS
- TTL to PROM Logic Levels
- Double-throw Switch Control

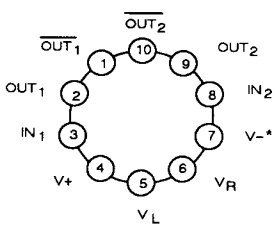
DESCRIPTION

The D139 is a dual low level to high level voltage translator with complementary outputs. Uses include bipolar to MOS logic interface and bipolar logic to FET analog switch control. The following characteristics of the input circuit provide an ideal interface to the common logic forms TTL, CMOS, and DTL: light loading (~1/3 TTL load) to "0" inputs, a 1.2 V trip point, and high input impedance with high breakdown to "1" inputs. The output can drive up to 30 V peak-to-peak into pure capacitive loads or moderate resistive loads. Current source coupling between the input and output and split power supplies allow wide flexibility in the actual output voltage levels. Complementary outputs permit maximum application versatility, allowing functions such a double-throw analog switch control. A positive logic "1" at the input provides a "1" at OUT and a "0" at $\overline{OUT}$.

The D139 is offered in 10-pin metal can, plus 14-pin PDIP, side braze and flat pack packages. Performance grades include military, A suffix (-55 to 125°C) and commercial, C suffix (0 to 70°C) temperature range.

PIN CONFIGURATION

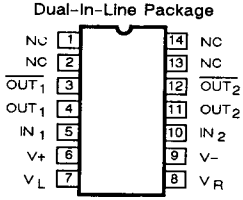
TO-100
Top View



Order Number: D139AA /883

*Common to Substrate and Case

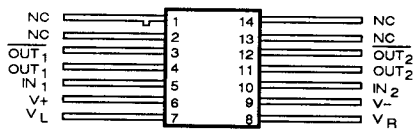
Dual-In-Line Package



Top View

Order Number:
Side Braze: D139AP/883
Plastic: D139CJ

Flat Package

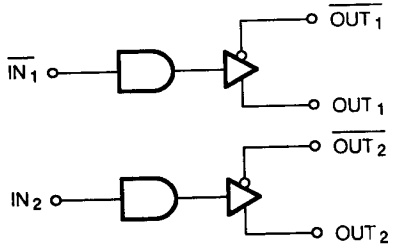


Order Number:
D139AL/883

8

Not Recommended for New Designs

FUNCTIONAL BLOCK DIAGRAM



LOGIC	OUT	$\overline{OUT}$
0	V-	V+
1	V+	V-

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.0 V

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 36 V
V+ to V_R ..... 36 V
V+ to V_O ..... 36 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V- ..... 36 V
V_L to V- ..... 36 V
V_O to V- ..... 36 V
V_L to V_{IN} ..... 8 V
CURRENT, (Any Terminal) DC ..... 12 mA
Peak Current (Any Terminal)
(200 µs pulse width, 100 pps) ..... 100 mA

Operating Temperature (A Suffix) ..... -55 to 125°C
(C Suffix) ..... 0 to 70°C
Storage Temperature (A Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C
Power Dissipation* (L Package)** ..... 900 mW
(P Package)*** ..... 825 mW
(A Package)**** ..... 450 mW
Thermal Resistance (θ_{JA}, J Package) ..... 0.16°C/mW

* All leads soldered or welded to PC board.
** Derate 10 mW/°C above 75°C.
*** Derate 11 mW/°C above 75°C.
**** Derate 6 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 10 V, V_L = 5 V, V- = -20 V, V_R = 0 V		LIMITS 1=25°C 2=125, 70°C 3=-55, 0°C TEMP	TYP [d]	A SUFFIX -55 to 125°C MIN [b]	A SUFFIX -55 to 125°C MAX [b]	C SUFFIX 0 to 70°C MIN [b]	C SUFFIX 0 to 70°C MAX [b]	UNIT
OUTPUT										
Output Voltage HIGH V+ to V_O	V_{OH}, $V_{\overline{OH}}$	V_{IH} = 2 V for V_{OH}	I_{OUT} = - 10 µA	1 2 3	0.6		0.9 0.7 1.1		0.9 0.7 1.1	V
			I_{OUT} = -2 mA	1,2,3	0.82		1.5		1.5	
Output Voltage LOW V_O to V-	V_{OL}, $V_{\overline{OL}}$	V_{IL} = 0.8 for V_{OL}	I_{OUT} = 10µA	1 2 3	0.52		1.1 0.9 1.3		1.1 0.9 1.3	
			I_{OUT} = 2 mA	1,2,3			1.5		1.5	
INPUT										
Input Current Voltage HIGH	I_{INH}	V_{IN} = 5 V		1 2	0.003		10 20		10 20	µA
Input Current Voltage LOW	I_{INL}	V_{IN} = 0 V		1,2 3	-18	-500 -600		-500 -600		

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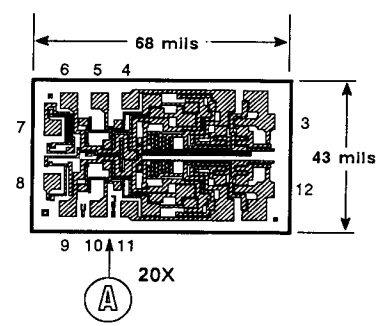
ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 10 V, V_L = 5 V, V− = −20 V, V_R = 0 V	LIMITS 1=25°C, 2=125, 70°C, 3=−55, 0°C		A SUFFIX −55 to 125°C		C SUFFIX 0 to 70°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC									
Switching Time LOW to High, Delay Plus Rise Time	$t_{(+)}$	See Switching Time Test Circuit C_L = 35 pF	1	65		170		170	ns
Switching Time HIGH to Low, Delay Plus Fall Time	$t_{(-)}$		1	90		200		200	
SUPPLY									
Positive Supply Current	I+	V_{IN} = 0 or 5 V	1	0.01		0.1		0.1	mA
Logic Supply Current	I_L		1	2.2		4		4	
Negative Supply Current	I−		1	−1.6	−3		−3		
Reference Supply Current Input Voltage HIGH	I_{RH}	V_{IN1} = V_{IN2} = 5 V	1	−0.66	−1.6		−1.6		
Reference Supply Current Input Voltage LOW	I_{RL}	V_{IN1} = V_{IN2} = 0 V	1	−0.63	−1.1		−1.1		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. All dc parameters are 100% tested at 25°C. Lots are sample-tested for ac parameters and HIGH and LOW temperature limits to assure conformance with specifications.

DIE TOPOGRAPHY



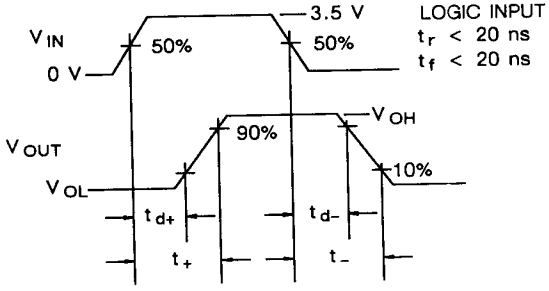
CMOA

4 Diodes
4 Capacitors
11 Resistors
4 P-channel enhancement MOSFET
10 PNP Bipolar Transistors
12 NPN Bipolar Transistors

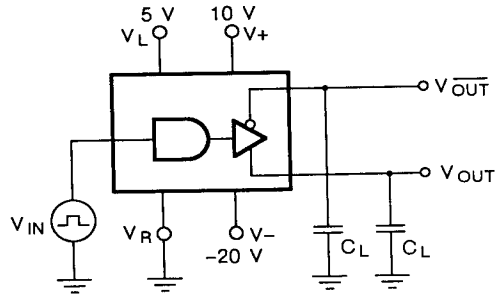
Pad No.	Function
3	$\overline{\text{Out 1}}$
4	Out 1
5	Input 1
6	V+
7	VL
8	VR
9	V− (Substrate)
10	Input 2
11	Out 2
12	$\overline{\text{Out 2}}$

8

SWITCHING TIME TEST CIRCUIT



($V_{\overline{OUT}}$ IS THE COMPLEMENT OF V_{OUT})



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