SUN MICROELECTRONICS

STP2016

July 1997

Clock-2 Generator

DATA SHEET — System Clock Generator

DESCRIPTION

The STP2016 Clock-2 Chip generates clock signals for components on the SBus and MBus. The MBus and SBus are used by SPARC™ processors, such as SuperSPARC™. The MBus is designed for multiprocessing (MP), operating at either 40 or 50 MHz with a 64-bit wide data path. The SBus is a multi-master bus primarily intended for I/O transactions with operation between 16 and 25 MHz.

The STP2016 generates the 40/50 MHz MBus clock signal by dividing the inputs from a 80/100 MHz crystal oscillator by two. The 20/25 SBus clock signal is derived in the same manner from the MBus clock signal.

Each component in the system that requires either bus clock receives a separate clock line. Because each chip receives a separate clock line, the skew between clock lines is the sum of the skew between the output drivers of the Clock-2 Chip and the trace skew. To minimize trace skew the clock traces to each chip are matched in delay. Both the SBus clock and the MBus clock have a 50% duty cycle.

Features

- Supports 50MHz MBus / 25 MHz SBus
- Generates SBus Clock from MBus Clock
- Generates 14 MBus clock lines with clock skew less than 1.0 ns between all MBus clocks
- Generates 6 SBus clock lines with clock skew less than 1.5 ns between SBus and MBus clocks
- Contains IEEE 1149.1 JTAG standard master control circuitry
- Contains Global Reset logic

Benefits

- Improved system performance
- SBus clock is synchronized with MBus clock
- System accuracy
- System accuracy
- Improved chip and board level testability

BLOCK, LOGIC AND APPLICATION DIAGRAMS

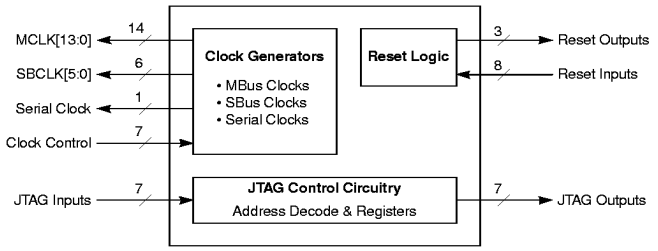


Figure 1. STP2016 Block Diagram

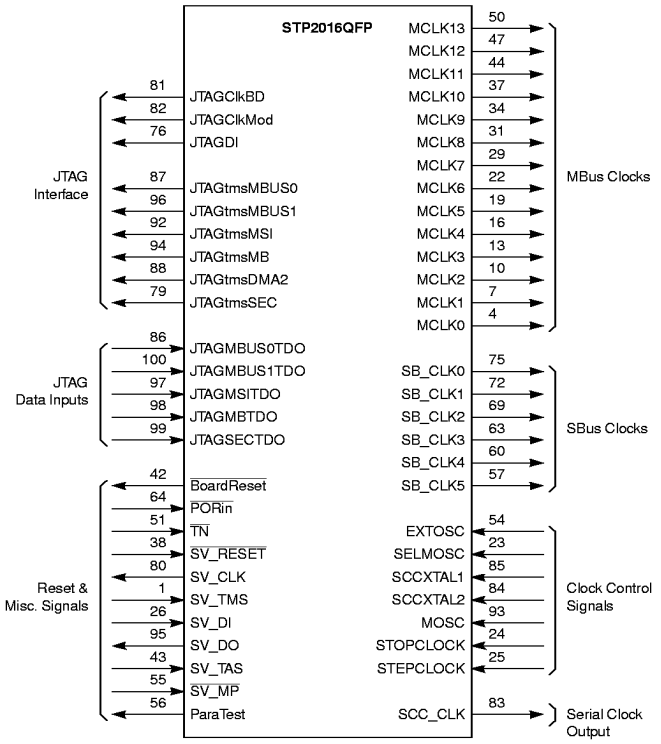


Figure 2. STP2016 Logical Connections

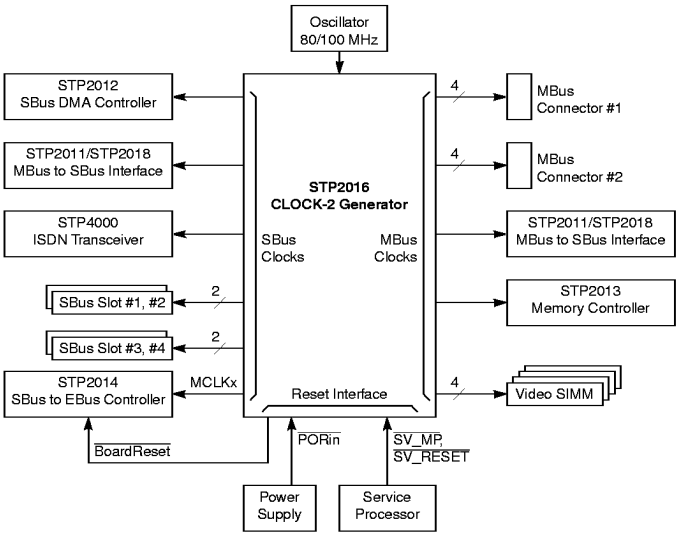


Figure 3. STP2016 Typical Application

SIGNAL DESCRIPTIONS

Signal	Type	Description
MCLK[13:0]	Output	40/50 MHz clock generated synchronously from a 80/100 MHz crystal.
SB_CLK[5:0]	Output	20/25 MHz clock generated synchronously from the 80/100 MHz crystal synchronized to the 40/50 MHz MBus clock
JTagClkBd	Output	Bd50% duty cycle Clock used to clock motherboard JTAG circuitry. Maximum frequency is 6.25 MHz.
JTagClkMod	Output	Mod50% duty cycle Clock used to clock MBus module JTAG circuitry. Maximum frequency is 6.25 MHz.
JTAG_DI	Output	JTAG Scan data input into scan ring.
JTAGMBTDO	Input	JTAG Scan data output out of scan ring.
JTAGtmsMBUS0	Output	JTAG MBus Module 0 Scan Ring Select.
JTAGtmsMBUS1	Output	JTAG MBus Module 1 Scan Ring Select.
JTAGtmsMSI	Output	JTAG MSBI (STP2011/STP2018) Scan Ring Select.
JTAGtmsMB	Output	JTAG Motherboard Scan Ring Select.
JTAGtmsDMA2	Output	JTAG DMA2 (STP2012) Scan Ring Select.
JTAGtmsSEC	Output	JTAG SEC (STP2014) Scan Ring Select.
JTAGMSITDO	Input	JTAG Data input from MSBI (STP2011/STP2018).
JTAGMBTDO	Input	JTAG Data input from Motherboard Ring.
JTAGSECTDO	Input	JTAG Data input from SEC (STP2014).
JTAGMBUS0TDO	Input	JTAG Data input from MBus 0.
JTAGMBUS1TDO	Input	JTAG Data input from MBus 1.
$\overline{\text{SV\_RESET}}$ [1]	Input	Service Processor Reset - Asserted to initialize the system.
SV_CLK [1]	Input	Service Processor Clock - Data is shifted serially on the falling edge of this clock. Data is sampled on the rising edge of this signal. The cycle time is 200ns = 5 MHz.
SV_TMS [1]	Input	Service Processor Mode Select - Used to select between shifting data into the system or capture data in the system. Some systems have more than one scan ring and hence a separate TMS for each ring.
SV_DI [1]	Input	Service Processor Data In - used to shift data into the selected device on the falling edge of SV_CLK.
SV_D0 [1]	Output	Service Processor Data Out - Used to shift data out of the selected device on the falling edge of SV_CLK.
SV_TAS [1]	Input	Service Processor Address Strobe - High = allows data to be clocked in to JTAG chips.
$\overline{\text{SV\_MP}}$ [1]	Input	Service Processor Master Present - This signal is asserted to indicate that a service processor is present in the system. This is not part of the IEEE P.1149.1 JTAG Standard.
ParaTest	Output	Parametric Test Output - always active.
$\overline{\text{TN}}$	Input	Turns off three-state Outputs for testing errors.
$\overline{\text{PORin}}$	Input	Power On Reset used to generate $\overline{\text{ResetOut}}$.
$\overline{\text{BoardReset}}$	Output	Generated from $\overline{\text{PORin}}$ or $\overline{\text{SV\_Reset}}$ & $\overline{\text{SV\_MP}}$ and used to reset the motherboard.

SIGNAL DESCRIPTIONS (CONTINUED)

Signal	Type	Description
SCCXTAL1	Input	4.9152 MHz crystal input used to generate the serial clock.
SCCXTAL2	Input	4.9152 MHz crystal input used to generate the serial clock.
SCC_CLK	Output	Serial Clock output generated by the 4.9152 MHz crystal.
STOPCLOCK	Input	When high stops MBus and SBus clocks in their current phase.
STEPCLOCK	Input	When high steps MBus clock one cycle, and correspondingly steps SBus one-half cycle.
MOSC	Input	80/100 MHz oscillator input from 80/100 MHz TTL-can. One of two clock inputs.
EXTOSC	Input	External oscillator input, second clock input.
SELMOSC	Input	Selects between 80/100 MHz clock input and EXTOSC clock input. High selects MOSC = 80/100 MHz input, low selects EXTOSC input.

1. Service Processor is an external workstation installed with scan tool for inserting scan data to the target motherboard.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings [1]

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	5.25	V
V_I	Input voltage (any pin)	$GND \le V_{IN} \le V_{CC}$	V
P_D	Power dissipation	400	mW

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply voltage	4.75	5.0	5.25	V
T_A	Ambient temperature	0	–	55	°C
f_{OSC}	Frequency of operation	–	–	80/100	MHz

DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
V_{IH}	High Level Input Voltage		2.0	–	V
V_{IL}	Low Level Input Voltage		–	0.8	V
V_{OH}	High Level Output Voltage	4 mA Buffer, I_{OH} = -4 mA [1]	2.4	–	V
		8 mA Buffer, I_{OH} = -8 mA [2]	2.4	–	V
		12 mA Buffer, I_{OH} = -12 mA [3]	2.4	–	V
V_{OL}	Low Level Output Voltage	4 mA Buffer, I_{OL} = 4 mA [1]	–	0.4	V
		8 mA Buffer, I_{OL} = 8 mA [2]	–	0.4	V
		12 mA Buffer, I_{OL} = 12 mA [3]	–	0.4	V
I_{IL}	Input Leakage Current		–	10	µA
I_{OL}	Output Leakage Current		–	10	µA
C_{OUT}	Output Capacitance		–	10	pF
C_{IN}	Input Capacitance		–	10	pF

1. 4 mA Output Buffer Signals - SCC_CLK, JTAGDI, JTAGtmsMBUS0, JTAGtmsMBUS1, JTAGtmsMSI, JTAGtmsMB, JTAGtmsDMA2, JTAGtmsSEC, SV_DO, ParaTest
2. 8 mA Output Buffer Signals - $\overline{\text{BoardReset}}$
3. 12 mA Output Buffer Signals - MCLK[13:0], SB_CLK[5:0], JTAGClkBd, JTAGClkMod

AC Characteristics

Symbol	Parameter	Min	Max	Unit
t_{M-M}	all MCLKs	0	1.0	ns
t_{S-M}	SCLKs to MCLKs	0	1.5	ns

TIMING DIAGRAMS

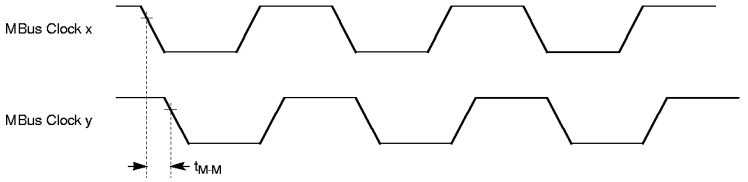


Figure 4. Timing Relationship Between MBus Clocks

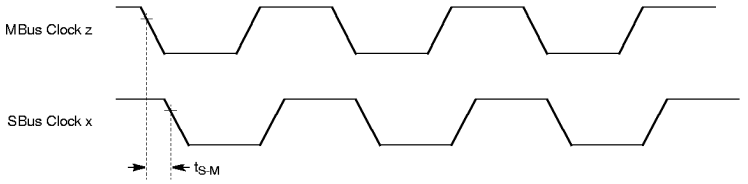
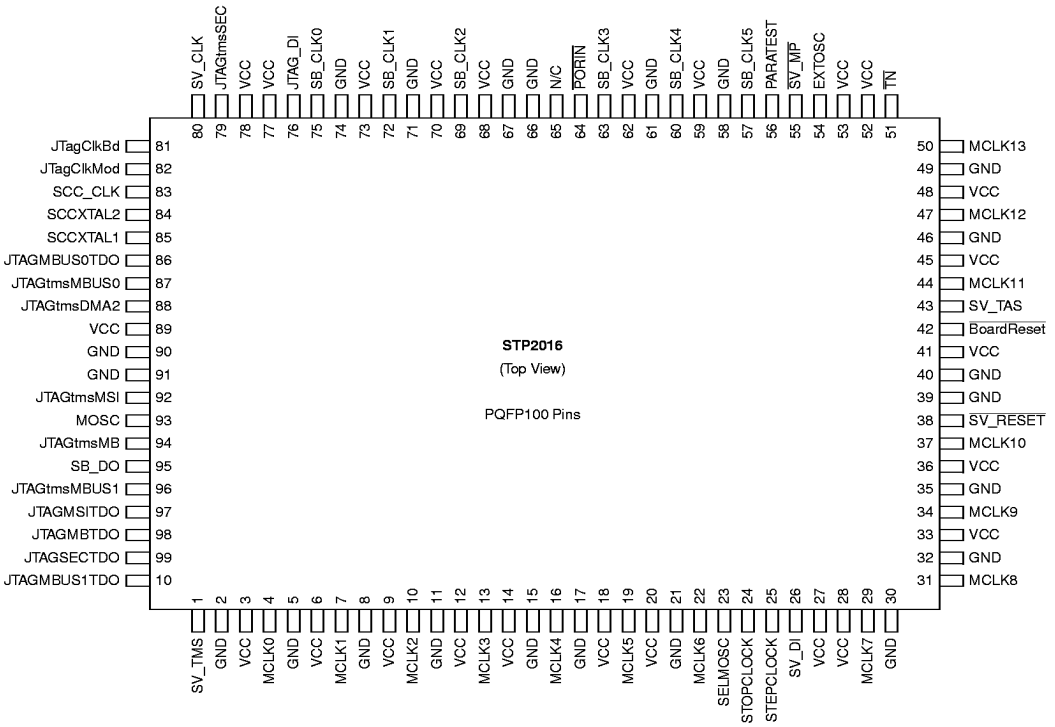


Figure 5. Timing Relationship Between SBus Clocks and MBus Clocks

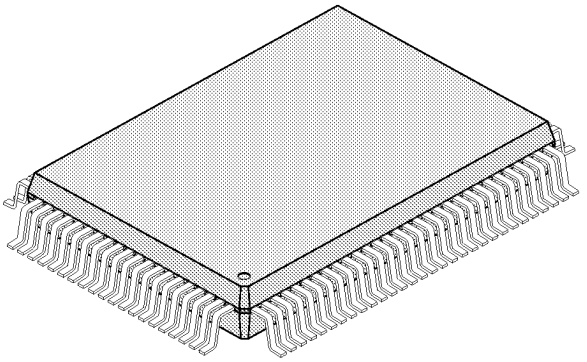
PACKAGE INFORMATION

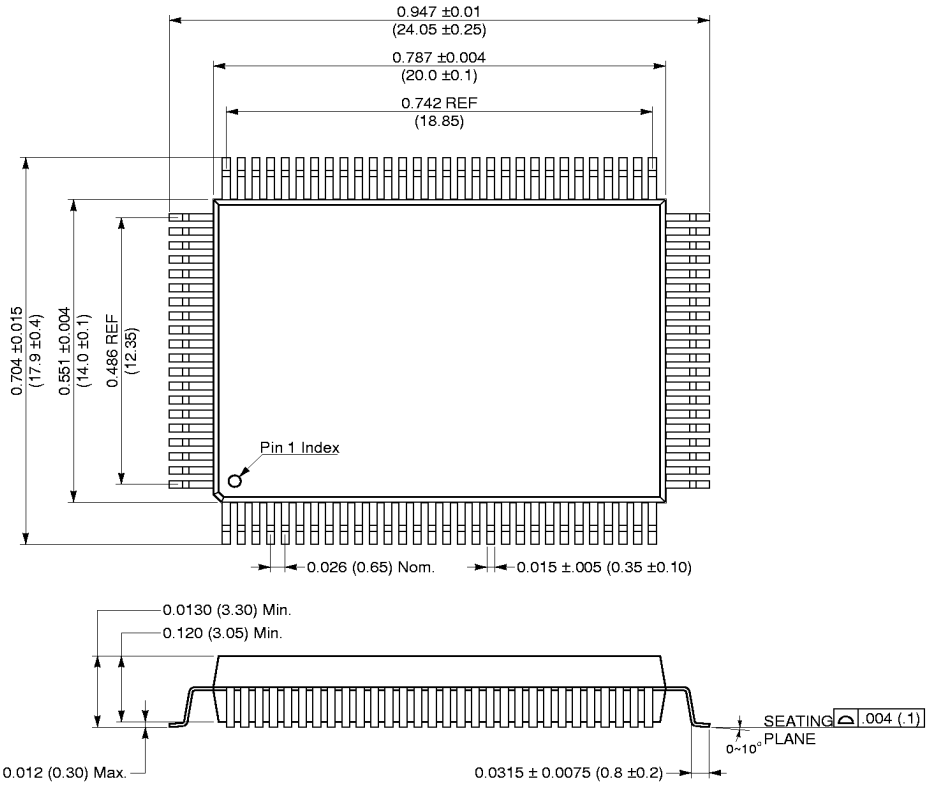
100-Pin PQFP Pin Assignment

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	SV_TMS	18	VCC	35	GND	52	VCC	69	SB_CLK2	86	JTAGMBUS0TDO
2	GND	19	MCLK5	36	VCC	53	VCC	70	VCC	87	JTAGtmsMBUS0
3	VCC	20	VCC	37	MCLK10	54	EXTOSC	71	GND	88	JTAGtmsDMA2
4	MCLK0	21	GND	38	$\overline{\text{SV\_RESET}}$	55	$\overline{\text{SV\_MP}}$	72	SB_CLK1	89	VCC
5	GND	22	MCLK6	39	GND	56	PARATEST	73	VCC	90	GND
6	VCC	23	SELMOSC	40	GND	57	SB_CLK5	74	GND	91	GND
7	MCLK1	24	STOPCLOCK	41	VCC	58	GND	75	SB_CLK0	92	JTAGtmsMSI
8	GND	25	STEPCLOCK	42	$\overline{\text{BoardReset}}$	59	VCC	76	JTAG_DI	93	MOSC
9	VCC	26	SV_DI	43	SV_TAS	60	SB_CLK4	77	VCC	94	JTAGtmsMB
10	MCLK2	27	VCC	44	MCLK11	61	GND	78	VCC	95	SV_DO
11	GND	28	VCC	45	VCC	62	VCC	79	JTAGtmsSEC	96	JTAGtmsMBUS1
12	VCC	29	MCLK7	46	GND	63	SB_CLK3	80	SV_CLK	97	JTAGMSITDO
13	MCLK3	30	GND	47	MCLK12	64	$\overline{\text{PORIN}}$	81	JTagClkBd	98	JTAGMBTDO
14	VCC	31	MCLK8	48	VCC	65	N/C	82	JTagClkMod	99	JTAGSECTDO
15	GND	32	GND	49	GND	66	GND	83	SCC_CLK	100	JTAGMBUS1TDO
16	MCLK4	33	VCC	50	MCLK13	67	GND	84	SCCXTAL2		
17	GND	34	MCLK9	51	$\overline{\text{TN}}$	68	VCC	85	SCCXTAL1		



100-Pin PQFP Package Dimensions





Dimensions in inches, dimensions in brackets in (millimeters).

ORDERING INFORMATION

Part Number	Description
STP2016QFP	100-Pin Plastic Quad Flat Pack (PQFP)

Document Part Number: STP2016