

SEC

DATA SHEET**SBus-to-EBus Controller**

DESCRIPTION

The STP2014 SBus-to-EBus Controller (SEC) is an interface between the SBus and the EBus that is used for slow I/O devices such as TOD, EPROM, serial port, and keyboard/mouse. The STP2014 also houses the interrupt control and steering logic, the timer/counter registers, reset logic, and miscellaneous registers. The STP2014 is physically located on the SBus. However, the STP2104 does not follow the SBus protocol completely. For instance, in order to save pins on chip, address and data are multiplexed. Therefore, all references to the SBus in this document really refer to the pseudo SBus implementation.

FEATURES

- Supports byte, halfword, word, and doubleword transfers
- Built in scan capability
- Supports early write acknowledge
- 160-pin PQFP package

BLOCK, LOGIC, AND TYPICAL APPLICATION DIAGRAMS

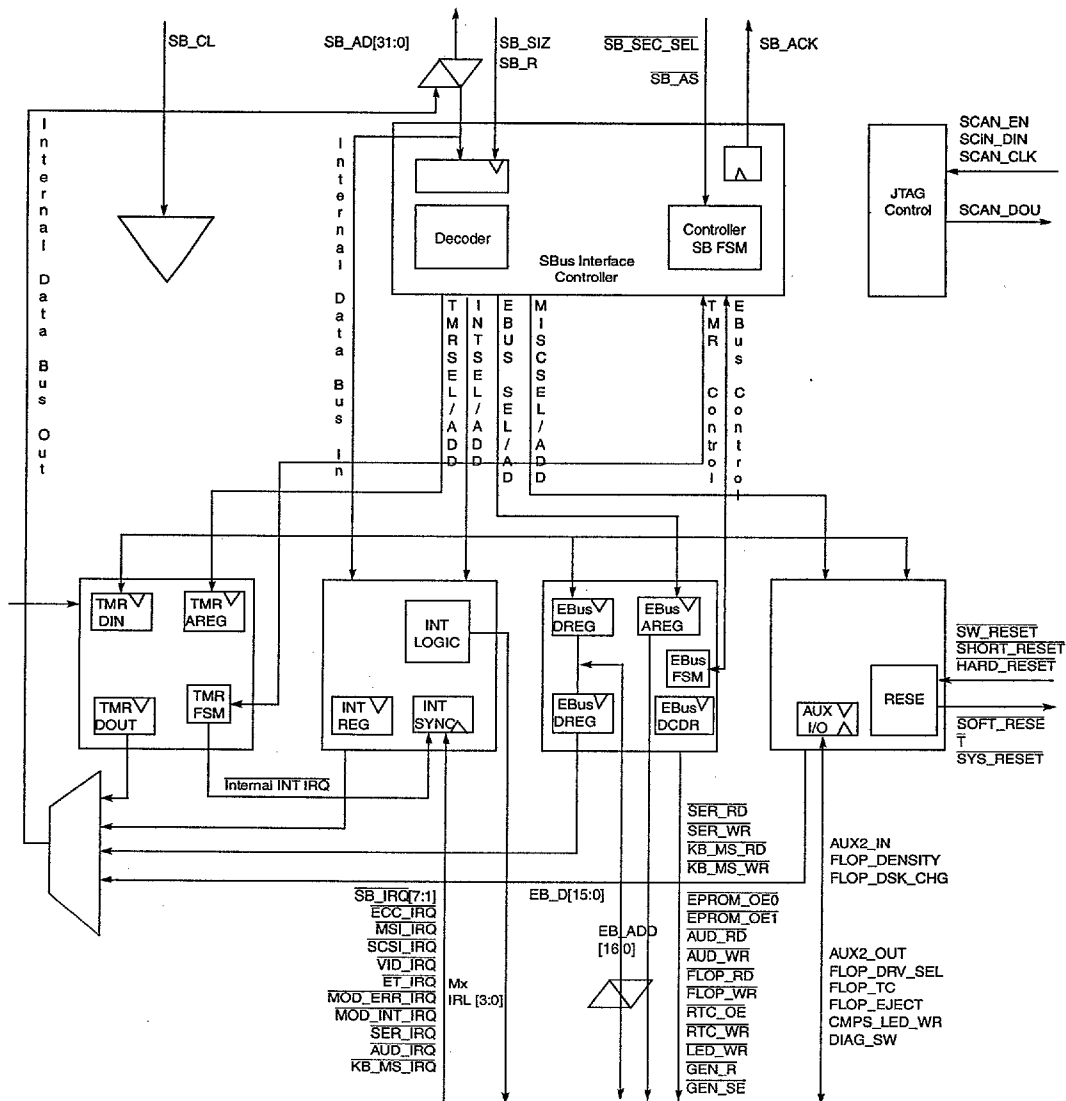


Figure 1. STP2014 Block Diagram

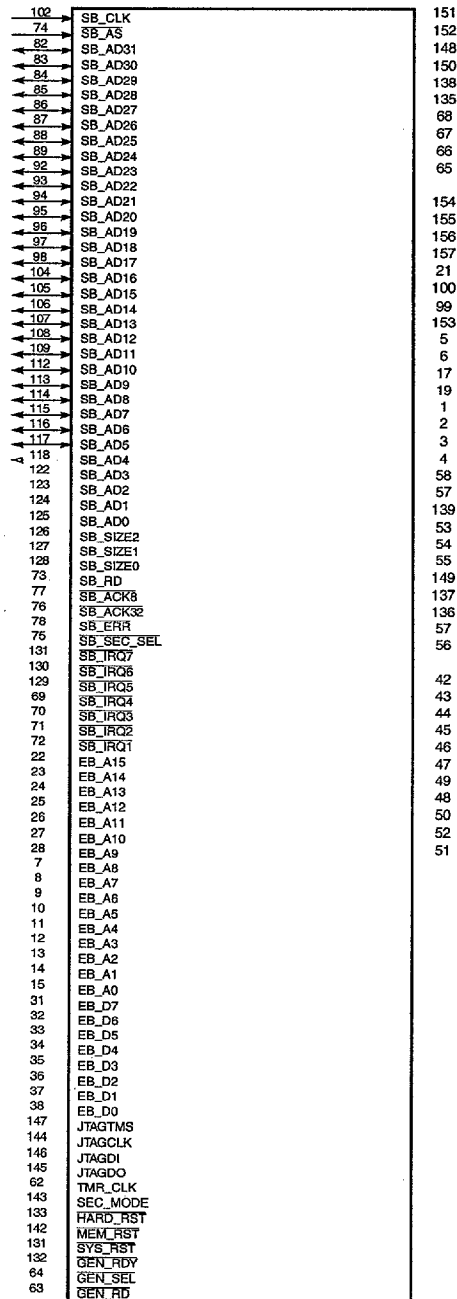


Figure 2. STP2014 Logical Connections

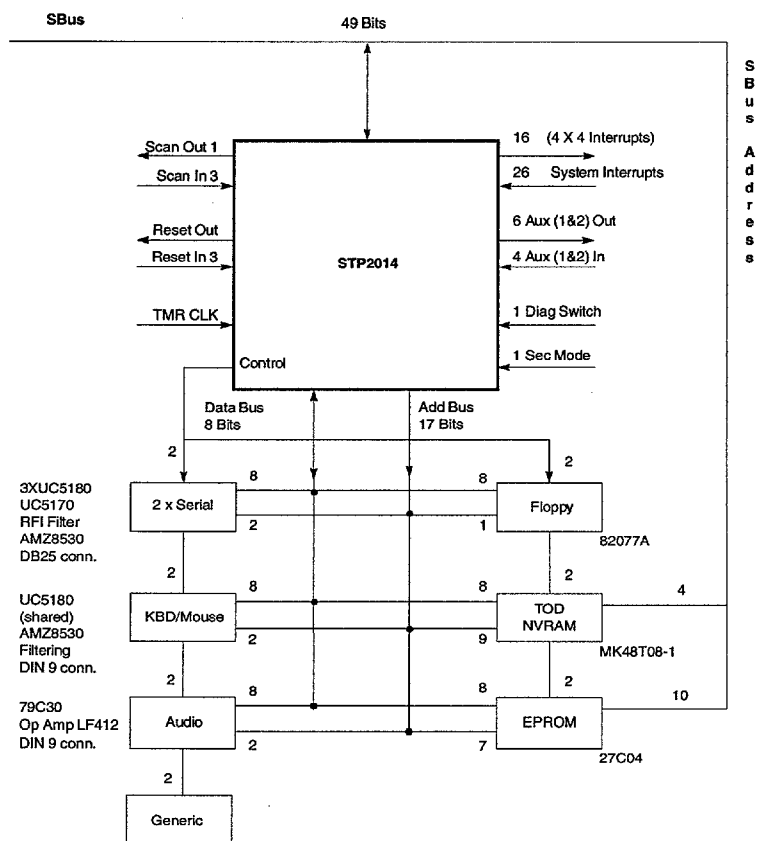


Figure 3. STP2014 Typical Application

SIGNAL DESCRIPTIONS

SBus Interface

Signal	Type	Description
SB_CLK	Input	SBus clock
SB_AS	Input	SBus address strobe
SB_AD[31:0]	Input/Output	SBus data bus
SB_SIZE[2:0]	Input/Output	SBus size
SB_RD	Input/Output	SBus read
SB_ACR[8, 32]	Input/Output	SBus acknowledge
SB_ERR	Output	SBus error
SB_SEC_SEL	Input	SBus slave select
SB_IRQ[7:1]	Output	SBus interrupt request

External Bus Interface

Signal	Type	Description
EB_A[15:0]	Output	External bus address
EB_D[7:0]	Input/Output	External bus data

Auxiliary Ports 1 and 2

Signal	Type	Description
AUX2IN[1:0]	Input	Auxiliary register 2 input
AUX2OUT[1:0]	Output	Auxiliary register 2 output
AUX1IN[1:0]	Input	Auxiliary register 1 input
AUX1OUT[3:0]	Output	Auxiliary register 1 output

Interrupt Controller Interface

Signal	Type	Description
M3_IRL[3:0]	Output	Processor 3 interrupt lines
M2_IRL[3:0]	Output	Processor 2 interrupt lines
M1_IRL[3:0]	Output	Processor 1 interrupt lines
M0_IRL[3:0]	Output	Processor 0 interrupt lines
MOD_IRQ	Input	Module interrupt request
AERR	Input	Asynchronous error
VID_IRQ	Input	Video interrupt request
SER_IRQ	Input	Serial interrupt request
KB_MS_IRQ	Input	Keyboard/mouse interrupt request
AUD_IRQ	Input	Audio interrupt request
FLOP_IRQ	Input	Floppy interrupt request
MSI_CNTRL_IRQ	Input	Mbus/SBus controller interrupt request
MEMCTL_IRQ	Input	Memory controller interrupt request
ET_IRQ	Input	Ethernet interrupt request
SCSI_IRQ	Input	SCSI interrupt request

Read/Write Controls

Signal	Type	Description
SER_RD	Output	Serial port read
SER_WR	Output	Serial port write
KB_MS_RD	Output	Keyboard/mouse read
KB_MS_WR	Output	Keyboard/mouse write
AUD_RD	Output	Audio read
AUD_WR	Output	Audio write
RTC_WR	Output	TOD write
RTC_OE	Output	TOD output enable
FLOPPY_RD	Output	Floppy read
FLOPPY_WR	Output	Floppy write
EPROM_OE0	Output	EPROM output enable

Miscellaneous

Signal	Type	Description
JTAGTMS	Input	JTAG mode select
JTAGCLK	Input	JTAG clock
JTAGDI	Input	JTAG data input
JTAGDO	Output	JTAG data output
TMR_CLK	Input	Counter timer clock
SEC_MODE	Input	Mode: 0 = Reserved, 1 = System
HARD_RST	Input	System reset input
MEM_RST	Output	Memory reset output
SYS_RST	Output	System reset output
GEN_RDY	Input	Generic port ready
GEN_SEL	Output	Generic port write
GEN_RD	Output	Generic port read

ELECTRICAL SPECIFICATIONS***Absolute Maximum Ratings^[1]***

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply voltage	-0.5	7.0	V
V _{IN}	Input voltage	-0.5 ¹	7.0	V
T _{ST}	Storage temperature	-65	150	°C
T _{CASE}	Operating temperature	0	85	°C

1. V_{IN} MIN = -3.0 V for pulse width less than 15 ns.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V _{CC}	DC supply	4.75	5.25	V
T _A	Ambient temperature	0	70	°C

Capacitance

Symbol	Parameter	Min	Max	Units
	Pin loading capacitance	20	45	pF

DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IL}	Voltage input low		–	0.8	V
V_{IH}	Voltage input high		2.0	–	
V_{OL}	Voltage output low	$I_{OL} = 1.0 \text{ mA}$ $I_{OL} = 2.0 \text{ mA}$ $I_{OL} = 4.0 \text{ mA}$ $I_{OL} = 6.0 \text{ mA}$ $I_{OL} = 8.0 \text{ mA}$	–	0.4	V
V_{OH}	Voltage output high	$I_{OH} = -1.0 \text{ mA}$ $I_{OH} = -2.0 \text{ mA}$ $I_{OH} = -4.0 \text{ mA}$ $I_{OH} = -6.0 \text{ mA}$ $I_{OH} = -8.0 \text{ mA}$	2.4	–	V
I_{IL}	Input leakage current low TTL input, without pullup TTL input, with pullup Bidirect 1 mA, with pullup Bidirect 2 mA, hold amp Bidirect 4 mA Bidirect 6 mA, hold amp	$V_{IN} = 0.0 \text{ V}, V_{DD}$ $V_{IN} = 0 \text{ V}$ $V_{IN} = 0.0 \text{ V}$ $V_{IN} = 0.40 \text{ V}$ $V_{IN} = 0.0 \text{ V}$ $V_{IN} = 0.40 \text{ V}$	–10 –175 –290 45 –10 45	– – –45 160 – 160	μA
I_{IH}	Input leakage current high TTL input, without pullup TTL input, with pullup Bidirect 1 mA, with pullup Bidirect 2 mA, holding amp Bidirect 4 mA Bidirect 6 mA, holding amp	$V_{IN} = V_{DD}$ $V_{IN} = 3.5 \text{ V}$ $V_{IN} = V_{DD}$ $V_{IN} = 2.40 \text{ V}$ $V_{IN} = V_{DD}$ $V_{IN} = 2.40 \text{ V}$	– – NA –175 NA –175	10 –2.00 40 –715 10 –715	μA
I_{OZ}	3-state output leakage current, w/ pullup	$V_O = \text{GND}, V_O = V_{CC}$	–10	10	μA
I_{OSN}	3-state bidirect or output buffer 1 mA drive 2 mA drive 4 mA drive 6 mA drive 8 mA drive	$V_{OUT} = V_{DD}$	7.50 15.00 30.00 45.00 60.00	35.00 70.00 140.00 210.00 280.00	mA
I_{OSP}	3-state bidirect or output buffer 1 mA drive 2 mA drive 4 mA drive 6 mA drive 8 mA drive	$V_{OUT} = 0 \text{ V}$	–6.25 –12.50 –25.00 –37.50 –50.00	–35.00 –70.00 –140.00 –210.00 –280.00	mA
I_{CC}	Dynamic supply current			160	mA
I_{CC}	Quiescent current	$V_{IN} = V_{CC} \text{ or GND}, V_{CC} = \text{Max}$		2.0	mA

AC Characteristics: SBus Interface Signals

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{si}	SB_AS	SB_CLK	Min		15	120
T_{hi}	SB_SIZ[2:0]	SB_CLK	Min		0	60
	SB_RD	SB_CLK				
T_{si}	SB_SEC_SEL	SB_CLK	Min		15	
T_{hi}		SB_CLK	Min		0	
T_{si}	SB_D[31:0]	SB_CLK	Min		15	120
T_{hi}		SB_CLK	Min		0	60
T_{do}		SB_CLK	Max		30	120
T_{ho}		SB_CLK	Min		0	60
T_{do}	SB_ACK32	SB_CLK	Max		30	120
T_{ho}	SB_ACK8	SB_CLK	Min		0	60
	SB_ERR					
T_{si}	SB_RESET	SB_CLK	Min		15	120
T_{hi}	Applicable only for deassertion	SB_CLK	Min		0	6
	SB_IRQ[7:1]	ASYNC				

AC Characteristics: EBus Interface Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T_{do}	EB_A[16:0]	SB_CLK	Max		25	125.5
T_{ho}		SB_CLK	Min		0	
T_{do}	EB_D[15:0]	SB_CLK	Max		25	158.5
T_{ho}		SB_CLK	Min		0	
T_{si}		SB_CLK	Min		10	
T_{hi}		SB_CLK	Min		0	

1. 37.5 pF trace load

AC Characteristics: Serial Port Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	SER_RD	SB_CLK	Max		25	47.5
T _{ho}	SER_WR	SB_CLK	Min		0	
	SER_IRQ	ASYNC				

1. 37.5 pF trace load

AC Characteristics: Keyboard/Mouse Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	KB_MS_RD	SB_CLK	Max		25	47.5
T _{ho}	KB_MS_WR	SB_CLK	Min		0	
	KB_MS_IRQ	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: EPROM Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	EPROM_OE0	SB_CLK	Max		25	77.5
T _{ho}	EPROM_OET	SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: Audio Port Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	AUD_WR	SB_CLK	Max		25	47.5
T _{ho}	AUD_RD	SB_CLK	Min		0	
	AUD_IRQ	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: Floppy Port Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	FLOP_RD	SB_CLK	Max		25	47.5
T _{ho}	FLOP_WR	SB_CLK	Min		0	
	FLOP_IRQ	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: AUX 1 and 2 I/O Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
	FLOP_DENSITY FLOP_DSK_CHG AUX2_OUT	ASYNC				
T _{do}	FLOP_DRV_SEL	SB_CLK	Max		25	47.5
T _{ho}	FLOP_TC FLOP_EJECT LED_WR AUX2_OUT	SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: TOD Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	RTC_OE	SB_CLK	Max		25	44.5
T _{ho}	RTC_WR	SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: LED Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	LED_WR	SB_CLK	Max		25	47.5
T _{ho}		SB_CLK	Min		0	

1. 37.5 pF trace load assumed

AC Characteristics: Generic Port Signals^[1]

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
T _{do}	GEN_RD	SB_CLK	Max		25	-47.5
T _{ho}	GEN_SEL	SB_CLK	Min		0	
	GEN_RDY	ASYNC				

1. 37.5 pF trace load assumed

AC Characteristics: Interrupt Signals (not previously listed)

Parameter	Signal Name	Ref Edge	MIN/MAX	Timing (ns)		Load (pF)
				Test	Sys	
	VME_IRQ[7:1] MSI_CTRL_IRQ ECC_IRQ SCSI_IRQ[1:0] ET_IRQ MOD_INT_IRQ MOD_ERR_IRQ VID_IRQ	ASYNC				
T _{do}	M0_IRL[3:0]	SB_CLK	Max		30	20
T _{ho}	M1_IRL[3:0] M2_IRL[3:0] M3_IRL[3:0]	SB_CLK	Min		0	

TIMING DIAGRAMS

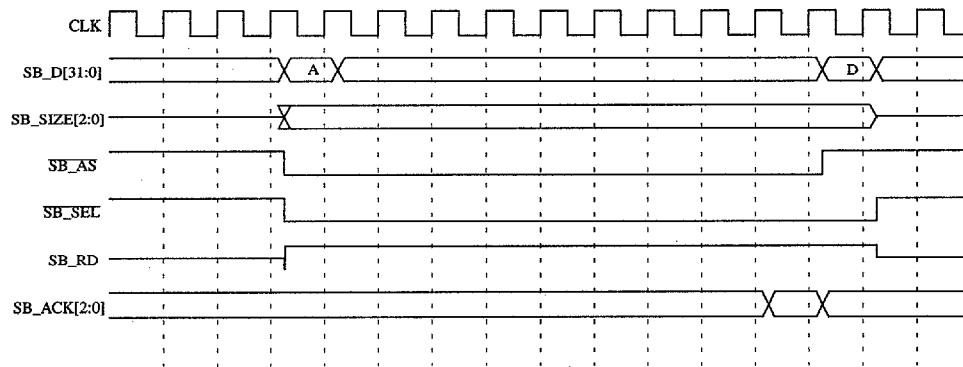


Figure 4. EPROM Byte Read

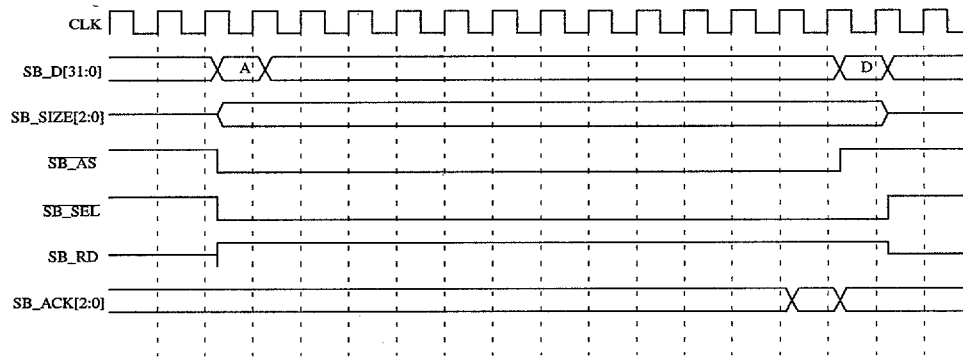
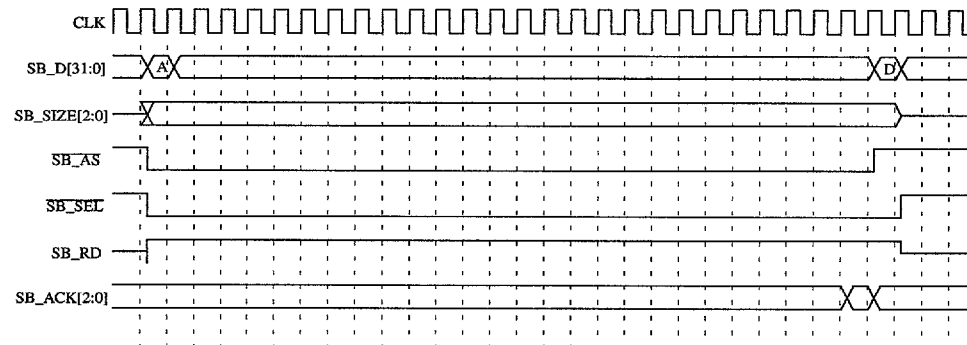
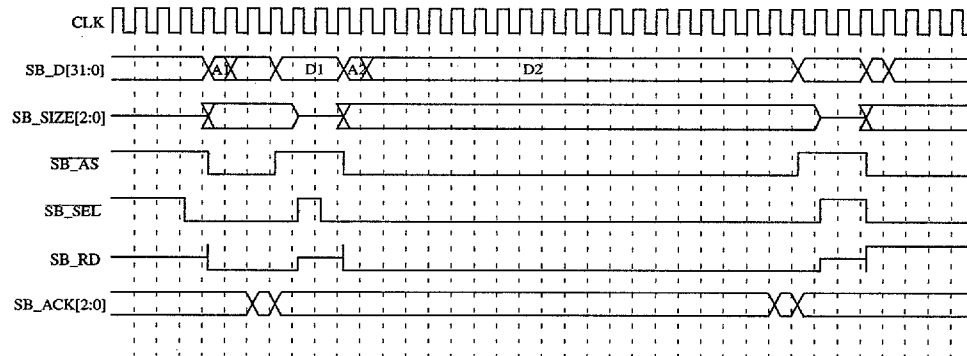


Figure 5. EPROM Word Read



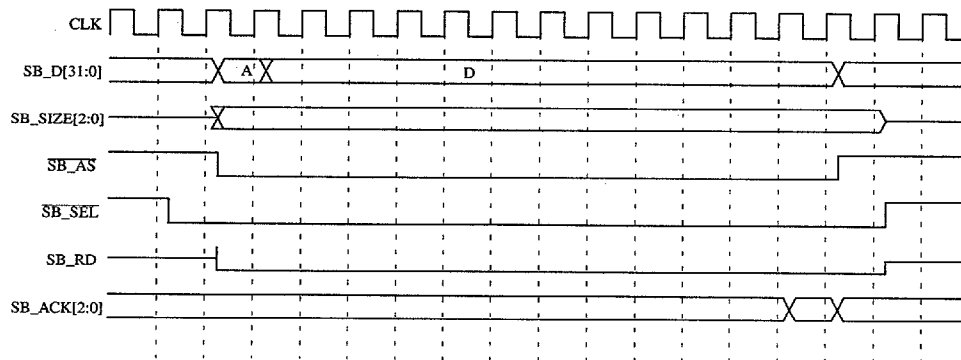


Figure 8. RTC (NVRAM, TOD) Write

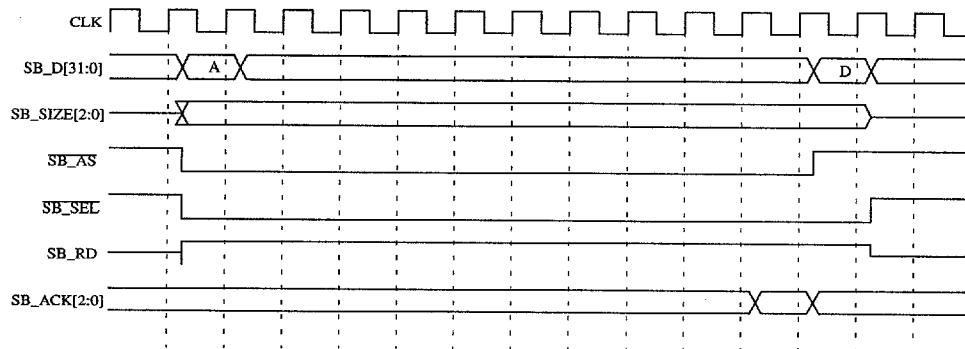


Figure 9. NTC (NVRAM, TOD) Read

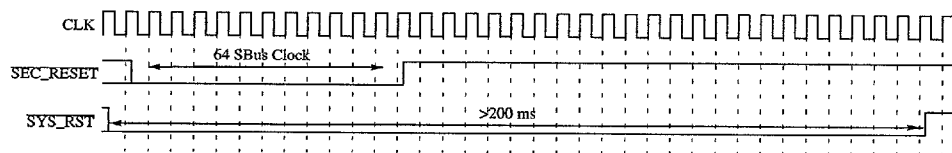


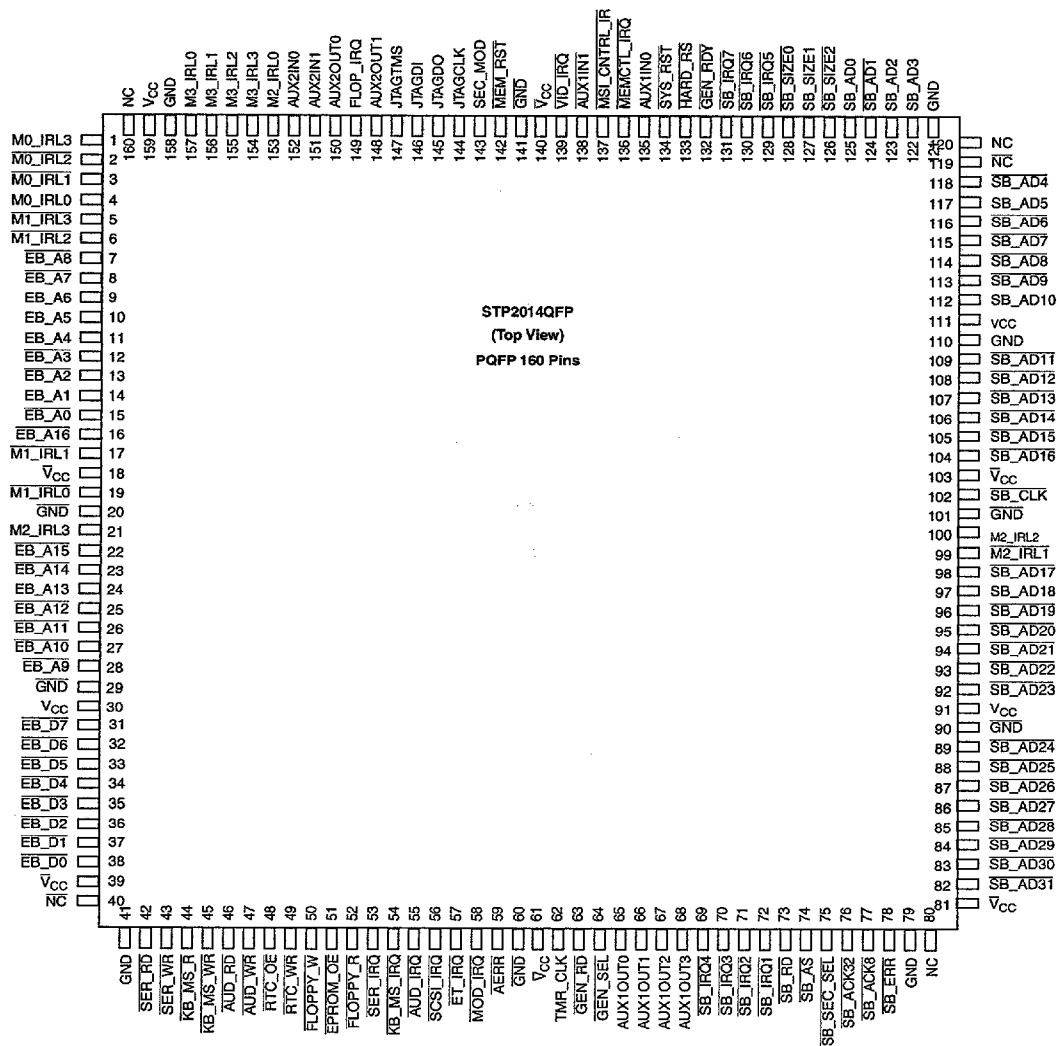
Figure 10. Hard Reset (Not Drawn to Scale)

PACKAGE INFORMATION

160-Pin PQFP Pin Assignments

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	M0_IRL3	33	EB_D5	65	AUX1OUT0	97	SB_AD18	129	SB_IRQ5
2	M0_IRL2	34	EB_D4	66	AUX1OUT1	98	SB_AD17	130	SB_IRQ6
3	M0_IRL1	35	EB_D3	67	AUX1OUT2	99	M2_IRL1	131	SB_IRQ7
4	M0_IRL0	36	EB_D2	68	AUX1OUT3	100	M2_IRL2	132	GEN_RDY
5	M1_IRL3	37	EB_D1	69	SB_IRQ4	101	GND	133	HARD_RST
6	M1_IRL2	38	EB_D0	70	SB_IRQ3	102	SB_CLK	134	SYS_RST
7	EB_A8	39	VCC	71	SB_IRQ2	103	VCC	135	AUX1IN0
8	EB_A7	40	N/C	72	SB_IRQ1	104	SB_AD16	136	MEMCTL_IRQ
9	EB_A6	41	GND	73	SB_RD	105	SB_AD15	137	MSI_CNTRL_IRQ
10	EB_A5	42	SER_RD	74	SB_AS	106	SB_AD14	138	AUX1IN1
11	EB_A4	43	SER_WR	75	SB_SEC_SEL	107	SB_AD13	139	VID_IRQ
12	EB_A3	44	KB_MS_RD	76	SB_ACK32	108	SB_AD12	140	VCC
13	EB_A2	45	KB_MS_WR	77	SB_ACK8	109	SB_AD11	141	GND
14	EB_A1	46	AUD_RD	78	SB_ERR	110	GND	142	MEM_RST
15	EB_A0	47	AUD_WR	79	GND	111	VCC	143	SEC_MODE
16	EB_A16	48	RTC_OE	80	N/C	112	SB_AD10	144	JTAGCLK
17	M1_IRL1	49	RTC_WR	81	VCC	113	SB_AD9	145	JTAGDO
18	VCC	50	FLOPPY_WR	82	SB_AD31	114	SB_AD8	146	JTAGDI
19	M1_IRL0	51	EPROM_OE0	83	SB_AD30	115	SB_AD7	147	JTAGTMS
20	GND	52	FLOPPY_RD	84	SB_AD29	116	SB_AD6	148	AUX2OUT1
21	M2_IRL3	53	SER_IRQ	85	SB_AD28	117	SB_AD5	149	FLOP_IRQ
22	EB_A15	54	KB_MS_IRQ	86	SB_AD27	118	SB_AD4	150	AUX2OUT0
23	EB_A14	55	AUD_IRQ	87	SB_AD26	119	N/C	151	AUX2IN1
24	EB_A13	56	SCSI_IRQ	88	SB_AD25	120	N/C	152	AUX2IN0
25	EB_A12	57	ET_IRQ	89	SB_AD24	121	GND	153	M2_IRL0
26	EB_A11	58	MOD_IRQ	90	GND	122	SB_AD3	154	M3_IRL3
27	EB_A10	59	AERR	91	VCC	123	SB_AD2	155	M3_IRL2
28	EB_A9	60	GND	92	SB_AD23	124	SB_AD1	156	M3_IRL1
29	GND	61	VCC	93	SB_AD22	125	SB_AD0	157	M3_IRL0
30	VCC	62	TMR_CLK	94	SB_AD21	126	SB_SIZE2	158	GND
31	EB_D7	63	GEN_RD	95	SB_AD20	127	SB_SIZE1	159	VCC
32	EB_D6	64	GEN_SEL	96	SB_AD19	128	SB_SIZE0	160	N/C

Pinout Information



Top View

Dimensions: D, D1, D3, E, E1, E3, 1, 40, 41, 80, 121, 120, 81.

No. of Pins = 40

Index Mark

Side View

Detail W

Dimensions: A, A2, G (Note 3).

Detail X

Dimensions: A1, A, B, C, e (Note 4), L, q, H (Note 4), C (Note).

Dimension		mm
A	Max	4.01
A1	Min	0.25
	Max	0.36
A2	Min	3.17
	Norm	3.42
	Max	3.65
B	Min	0.22
	Max	0.38
C	Min	0.13
	Max	0.23
D	Min	31.60
	Norm	32.00
	Max	32.40
D1	Min	27.90
	Norm	28.00
	Max	28.10
D3	Ref	25.35
e	BSC	0.65
E	Min	31.60
	Norm	32.00
	Max	32.40
E1	Min	27.90
	Norm	28.00
	Max	28.10
E3	Ref	25.35
L	Min	0.65
	Norm	0.80
	Max	0.95
q	Min	0.25
	Max	0.36

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Preliminary
STP2014

SEC
SBus-to-EBus Controller

ORDERING INFORMATION

Part Number	Description
STP2014PQFP	160-Pin Plastic Quad Flat Package (PQFP)

Document Part Number: STP2014