P93U422
HIGH SPEED 256 × 4 CMOS STATIC RAM

T-46-23-08

FEATURES

- Universal 256 × 4 Static RAM
- One part, the 93U422, replaces the following bipolar and CMOS parts:
  - 93422A
  - 93422
  - 93L422A
  - 93L422
- PACE Technology™ for High Performance/Low Power
- Fast Access Time
  - 35 ns (Commercial)
  - 35 ns (Military)
- Standard 400 mil DIP and Chip carrier packages
- CMOS for Low Power
  - 440 mW (Commercial)
  - 495 mW (Military)
- 5V Power Supply ±10% for both commercial and military temperature ranges
- Separate I/O
- Fully static operation with equal access and cycle time
- Resistant to single event upset and latchup due to advanced process and design improvements
- Capable of withstanding greater than 2000V static discharge

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DESCRIPTION

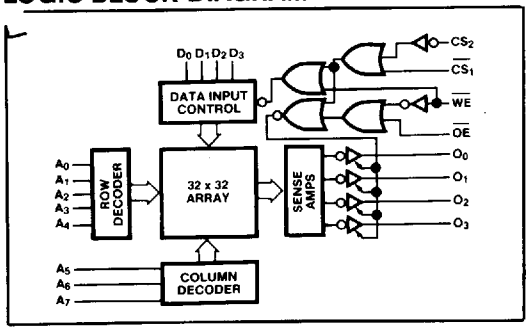
The P93U422 is a universal device designed to replace the entire 93 and 93L 256×4 bit static RAM families. The memory requires no clocks or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL compatible. Operation is from a single 5 Volt supply. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) and an active HIGH chip select two (CS_2) as well as 3-state outputs.

The P93U422 is part of the PACE RAM™ family of static RAMs. These high performance static RAMs are manufactured using PACE Technology™.

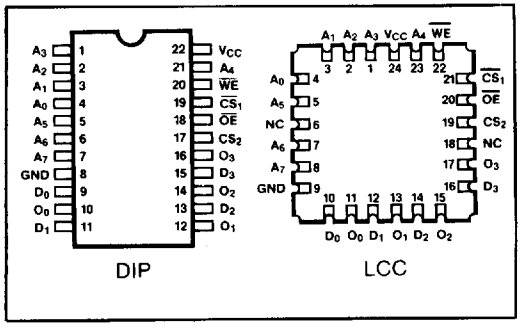
PACE Technology is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths to give 500 picoseconds loaded* internal gate delays. PACE Technology™ includes two level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a class 2 environment volume production facility. The P93U422 is one of a family of PACE RAM™ products offering super fast access times.

*For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature and 5.0V.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



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MAXIMUM RATINGS[1,2]

(Above which the useful life may be impaired.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 22 to Pin 8)	-0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to V_{CC} + 0.5V
DC Input Voltage	-0.5V to V_{CC} + 0.5V

Output Current, Into Outputs (Low)	20mA
DC Input Current	-30 mA to +5.0mA
Static Discharge Voltage (per MIL-STD-883 Method 3015.2)	>2000V
Latchup Current	>200mA

OPERATING RANGE

Range	V_{CC}	Ambient Temperature
Commercial	5V ±10%	0°C to 75°C

Range[6]	V_{CC}	Ambient Temperature
Military	5V ±10%	-55°C to +125°C

DC ELECTRICAL CHARACTERISTICS[6]

Over Operating Range (Commercial and Military)

Parameters	Description	Test Conditions		P93U422 Min.	P93U422 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = -5.2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 8.0 mA			0.45	V
V_{IH}	Input HIGH Level			2.1		V
V_{IL}	Input LOW Level				0.8	V
I_{IL}	Input LOW Current	V_{IN} = 0.40 V			-300	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5 V			40	μA
I_{SC}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = 0.0 V			-70	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max.	T_A = 125°C		70	mA
			T_A = 75°C		70	
			T_A = 0°C		80	
			T_A = -55°C		90	
V_{CL}	Input Clamp Voltage	I_{IN} = -10mA			-1.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V, V_{CC} = Max.			50	μA
		V_{OUT} = 0.5V, V_{CC} = Max.		-50		

CAPACITANCE

Parameters	Description	P93U422 Typ.	Units
C_{IN}	Input Pin Capacitance[4]	5	pF

Parameters	Description	P93U422 Typ.	Units
C_{OUT}	Output Pin Capacitance[4]	7	pF

Notes:

1) These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields, however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.
2) Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3) For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4) Tested on a sample basis.

SWITCHING CHARACTERISTICS

An active LOW write enable ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and the write enable ($\overline{WE}$) are LOW and chip select two (CS_2) is HIGH, the information on data inputs (D_0 through D_3) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch". Reading is performed with chip select one ($\overline{CS_1}$) LOW, chip select two (CS_2) HIGH, write enable ($\overline{WE}$) HIGH and output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the non-inverting outputs (O_0 through O_3). The outputs of the memory go to an inactive high impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

MODE SELECT TABLE

Input					Output	Mode
CS_2	$\overline{CS_1}$	$\overline{WE}$	$\overline{OE}$	D_n	O_n	
L	X	X	X	X	*HIGH Z	Not Select
X	H	X	X	X	*HIGH Z	Not Select
H	L	X	H	X	*HIGH Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	*HIGH Z	Write "0"
H	L	L	X	H	*HIGH Z	Write "1"

Notes:
H = HIGH L = LOW X = Don't Care
*HIGH Z implies outputs are disabled or off. This condition is defined as high impedance state for the P93U422.

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SWITCHING CHARACTERISTICS (5,6)

Over Operating Range (Commercial and Military)

Parameters	Description	P93U422		Units
		Min.	Max.	
$t_{PLH(A)}$[7] $t_{PHL(A)}$[7]	Delay from Address to Output (Address Access Time) (See Fig. 2)		35	ns
t_{PZH} ($\overline{CS_1}$, CS_2)[8] t_{PZL} (CS_1, CS_2)[8]	Delay from Chip Select to Active Output and Correct Data (See Fig. 2)		25	ns
t_{PZH} ($\overline{WE}$)[8] t_{PZL} ($\overline{WE}$)[8]	Delay from Write Enable to Active Output and Correct Data (Write Recovery)(See Fig. 1)		25	ns
t_{PZH}($\overline{OE}$)[8] t_{PZL}(OE)[8]	Delay from Output Enable to Active Output and Correct Data (See Fig. 2)		25	ns
t_s(A)	Setup Time Address (Prior to Initiation of Write)(See Fig. 1)	5		ns
t_h(A)	Hold Time Address (After Termination of Write)(See Fig. 1)	5		ns
t_s(DI)	Setup Time Data Input (Prior to Initiation of Write)(See Fig. 1)	5		ns
t_h(DI)	Hold Time Data Input (After Termination of Write)(See Fig. 1)	5		ns
t_s ($\overline{CS_1}$, CS_2)	Setup Time Chip Select (Prior to Initiation of Write)(See Fig. 1)	5		ns
t_h ($\overline{CS_1}$, CS_2)	Hold Time Chip Select (After Termination of Write)(See Fig. 1)	5		ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width (to Insure Write)(See Fig. 1)	20		ns
t_{PHZ} ($\overline{CS_1}$, CS_2)[8] t_{PLZ} (CS_1, CS_2)[8]	Delay from Chip Select to Inactive Output (HIGH Z)(See Fig. 2)		30	ns
t_{PHZ} ($\overline{WE}$)[8] t_{PLZ} ($\overline{WE}$)[8]	Delay from Write Enable to Inactive Output (HIGH Z)(See Fig. 1)		30	ns
t_{PHZ} ($\overline{OE}$)[8] t_{PLZ} ($\overline{OE}$)[8]	Delay from Output Enable to Inactive Output (HIGH Z)(See Fig. 2)		30	ns

Notes:
5) Test conditions assume signal transition times of 10 ns or less
6) Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
7) t_{PLH}(A) and t_{PHL}(A) are tested with S_1 closed and C_L = 15 pF with both input and output timing referenced to 1.5V.
8) t_{PZH}($\overline{WE}$), t_{PZH}($\overline{CS_1}$, CS_2) and t_{PZH}($\overline{OE}$) are measured with S_1 open, C_L = 15 pF and with both the input and output timing referenced to 1.5V. t_{PZL}($\overline{WE}$), t_{PZL}($\overline{CS_1}$, CS_2) and t_{PZL}($\overline{OE}$) are measured with S_1 closed, C_L = 15 pF and with both the input and output timing referenced to 1.5V.
t_{PHZ}($\overline{WE}$), t_{PHZ}($\overline{CS_1}$, CS_2) and t_{PHZ}($\overline{OE}$) are measured with S_1 open, C_L < 5 pF and are measured between the 1.5 V level on the input to the V_{OH} - 500mV level on the output.
t_{PLZ}($\overline{WE}$), t_{PLZ}($\overline{CS_1}$, CS_2) and t_{PLZ}($\overline{OE}$) are measured with S_1 closed, C_L < 5 pF and are measured between the 1.5V level on the input to the V_{OL} +500mV level on the output.

SWITCHING TEST

Test Circuits (7,8)

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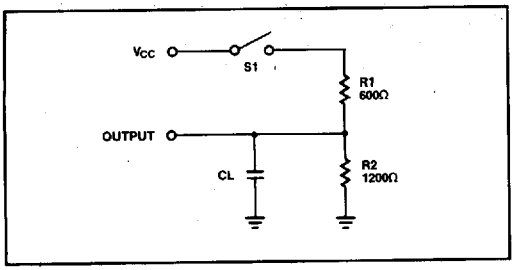

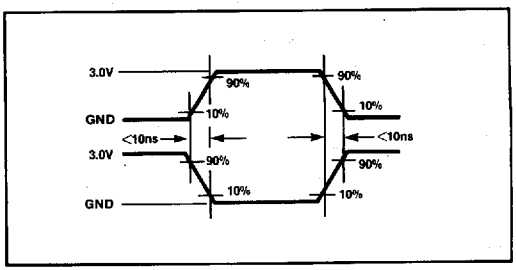

KEY TO DIAGRAM

Waveform	Inputs	Outputs
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H

Waveform	Inputs	Outputs
	Don't care; any change permitted	Changing; state unknown
	Does not apply	Center line is high impedance "off" state

SWITCHING WAVEFORMS

Write Mode (with $\overline{OE}$ = Low)

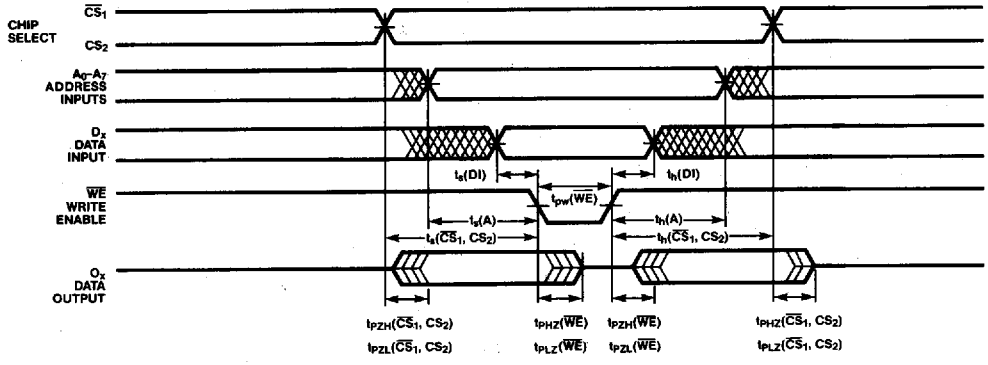

Figure 1.

Read Mode

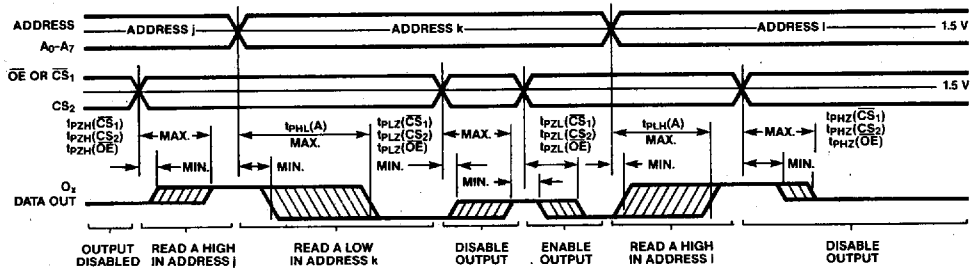

Figure 2.

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SELECTION GUIDE
(For higher performance and lower power refer to the P4C422 data sheet)

Maximum Access Time (ns)	Commercial	35	Maximum Operating Current (mA)	Commercial	80
	Military	35		Military	90

ORDERING INFORMATION

Ordering Code	Package Type	Operating Range
P4C422-35PC or P93U422-35PC	Plastic DIP	Commercial
P4C422-35DC or P93U422-35DC	Ceramic DIP	Commercial
P4C422-35LC or P93U422-35LC	LCC	Commercial
P4C422-35DMB or P93U422-35DMB	Ceramic DIP	Military
P4C422-35LMB or P93U422-35LMB	LCC	Military

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