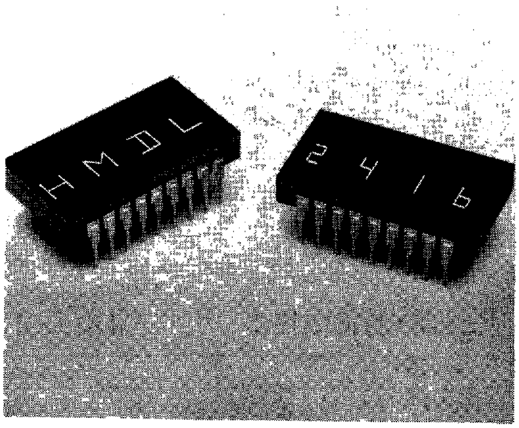
HEWLETT PACKARD

FOUR CHARACTER 3.8mm (0.15 inch) HERMETIC, SMART ALPHANUMERIC DISPLAY

HMDL-2416
HMDL-2416TXV
HMDL-2416TXVB

Features

- **WIDE OPERATING TEMPERATURE RANGE -55° C to +100° C**
- **TRUE HERMETIC PACKAGE**
- **TXVB VERSION CONFORMS TO MIL-D-87157 QUALITY LEVEL A TEST TABLES**
- **CMOS IC FOR LOW POWER CONSUMPTION**
- **SMART ALPHANUMERIC DISPLAY** **Built-in RAM, ASCII Decoder, and LED Drive Circuitry**
- **VERY FAST ACCESS TIME, 160 ns**
- **EXCELLENT ESD PROTECTION** **Built-in Protective Diodes**
- **FULL TTL COMPATIBILITY OVER OPERATING TEMPERATURE RANGE**
- **END-STACKABLE**
- **WIDE VIEWING ANGLE**
- **WAVE SOLDERABLE**



Description

The HMDL-2416 is a smart 3.8 mm (0.15") four character, sixteen segment red GaAsP display. It is contained in a hermetic 18 pin dual-in-line, glass sealed ceramic package. The on-board CMOS IC contains memory, ASCII decoder, multiplexing circuitry, and drivers It has a wide operating temperature range, and is fully TTL compatible, wave solderable, and highly reliable This display is ideally suited for military and high reliability industrial applications where a rugged, reliable, easy-to-use alphanumeric display is required.

Typical Applications

- **MILITARY EQUIPMENT**
- **AVIONICS**
- **HIGH RELIABILITY INDUSTRIAL EQUIPMENT**

Absolute Maximum Ratings

Supply Voltage, V_{CC} to Ground .... -0.5 V to 7.0 V

Input Voltage, Any Pin to Ground .... -0.5 V to V_{CC} + .5 V

Free Air Operating Temperature Range, T_A .... -55° to +100°C

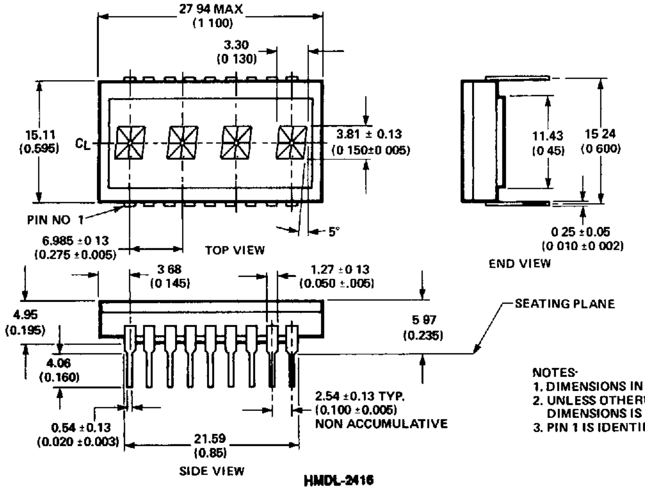
Storage Temperature, T_S .... -65° to +125°C

Maximum Solder Temperature, 1.59 mm (0.063 in.) below Seating Plane, t < 5 sec. .... 260° C

ESD WARNING: The HMDL-2416 is implemented in a standard CMOS process with diode protection of all inputs. The ESD susceptibility of this IC device is Class A of MIL-STD-883 or Class 2 of DOD-STD-1686 and DOD-HDBK-263. Standard precautions for handling CMOS devices should be observed.

HERMETIC DISPLAYS

Package Dimensions



NOTES:
1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±0.38 mm (0.015").
3. PIN 1 IS IDENTIFIED BY INK DOT ON BOTTOM OF PACKAGE

HMDL-2416

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	$\overline{CE}_1$ CHIP ENABLE	10	GND
2	$\overline{CE}_2$ CHIP ENABLE	11	D_0 DATA INPUT
3	$\overline{CLR}$ CLEAR	12	D_1 DATA INPUT
4	CUE CURSOR ENABLE	13	D_2 DATA INPUT
5	$\overline{CU}$ CURSOR SELECT	14	D_3 DATA INPUT
6	$\overline{WR}$ WRITE	15	D_6 DATA INPUT
7	A_1 DIGIT SELECT	16	D_5 DATA INPUT
8	A_0 DIGIT SELECT	17	D_4 DATA INPUT
9	V_{CC}	18	$\overline{BL}$ DISPLAY BLANK

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage High	V_{IH}	2.0			V
Input Voltage Low	V_{IL}			0.8	V

DC Electrical Characteristics Over Operating Temperature Range

TYPICAL VALUES

Parameter	Symbol	Units	-55°C	25°C	+100°C	Test Condition
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	120	85	70	V_{CC} = 5.0 V
I_{CC} Cursor[2,3,4]	$I_{CC}(\overline{CU})$	mA	170	125	105	V_{CC} = 5.0 V
I_{CC} Blank	$I_{CC}(\overline{BL})$	mA	1.8	1.5	1.3	V_{CC} = 5.0 V $\overline{BL}$ = 0.8 V
Input Current, Max.	I_{IL}	µA	22	17	12	V_{CC} = 5.0 V V_{IN} = 0.8 V
Thermal Resistance Junction to Case	$R\Theta_{J\text{-}C}$	°C/W/ Device		20		

GUARANTEED VALUES

Parameter	Symbol	Units	25°C V_{CC} = 5.0 V	Maximum Over Operating Temperature Range V_{CC} = 5.5 V
I_{CC} 4 digits on (10 seg/digit)[1,2]	I_{CC}	mA	115	167
I_{CC} Cursor[2,3,4]	$I_{CC}(\overline{CU})$	mA	165	225
I_{CC} Blank	$I_{CC}(\overline{BL})$	mA	3.5	8.0
Input Current, Max.	I_{IL}	µA	30	40
Power Dissipation[5]	P_D	mW	575	918
Leak Rate	LR	cc/sec		5×10^{-8}

Notes:
1. "%" illuminated in all four characters
2. Measured at five seconds
3. Cursor character is sixteen segments and DP on
4. Cursor operates continuously over operating temperature range
5. Power dissipation = $V_{CC} \cdot I_{CC}$ (10 seg.)

AC Timing Characteristics Over Temperature at V_{CC} = 4.5 V[1]

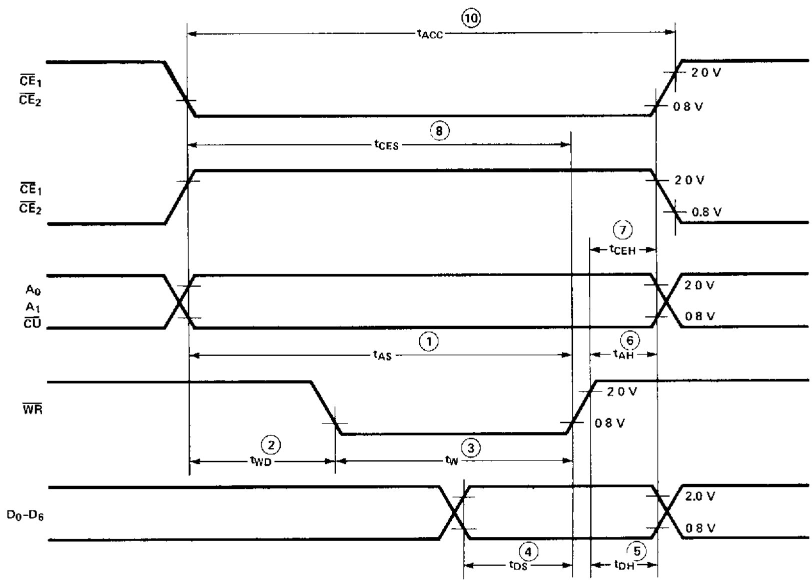
Symbol	Description	-20° C t_{MIN}	25° C t_{MIN}	70° C t_{MIN}	Units
1 t_{AS}	Address Setup Time	90	115	150	ns
2 t_{WD}	Write Delay Time	10	15	20	ns
3 t_W	Write Time	80	100	130	ns
4 t_{DS}	Data Setup Time	40	60	80	ns
5 t_{DH}	Data Hold Time	40	45	50	ns
6 t_{AH}	Address Hold Time	40	45	50	ns
7 t_{CEH}	Chip Enable Hold Time	40	45	50	ns
8 t_{CES}	Chip Enable Setup Time	90	115	150	ns
9 t_{CLR}	Clear Time	2.4	3.5	4.0	ms
10 t_{ACC}	Access Time	130	160	200	ns
	Refresh Rate	420-790	310-630	270-550	Hz

Note: 1 These parameters are guaranteed by design but are not tested

Optical Characteristics

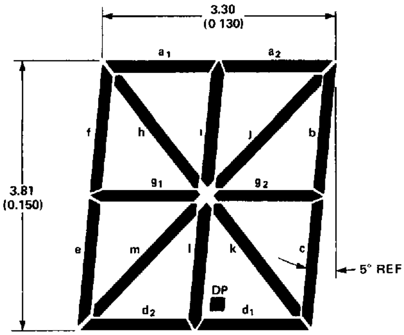
Parameter	Symbol	Test Condition	Min.	Typ.	Units
Peak Luminous Intensity per digit, 8 segments on (character average)	I_V Peak	V_{CC} = 5.0 V "✱" illuminated in all 4 digits (25° C)	0.2	0.6	mcd
Peak Wavelength	λpeak			655	nm
Dominant Wavelength	λ_d			640	nm
Off Axis Viewing Angle				±65	degrees
Digit Size				3.81	mm

Timing Diagram

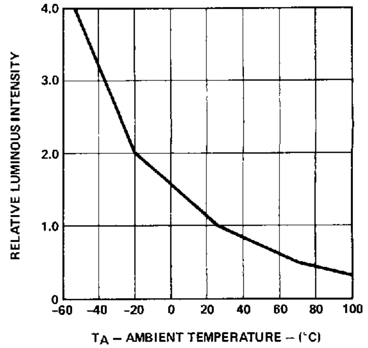


HERMETIC DISPLAYS

Character Font Description



Relative Luminous Intensity vs. Temperature



Electrical Description

Display Internal Block Diagram

Figure 1 shows the internal block diagram for the HMDL-2416 display. The CMOS IC consists of a four-word ASCII memory, a four-word cursor memory, a 64-word character generator, 17 segment drivers, four digit drivers, and the scanning circuitry necessary to multiplex the four monolithic LED characters. In normal operation, the divide-by-four counter sequentially accesses each of the four RAM locations and simultaneously enables the appropriate display digit driver. The output of the RAM is decoded by the character generator which, in turn, enables the appropriate display segment drivers. For each display location, the cursor enable (CUE) selects whether the data from the ASCII RAM (CUE = 0) or the stored cursor (CUE = 1) is to be displayed. The cursor character is denoted by all sixteen segments and the DP ON. Seven-bit ASCII data is stored in RAM. Since the display utilizes a 64-character decoder, half of the possible 128 input combinations are invalid. For each display location where $D_5 = \overline{D_6}$ in the ASCII RAM, the display character is blanked. The entire display is blanked when $\overline{BL} = 0$.

Data is loaded into the display through the data inputs (D_6- D_0), digit selects (A_1, A_0), chip enables ($\overline{CE}_1$, $\overline{CE}_2$, cursor select ($\overline{CU}$), and write ($\overline{WR}$) The cursor select ($\overline{CU}$) determines whether data is stored in the ASCII RAM ($\overline{CU}$ = 1) or cursor memory ($\overline{CU}$ = 0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 1$, the information on the data inputs is stored in the ASCII RAM at the location specified by the digit selects (A_1, A_0). When $\overline{CE}_1 = \overline{CE}_2 = \overline{WR} = 0$ and $\overline{CU} = 0$, the information on the data input, D_0, is stored in the cursor at the location specified by the digit selects (A_1, A_0) If $D_0 = 1$, a cursor character is stored in the cursor memory If $D_0 = 0$, a previously stored cursor character will be removed from the cursor memory.

If the clear input ($\overline{CLR}$) equals zero for one internal display cycle (4 ms minimum), the data in the ASCII RAM will be rewritten with zeroes and the display will be blanked. Note that the blanking input ($\overline{BL}$) must be equal to logical one during this time.

Data Entry

Figure 2 shows a truth table for the HMDL-2416 display. Setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its high state will enable data loading. The desired data inputs (D_6-D_0) and address inputs (A_1, A_0) as well as the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored into the display Valid ASCII data codes are shown in Figure 3 The display accepts standard seven-bit ASCII data Note that $D_6 = \overline{D_5}$ for the codes shown in Figure 2 If $D_6 = D_5$ during the write cycle, then a blank will be stored in the display Data can be loaded into the display in any order Note that when $A_1 = A_0 = 0$, data is stored in the furthest right-hand display location.

Cursor Entry

As shown in Figure 2, setting the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) to their low state and the cursor select ($\overline{CU}$) to its low state will enable cursor loading. The cursor character is indicated by the display symbol having all 16 segments and the DP ON The least significant data input (D_0), the digit selects (A_1, A_0), the chip enables ($\overline{CE}_1$, $\overline{CE}_2$), and the cursor select ($\overline{CU}$) must be held stable during the write cycle to ensure that the correct data is stored in the display If D_0 is in a low state during the write cycle, then a cursor character will be removed at the indicated location If D_0 is in a high state during the write cycle, then a cursor character will be stored at the indicated location The presence or absence of a cursor character does not affect the ASCII data stored at that location Again, when $A_1 = A_0 = 0$, the cursor character is stored in the furthest right-hand display location.

All stored cursor characters are displayed if the cursor enable (CUE) is high. Similarly, the stored ASCII data words are displayed, regardless of the cursor characters, if the cursor enable (CUE) is low The cursor enable (CUE) has no effect on the storage or removal of the cursor characters within the display. A flashing cursor is displayed by pulsing the cursor enable (CUE). For applications not requiring a cursor, the cursor enable (CUE) can be connected to ground and the cursor select ($\overline{CU}$) can be connected to V_{CC} This inhibits the cursor function and allows only ASCII data to be loaded into the display

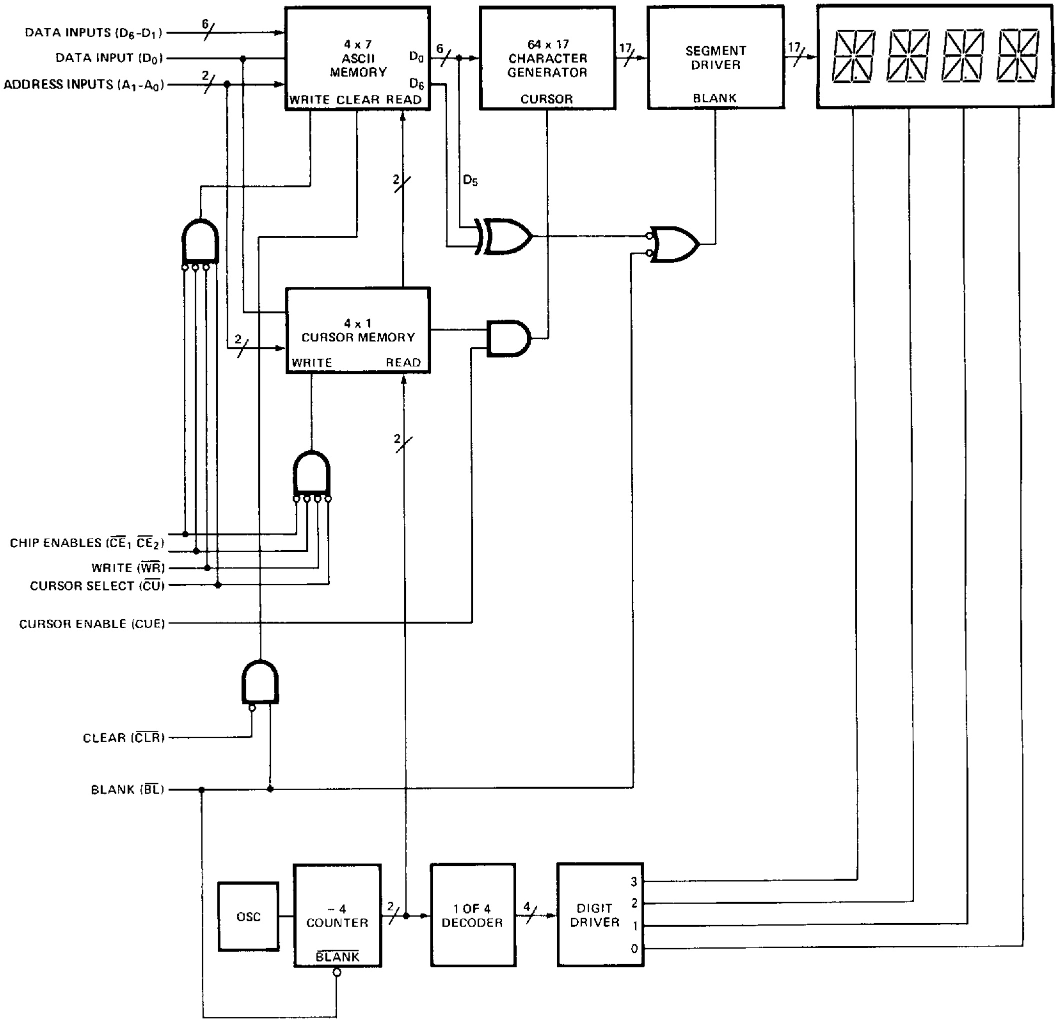


Figure 1. HMDL-2416 Internal Block Diagram

Display Clear

As shown in Figure 2, the ASCII data stored in the display will be cleared if the clear ($\overline{CLR}$) is held low and the blanking input ($\overline{BL}$) is held high for 4 ms minimum. The cursor memory is not affected by the clear ($\overline{CLR}$) input. Cursor characters can be stored or removed even while the clear ($\overline{CLR}$) is low. Note that the display will be cleared regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$). However, to ensure that all four display characters are cleared, $\overline{CLR}$ should be held low for 4 ms following the last write cycle

Display Blank

As shown in Figure 2, the display will be blanked if the blanking input ($\overline{BL}$) is held low Note that the display will be blanked regardless of the state of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) or write ($\overline{WR}$) inputs. The ASCII data stored in the display and the cursor memory are not affected by the blanking input. ASCII data and cursor data can be stored even while the blanking input ($\overline{BL}$) is low. Note that while the blanking input ($\overline{BL}$) is low, the clear ($\overline{CLR}$) function is inhibited. A flashing display can be obtained by applying a low frequency square wave to the blanking input ($\overline{BL}$). Because the blanking input ($\overline{BL}$) also resets the internal display multiplex counter, the frequency applied to the blanking input ($\overline{BL}$) should be much slower than the display multiplex rate. Finally, dimming of the display through the blanking input ($\overline{BL}$) is not recommended.

For further application information please consult Application Note 1026.

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	A_1	A_0	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DIG_3	DIG_2	DIG_1	DIG_0
Write	L	X	X	H	L	L	L	L	L	a	a	a	a	a	a	a	NC	NC	NC	A
Data				—OR—				L	H	b	b	b	b	b	b	b	NC	NC	B	NC
Memory	X	H	X	H	L	L	L	H	L	c	c	c	c	c	c	c	NC	C	NC	NC
								H	H	d	d	d	d	d	d	d	D	NC	NC	NC
Disable	X	X	X	H	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Data			
Data	X	X	X	H	X	H	X													
Memory	X	X	X	H	H	X	X													
Write																				
Write	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	H	NC	NC	NC	⊠
Cursor								L	H	X	X	X	X	X	X	H	NC	NC	⊠	NC
								H	L	X	X	X	X	X	X	H	NC	⊠	NC	NC
								H	H	X	X	X	X	X	X	H	⊠	NC	NC	NC
Clear	X	X	X	L	L	L	L	L	L	X	X	X	X	X	X	L	NC	NC	NC	[ ]
Cursor								L	H	X	X	X	X	X	X	L	NC	NC	[ ]	NC
								H	L	X	X	X	X	X	X	L	NC	[ ]	NC	NC
								H	H	X	X	X	X	X	X	L	[ ]	NC	NC	NC
Disable	X	X	X	L	X	X	H	X	X	X	X	X	X	X	X	X	Previously Written Cursor			
Cursor	X	X	X	L	X	H	X													
Memory	X	X	X	L	H	X	X													

L = LOGIC LOW INPUT
H = LOGIC HIGH INPUT
X = DON'T CARE
"a" = ASCII CODE CORRESPONDING TO SYMBOL "A"
NC = NO CHANGE
⊠ = CURSOR CHARACTER (ALL SEGMENTS ON)

Figure 2a. Cursor/Data Memory Write Truth Table

Function	$\overline{BL}$	$\overline{CLR}$	CUE	$\overline{CU}$	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WR}$	DIG_3	DIG_2	DIG_1	DIG_0	
CUE	H	H	L	X	X	X	X	A	B	C	D	Display previously written data
	H	H	H	X	X	X	X	⊠	⊠	⊠	⊠	Display previously written cursor
Clear	H	L	X	X	X	X	X*	[ ]	[ ]	[ ]	[ ]	Clear data memory, cursor memory unchanged
	*NOTE: CLR should be held low for 4 ms following the last WRITE cycle to ensure all data is cleared.											
Blanking	L	X	X	X	X	X	X	[ ]	[ ]	[ ]	[ ]	Blank display, data and cursor memories unchanged.

Figure 2b. Displayed Data Truth Table

BITS		D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
D6 D5 D4		HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 1 0		2	(space)	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
0 1 1		3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
1 0 0		4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
1 0 1		5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_

Figure 3. HPDL-2416 ASCII Character Set

Mechanical and Electrical Considerations

The HMDL-2416 is an 18 pin dual-in-line package, that can be stacked horizontally and vertically to create arrays of any size. The HMDL-2416 is designed to operate continuously from -55° to +100°C for all possible input conditions including the illuminated cursor in all four character locations The HMDL-2416 is assembled by die attaching and wire bonding the four GaAsP/GaAs monolithic LED chips and the CMOS IC to a 18 lead ceramic-glass dual-in-line package It is designed either to plug into DIP sockets or to solder into PC boards

The inputs of the CMOS IC are protected against static discharge and input current latchup However, for best results standard CMOS handling precautions should be used. Prior to use, the HMDL-2416 should be stored in anti-static tubes or conductive material During assembly, a grounded conductive work area should be used The assembly personnel should use conductive wrist straps. Lab coats made of synthetic materials should be avoided since they are prone to static charge build-up Input current latchup is caused when the CMOS inputs are subjected to a voltage either below ground (V_{IN} < ground) or to a higher voltage than V_{CC} ($V_{IN} > V_{CC}$) and a high current is forced into the input To prevent input current latchup and ESD damage, unused inputs should be connected either to ground or to V_{CC}, voltages should not be applied to the inputs until V_{CC} has been applied to the display, and transient input voltages should be eliminated

Soldering and Post Solder Cleaning Instructions for the HMDL-2416

The HMDL-2416 may be hand soldered or wave soldered with SN63 solder Hand soldering may be safely performed only with an electronically temperature-controlled and securely grounded soldering iron For best results, the iron tip temperature should be set at 315°C (600°F) For wave soldering, a rosin-based RMA flux or a water soluble organic acid (OA) flux can be used The solder wave temperature should be 245°C ±5°C (473°F ±9°F), and the dwell in the wave should be set at 1 1/2 to 3 seconds for optimum soldering

Post solder cleaning may be accomplished using water or Freon/alcohol mixtures formulated for vapor cleaning processing or Freon/alcohol mixtures formulated for room temperature cleaning Freon/alcohol vapor cleaning processing for up to 2 minutes in vapors at boiling is permissible. Suggested solvents include Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15, Genesolv DES, and water.

For further information on soldering, refer to Application Note 1027, "Soldering LED Components".

Optical Considerations/ Contrast Enhancement

Each HMDL-2416 display is tested for luminous intensity and marked with an intensity category on the back of the display package. To ensure intensity matching for multiple package applications, all displays for a given panel should have the same category.

The HMDL-2416 display is designed to provide maximum contrast when placed behind an appropriate contrast enhancement filter Some suggested filters are Panelgraphic Dark Red 63, SGL Homalite H100-1650, Rohm and Haas 2423, Chequers Engraving 118, and 3M R6510 For further information on contrast enhancement, see Hewlett-Packard Application Note 1015

High Reliability Testing

Two standard high reliability testing programs are available The TXVB program is in conformance with MIL-D-87157 level A Test Tables The TXVB product is tested to Tables I, II, IIIa, and IVa. The TXV program is an HP modification to the full conformance program and offers the 100% screening of Quality Level A, Table I, and Group A, Table II.

Part Marking System

Standard Product	With Table I and II	With Tables I, II, IIIa, IVa
HMDL-2416	HMDL-2416TXV	HMDL-2416TXVB

100% Screening

Table I. Quality Level A of MIL-D-87157

Test Screen	MIL-STD-750 Method	Conditions
1 Precap Visual	2072	Interpreted by HP Procedure 5956-7235-52
2. High Temperature Storage	1032	$T_A = 125°C$, Time = 24 hours
3. Temperature Cycling	1051	Condition B, 10 cycles, 15 min. dwell
4. Constant Acceleration	2006	5,000 G's at Y_1 orientation
5. Fine Leak	1071	Condition H
6. Gross Leak	1071	Condition C or K
7. Interim Electrical/Optical Tests[2]	—	I_{CC}, I_V @ $V_{CC} = 5.0$ V $T_A = 25°C$
8. Burn-In[1]	1015	Condition B at $V_{CC} = 5.5$ V $T_A = 100°C$ t = 160 hours
9. Final Electrical Test[2]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$) I_{IL}, I_V @ $V_{CC} = 5.0$ V $T_A = 25°C$
10 Delta Determinations	—	$\Delta I_{CC} = \pm 10\%$ $\Delta I_V = -20\%$ $T_A = 25°C$
11 External Visual[1]	2009	

Notes:
1 MIL-STD-883 Test Method Applies
2 Limits and conditions are per the electrical optical characteristics

Table II. Group A Electrical Tests — MIL-D-87157

Subgroup/Test	Parameters	LTPD
Subgroup 1 DC Electrical Tests at 25°C[1]	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V and visual function @ V_{CC} = 5.0 V	5
Subgroup 2 DC Electrical Tests at High Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = +100°C	7
Subgroup 3 DC Electrical Tests at Low Temperature[1]	Same as Subgroup 1, except delete I_V and visual function, T_A = -55°C	7
Subgroup 4, 5, and 6 not applicable		
Subgroup 7 Optical and Functional Tests at 25°C	Satisfied by Subgroup 1	5
Subgroup 8 External Visual	MIL-STD-883, Method 2009	7

Note:
1. Limits and conditions are per the electrical/optical characteristics

HERMETIC DISPLAYS

Table IIIa. Group B, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1 Resistance to Solvents	1022		4 Devices/ 0 Failures
Internal Visual and Design Verification[1]	2075[6]		1 Device/ 0 Failures
Subgroup 2[2,3] Solderability	2026	T_A = 245°C for 5 seconds	LTPD = 15
Subgroup 3 Thermal Shock (Temp. Cycle)	1051	Condition B1, 15 minute dwell	LTPD = 15
Moisture Resistance[4]	1021		
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Electrical/Optical Endpoints[5]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function, T_A = 25°C	
Subgroup 4 Operating Life Test (340 hrs.)	1027	T_A = 100°C @ V_{CC} = 5.5 V	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	
Subgroup 5 Non-operating (Storage) Life Test (340 hrs.)	1032	T_A = +125°C	LTPD = 10
Electrical/Optical Endpoints[5]	—	Same as Subgroup 3	

Notes:
1. Visual inspection is performed through the display window
2. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used
3. The LTPD applies to the number of leads inspected except in no case shall less than 3 displays be used to provide the number of leads required.
4. Initial conditioning is a 15° inward bend for one cycle
5. Limits and conditions are per the electrical/optical characteristics
6. Equivalent to MIL-STD-883, Method 2014

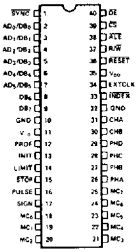
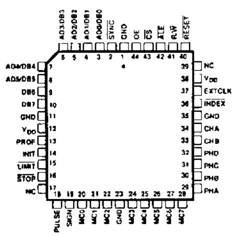
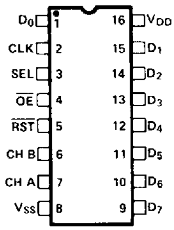
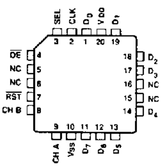
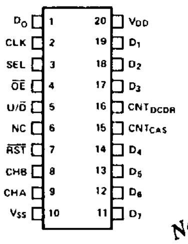
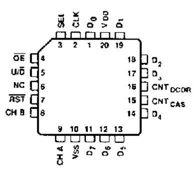
Table IVa. Group C, Class A and B of MIL-D-87157

Subgroup/Test	MIL-STD-750 Method	Conditions	Sample Size
Subgroup 1			
Physical Dimensions	2066		2 Devices/ 0 Failures
Subgroup 2[2]			
Lead Integrity[7, 9]	2004	Condition B2	LTPD = 15
Fine Leak	1071	Condition H	
Gross Leak	1071	Condition C or K	
Subgroup 3			
Shock	2016	1500G, Time = 0 5 ms, 5 blows in each orientation X_1, Y_1, Z_1	LTPD = 15
Vibration, Variable Frequency	2056		
Constant Acceleration	2006	5,000 G's at Y_1 orientation	
External Visual[4]	1010 or 1011		
Electrical/Optical Endpoints[8]	—	I_{CC}%, I_{CC} ($\overline{CU}$), I_{CC} ($\overline{BL}$), I_{IL}, I_V @ V_{CC} = 5.0 V and visual function. T_A = 25°C	
Subgroup 4[1,3]			
Salt Atmosphere	1041		LTPD = 15
External Visual[4]	1010 or 1011		
Subgroup 5			
Bond Strength[5]	2037	Condition A	LTPD = 20 (C = 0)
Subgroup 6			
Operating Life Test[6]	1026	T_A = 100°C @ V_{CC} = 5.5 V	λ = 10
Electrical/Optical Endpoints[8]	—	Same as Subgroup 3	

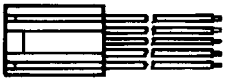
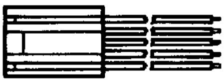
Notes:
1. Whenever electrical/optical tests are not required as endpoints, electrical rejects may be used
2. The LTPD applies to the number of leads inspected except in no case shall less than three displays be used to provide the number of leads required
3. Solderability samples shall not be used.
4. Visual requirements shall be as specified in MIL-STD-883, Methods 1010 or 1011
5. Displays may be selected prior to seal
6. If a given inspection lot undergoing Group B inspection has been selected to satisfy Group C inspection requirements, the 340 hour life tests may be continued on test to 1000 hours in order to satisfy the Group C life test requirements In such cases, either the 340 hour endpoint measurements shall be made a basis for Group B lot acceptance or the 1000 hour endpoint measurement shall be used as the basis for both Group B and Group C acceptance
7. MIL-STD-883 test method applies.
8. Limits and conditions are per the electrical/optical characteristics
9. Initial conditioning is a 15° inward bend for three cycles

T-90-20

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61