TrenchMOS™ transistor Standard level FET

BUK7620-55

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using '**trench**' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

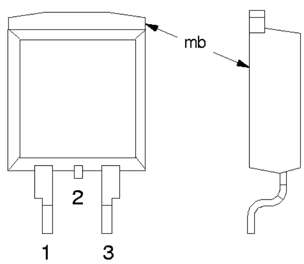
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	116	W
T_j	Junction temperature	175	˚C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	20	mΩ

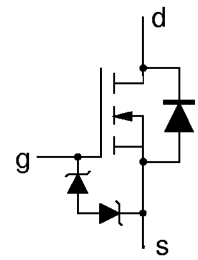
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
I_D	Drain current (DC)	T_{mb} = 25 ˚C	-	52	A
I_D	Drain current (DC)	T_{mb} = 100 ˚C	-	37	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 ˚C	-	208	A
P_{tot}	Total power dissipation	T_{mb} = 25 ˚C	-	116	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	˚C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.29	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

STATIC CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.04	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	15	20	mΩ
		T_j = 175˚C	-	-	42	mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	-	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1350	1800	pF
C_{oss}	Output capacitance		-	330	400	pF
C_{rss}	Feedback capacitance		-	155	215	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	18	26	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	50	75	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	40	50	ns
t_f	Turn-off fall time		-	30	40	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	52	A
I_{DRM}	Pulsed reverse drain current		-	-	208	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 40 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 40 A; -dI_F/dt = 100 A/µs;	-	47	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.15	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 45 A; $V_{DD} \leq$ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	-	110	mJ

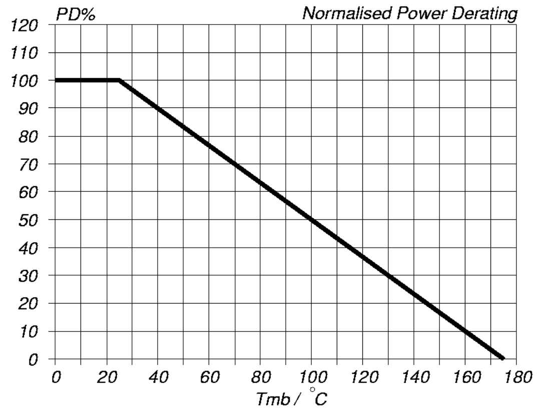


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\ 25\ ˚C} = f(T_{mb})$

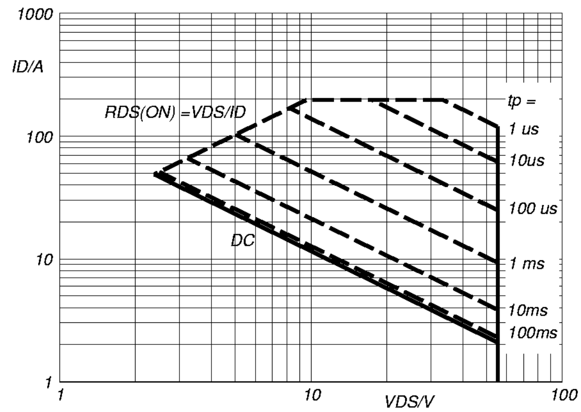


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

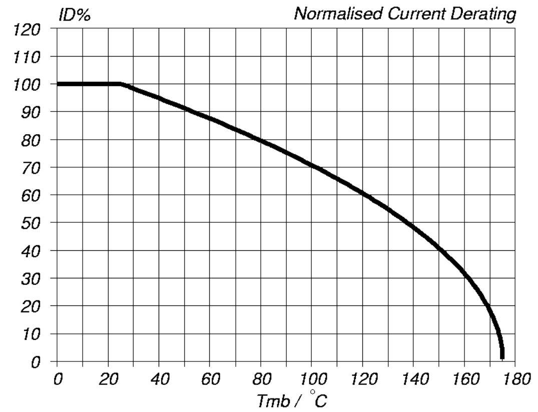


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\ 25\ ˚C} = f(T_{mb})$; conditions: $V_{GS} \geq$ 10 V

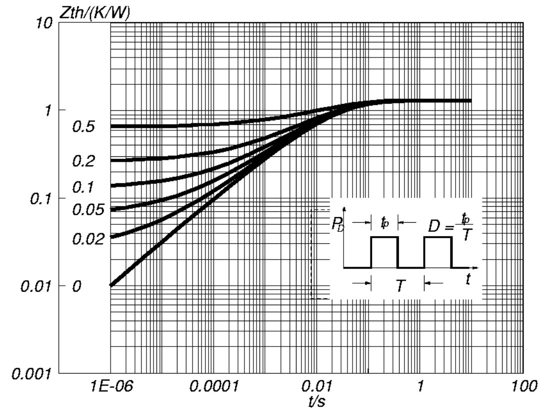


Fig.4. Transient thermal impedance.
$Z_{th\ j\text{-}mb} = f(t)$; parameter $D = t_p/T$

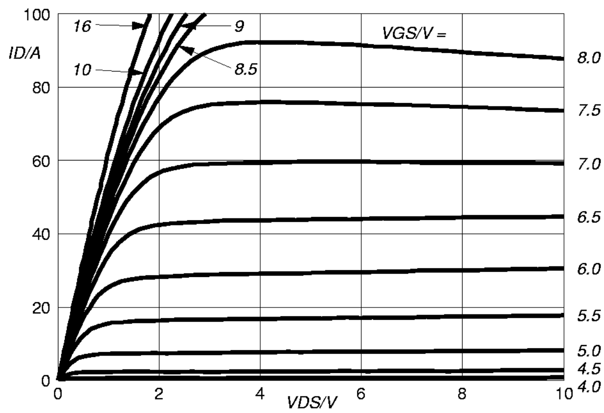


Fig.5. Typical output characteristics, T_j = 25 ˚C.
$I_D = f(V_{DS})$; parameter V_{GS}

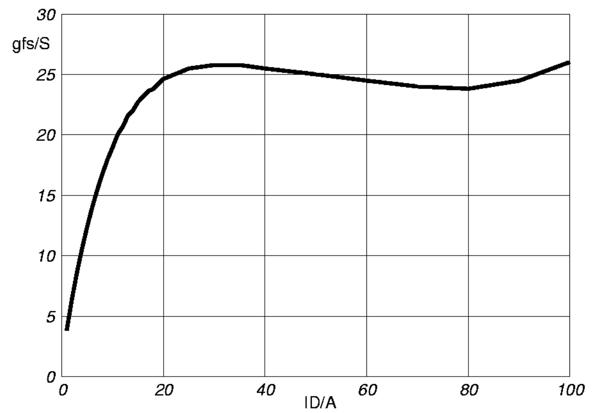


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

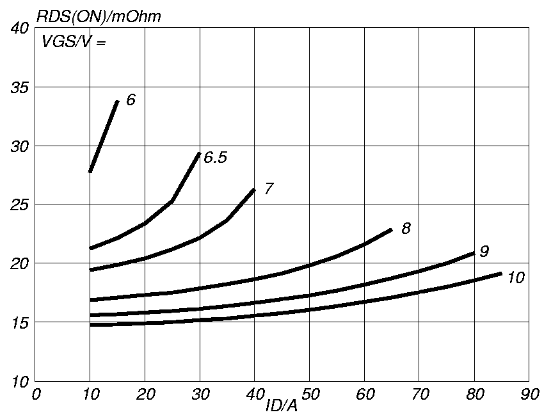


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

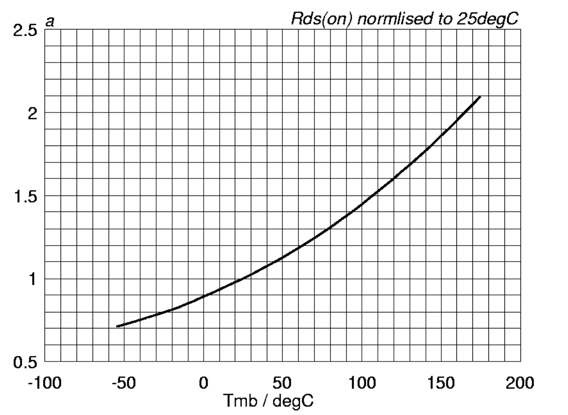


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ˚C} = f(T_j)$; I_D = 25 A; V_{GS} = 10 V

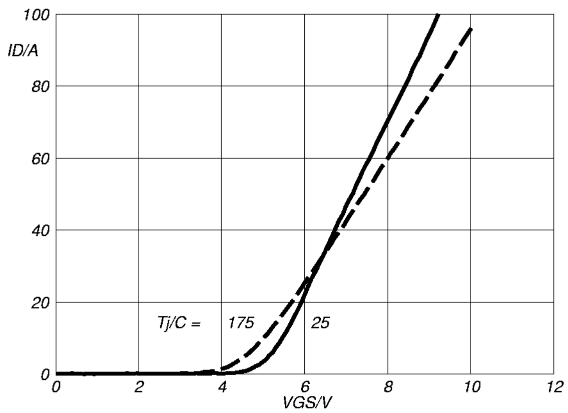


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

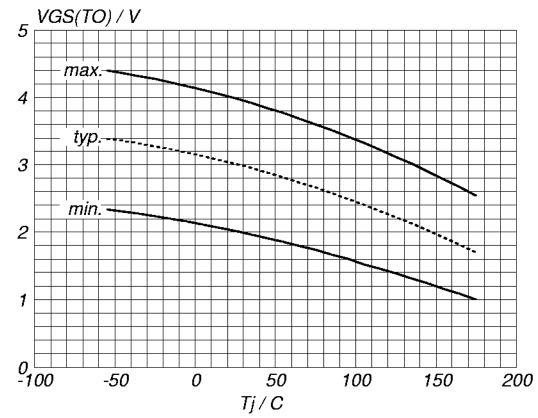


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

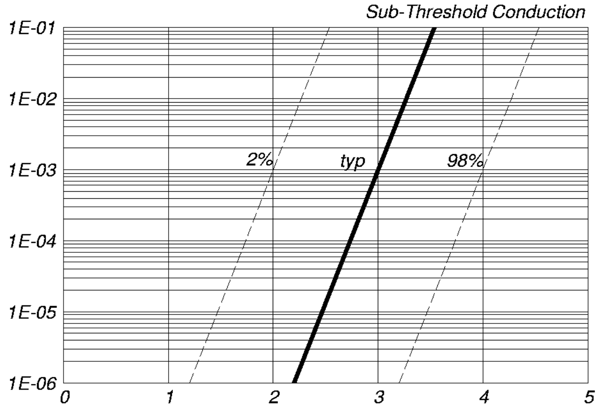


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

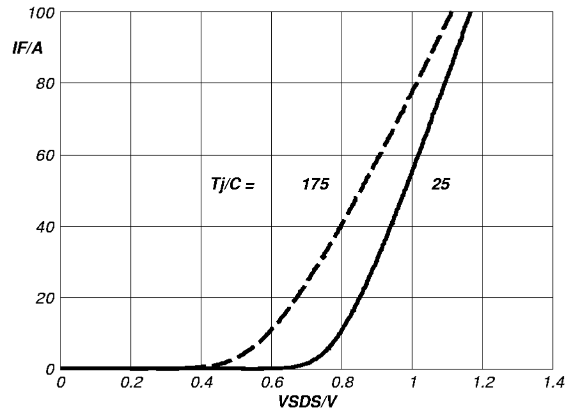


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

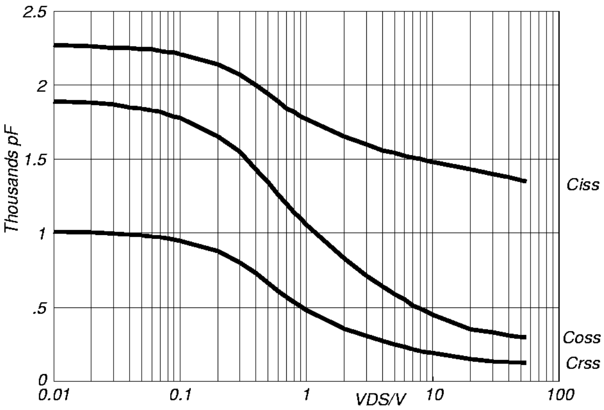


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

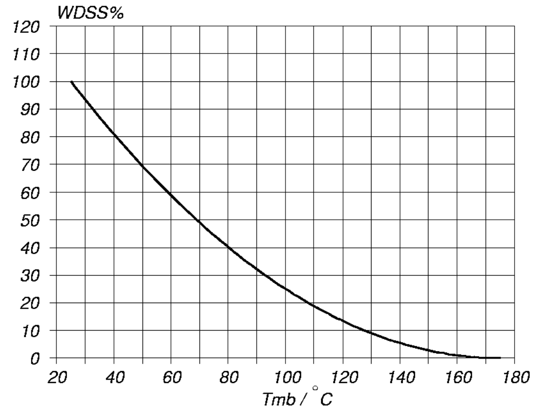


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 49$ A

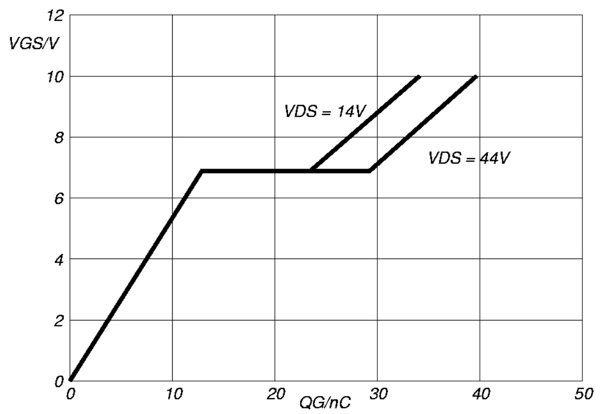


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

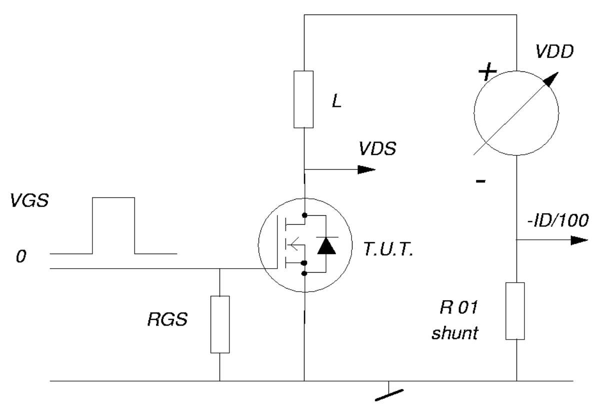


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

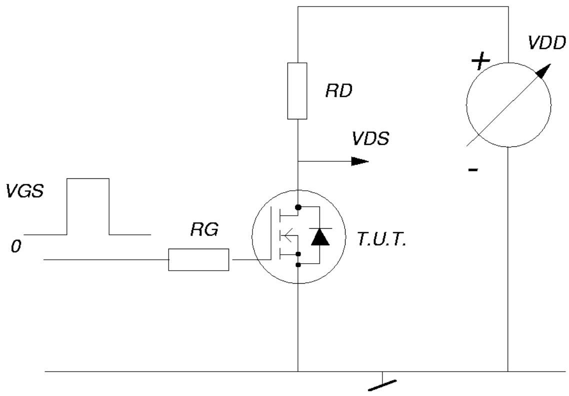


Fig.17. Switching test circuit.

MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

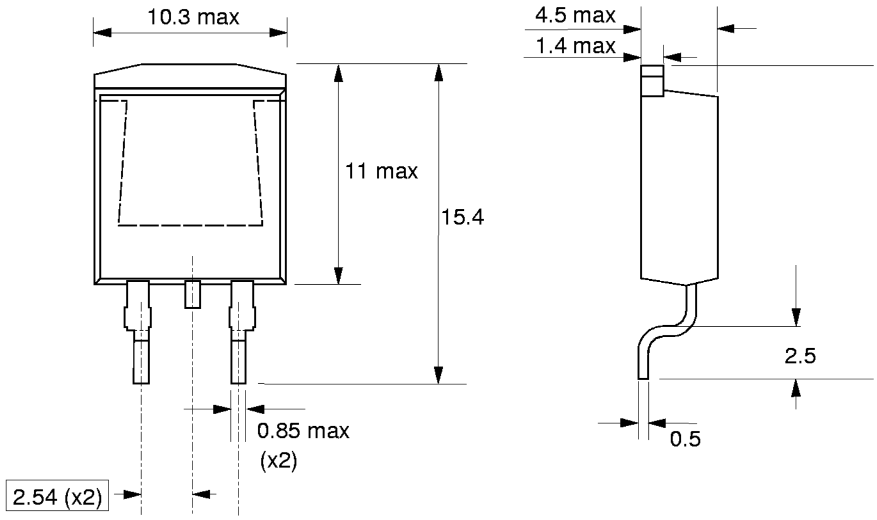


Fig.18. SOT404 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

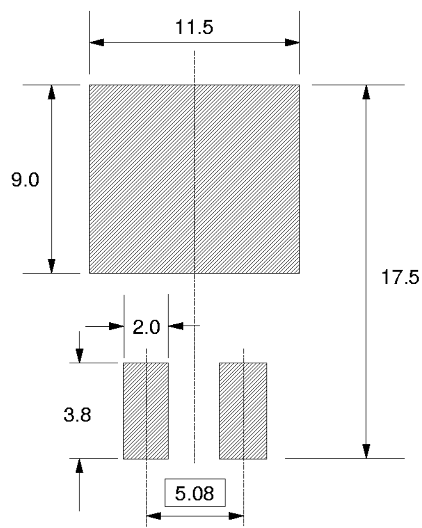


Fig.19. SOT404 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".