8-bit counter

54F269

FEATURES

- Synchronous counting and loading
- Built-in lookahead carry capability
- Count frequency 115MHz typ
- Supply current 95mA typ

DESCRIPTION

The 54F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-Pin Ceramic DIP	54F269/BLA	GDIP3-T24
28-Pin Ceramic LLCC	54F269/B3A	CQCC2-N28

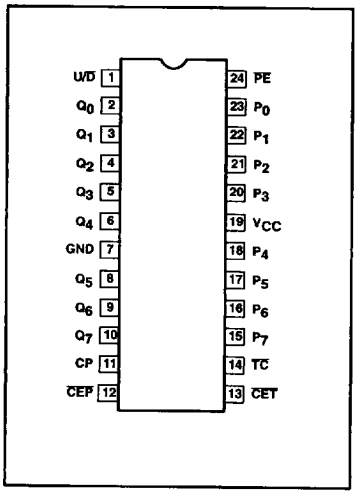
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

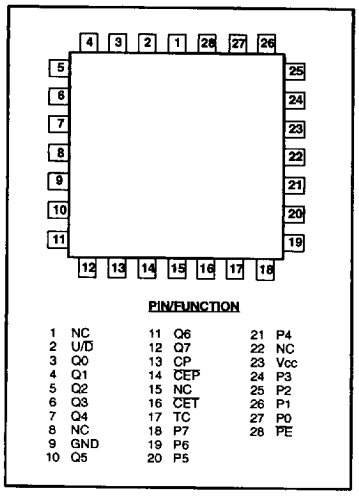
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	HIGH/LOW LOAD VALUE
P0 - P7	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up-Down count control input	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count enable trickle input (active Low)	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1mA/20mA
Q0 - Q7	Flip-flop outputs	50/33	1mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



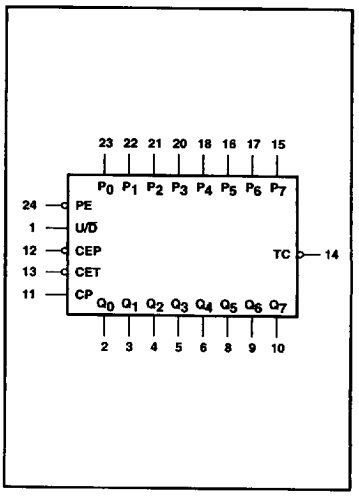
LLCC PIN CONFIGURATION



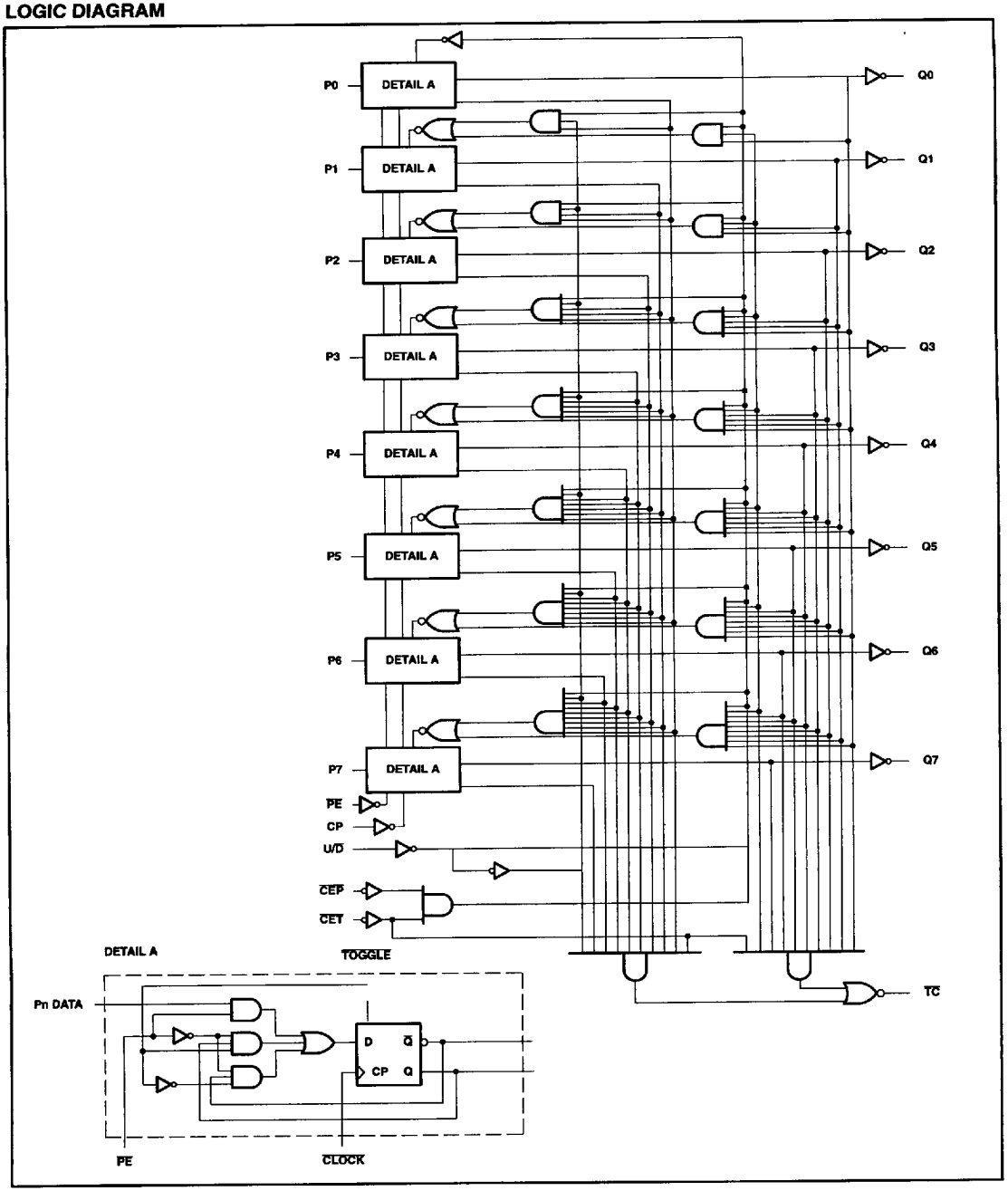
PIN/FUNCTION

1	NC	11	Q6	21	P4
2	U/$\overline{D}$	12	Q7	22	NC
3	Q0	13	CP	23	Vcc
4	Q1	14	$\overline{CEP}$	24	P3
5	Q2	15	NC	25	P2
6	Q3	16	$\overline{CET}$	26	P1
7	Q4	17	TC	27	P0
8	NC	18	P7	28	$\overline{PE}$
9	GND	19	P6		
10	Q5	20	P5		

LOGIC SYMBOL



LOGIC DIAGRAM

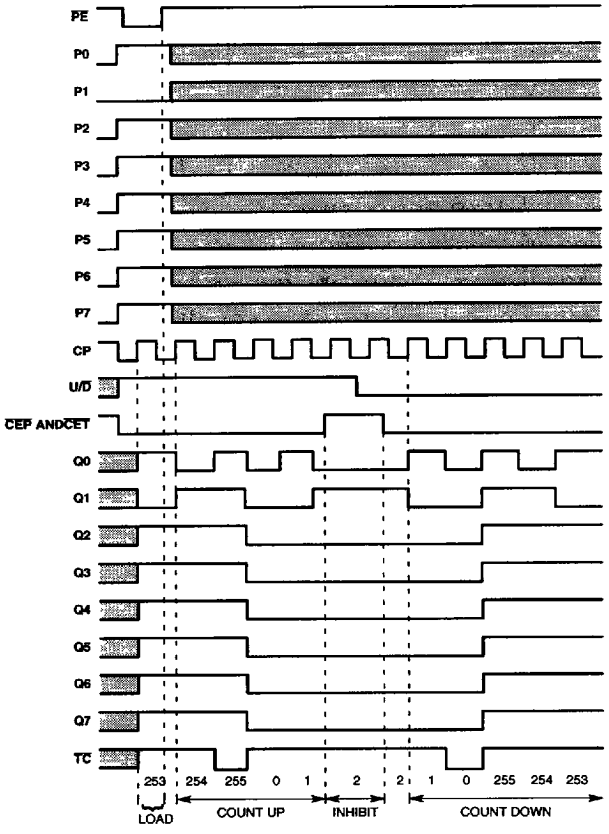


FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{CP}$	U/D	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	p_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(a)
	↑	X	X	X	l	h	H	(a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold	↑	X	h	X	h	X	q_n	(a)
do nothing	↑	X	X	h	h	X	q_n	H

H = High voltage level steady state.
h = High voltage level one set-up time prior to the Low-to-High clock transition.
L = Low voltage level steady state.
l = Low voltage level one set-up time prior to the Low-to-High clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
↑ = Low-to-High clock transition
(a) = The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Qn outputs Low.

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MIN	
V_{CC}	Supply voltage	4.50	5.0	5.5	V
V_{IH}	High-level input voltage[4]	2.0			V
V_{IL}	Low-level input voltage[4]			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = -MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = MAX, V_I = 2.7V			1	20	µA
I_{IL}	Low-level intput current		V_{CC} = MAX, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = MAX		-60	-115	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX	$\overline{PE}$ = $\overline{CET}$ = $\overline{CEP}$ = U/$\overline{D}$ = GND, P_n=4.5V, CP=↑, Outputs Open		93	120	mA
		I_{CCL}		$\overline{PE}$ = $\overline{CET}$ = $\overline{CEP}$ = U/$\overline{D}$ = GND, CP = ↑ Outputs Open		98	125	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			MIN	Typ	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		85[6]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Load)	Waveform 1 $\overline{PE}$ = Low	3.5 4.0	6.0 6.5	9.0 8.5	3.5 4.0	10.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Count)	Waveform 1 $\overline{PE}$ = High	3.5 4.5	5.5 7.5	8.0 10.5	3.5 4.5	9.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 6.0	6.5 8.0	9.5 10.0	4.5 5.5	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.0	6.5 7.0	9.0 10.5	3.5 3.0	10.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	3.5 4.5	7.5 7.0	9.5 9.5	3.5 4.5	10.0 11.0	ns ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup time, High or Low P_n to CP	Waveform 4	1.5 2.0			1.5 2.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low P_n to CP	Waveform 4	1.0 1.0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low $\overline{PE}$ to CP	Waveform 4	5.0 5.0			8.5 9.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	4.5 6.5			8.0 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	1.5 1.0			2.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low U/$\overline{D}$ to CP	Waveform 6	7.0 5.5			12.5 12.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 6	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width[5] High or Low	Waveform 1	3.5 3.5			3.5 4.0		ns ns

NOTES:

1 For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.

2 All typical values are at V_{CC} = 5V, T_A = 25°C.

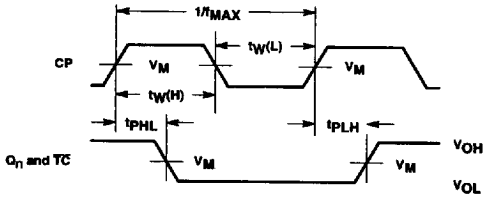
3 Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

4 When testing devices to the functional table specified refer to the 'Recommended Operating Conditions' section of Application Note 202, "Testing and Specifying FAST Logic".

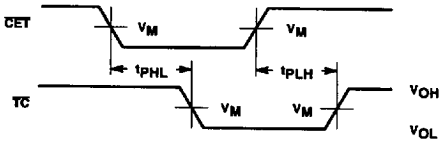
5 T_W tests are guaranteed as specified, but tested to 7.0ns due to tester limitations.

6 This parameter is guaranteed, but not tested.

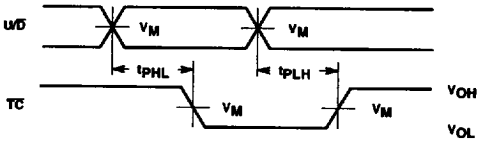
AC WAVEFORMS



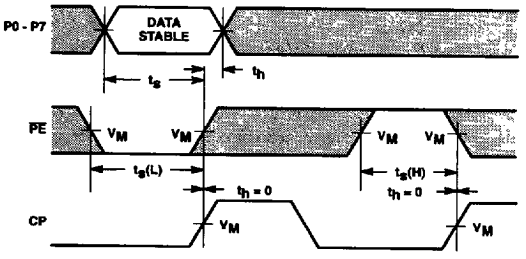
Waveform 1. Clock to Output Delays and Clock Pulse Width



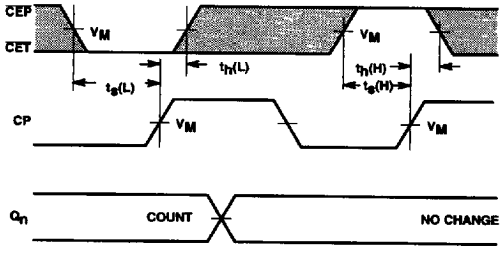
Waveform 2. Propagation Delays CET Input to Terminal Count Output



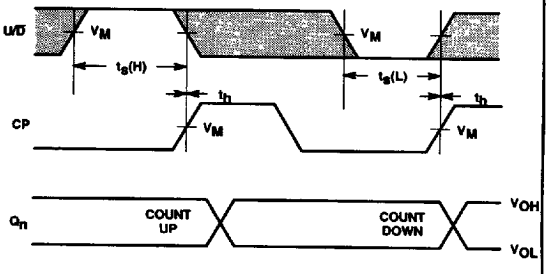
Waveform 3. Propagation Delays U/D Control to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Set-up and Hold Times



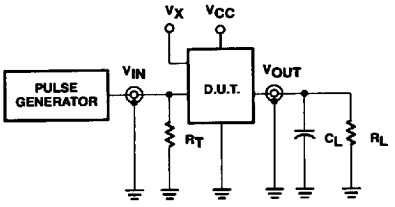
Waveform 5. Count Enable Set-Up and Hold Times



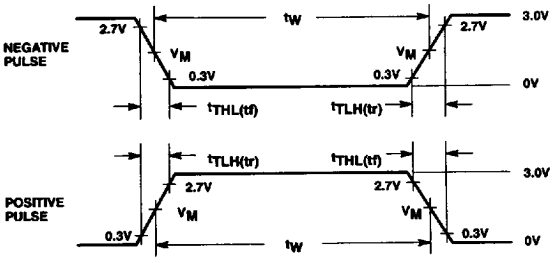
Waveform 6. Up/Down Control Set-Up and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns