

# M62001L/FP to M62008L/FP

## Low Power 2 Output System Reset IC Series

REJ03D0781-0100

Rev.1.00

Sep 14, 2005

### Description

The M62001 to M62008 are semiconductor integrated circuits whose optimum use is for the detection of the rise and fall in the power supply to a microcomputer system in order to reset or release the microcomputer system.

The M62001 to M62008 carry out voltage detection in two-steps and have two output pins. As Bi-CMOS process and low power dissipating circuits are employed, they output optimum signals through each output pin to a system that requires RAM backup. As output signals, interruption ( $\overline{\text{INT}}$ ) and compulsive reset ( $\overline{\text{RESET}}$ ) signals are available. The interruption signal ( $\overline{\text{INT}}$ ) is used to alter the microcomputer from normal mode to backup mode and vice versa. These output signals are classified into pulse type (M62001 to M62004) and hold type (M62005 to M62008).

### Features

- Bi-CMOS process realizes a configuration of low current dissipating circuits.

Circuit current

$$I_{CC} = 5 \mu\text{A} \text{ (Typ, normal mode, } V_{CC} = 5.0 \text{ V)}$$

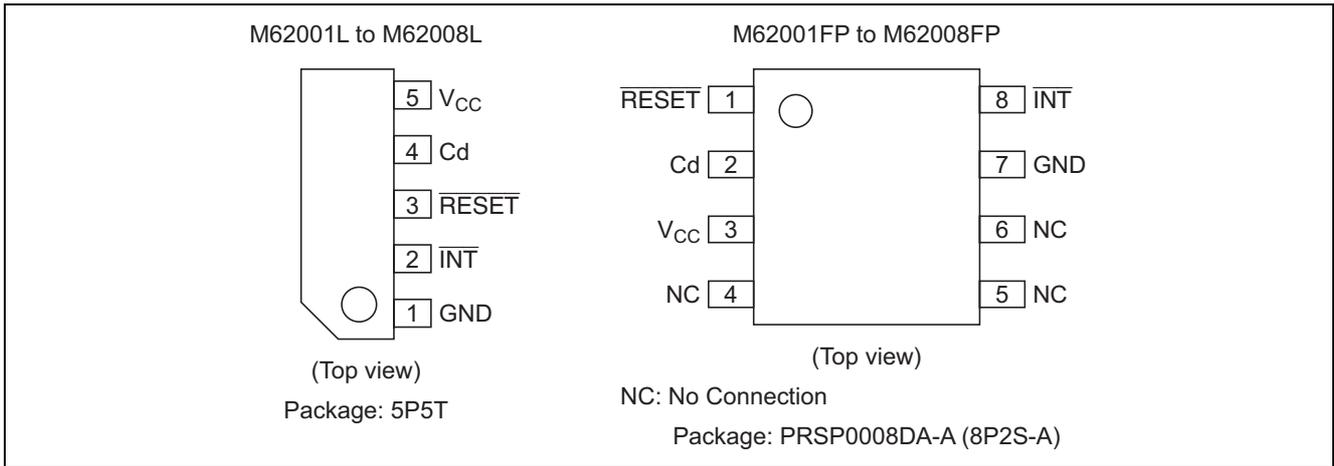
$$I_{CC} = 1 \mu\text{A} \text{ (Typ, backup mode, } V_{CC} = 2.5 \text{ V)}$$

- Two-step detection of supply voltage  
Detection voltage in normal mode (2 types)  
 $V_S = 4.45 \text{ V}/4.25 \text{ V}$  (Typ)  
Detection voltage in backup mode  
 $V_{BATT} = 2.15 \text{ V}$  (Typ)
- Two outputs  
Reset output ( $\overline{\text{RESET}}$ ): output of compulsive reset signal  
Interruption output ( $\overline{\text{INT}}$ ): output of interruption signal
- Two types of output forms: CMOS and open drain
- Two types of interruption output ( $\overline{\text{INT}}$ ) signals  
Pulse type (M62001 to M62004)  
Hold type (M62005 to M62008)
- Two types of outline packages  
5-pin plastic SIP (single in-line package)  
8-pin plastic SOP (mini flat package)
- Output based on RAM backup mode (see the timing chart)

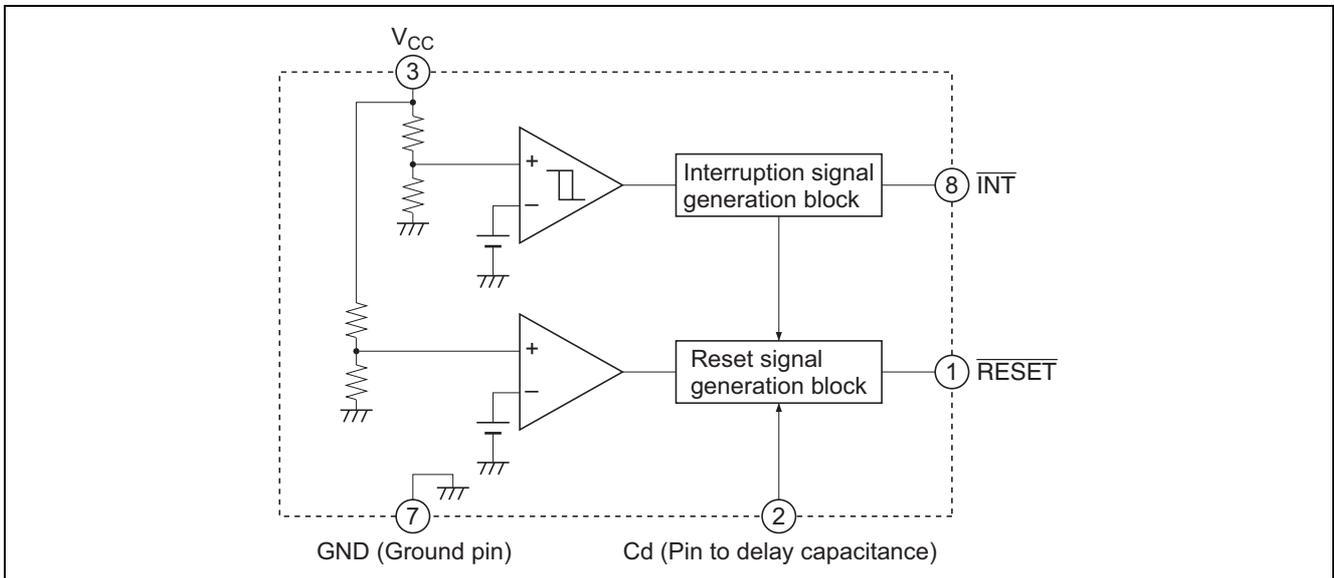
### Application

- Prevention of errors in microcomputer system in electronic equipment that requires RAM backup, such as office, industrial, and home-use equipment.

## Pin Arrangement



## Block Diagram



## Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

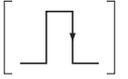
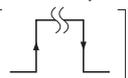
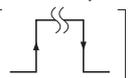
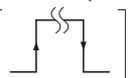
Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	8	V	
Output sink current	I <sub>sink</sub>	5	mA	
Power dissipation	P <sub>d</sub>	440	mW	
Thermal derating	K <sub>θ</sub>	4.4	mW/°C	Ta ≥ 25°C
Operating temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

## Electrical Characteristics

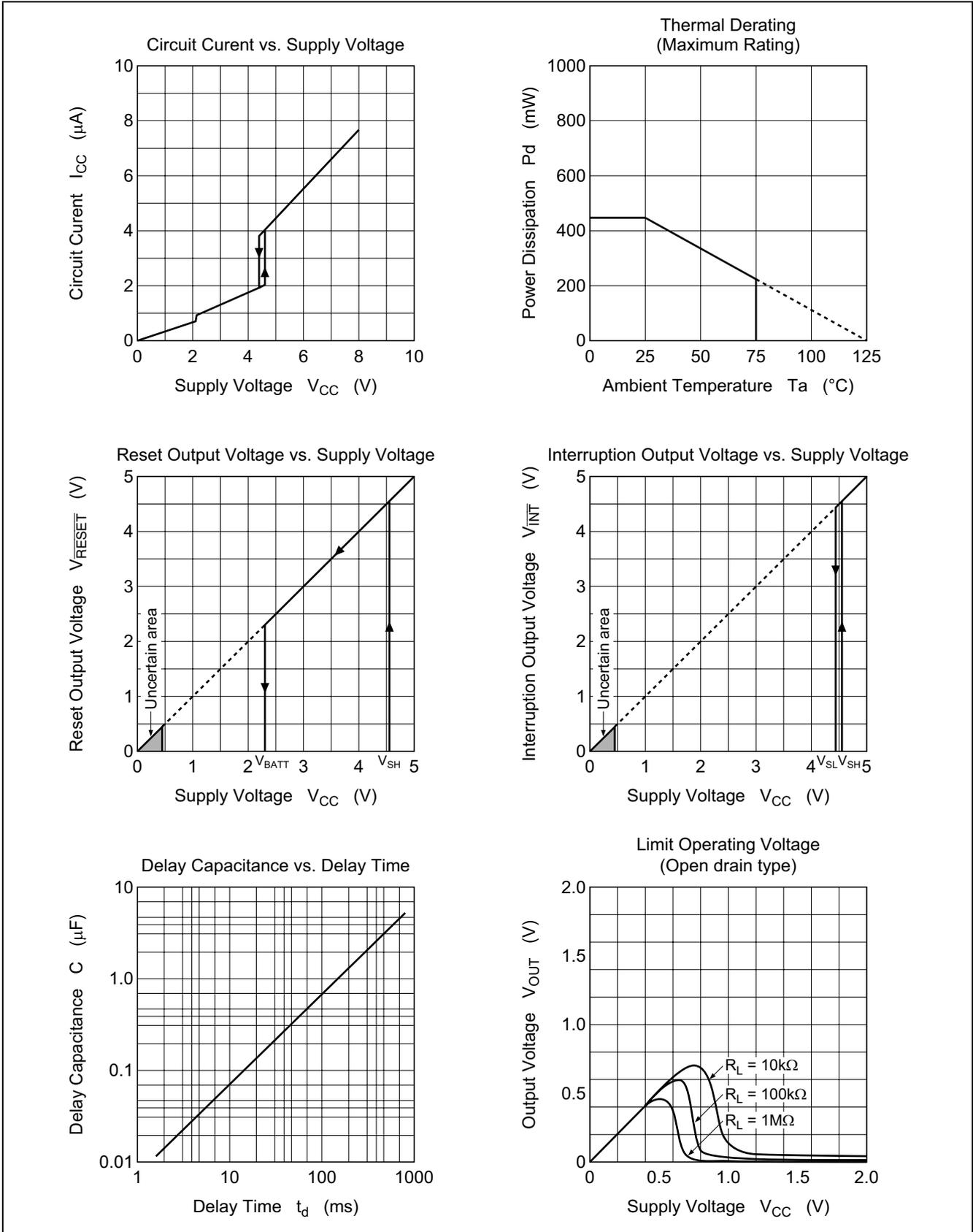
(Ta = 25°C, unless otherwise noted)

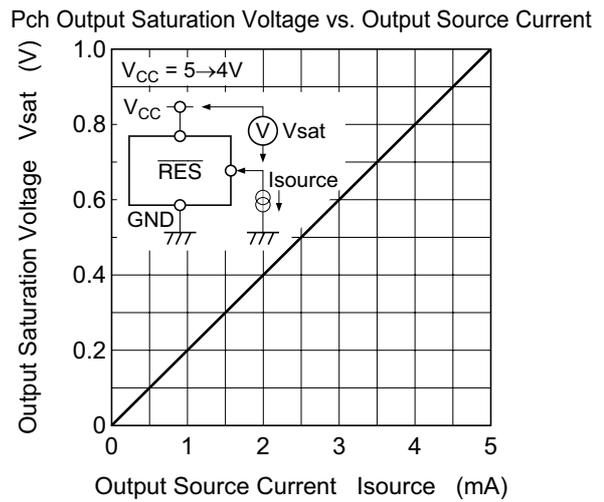
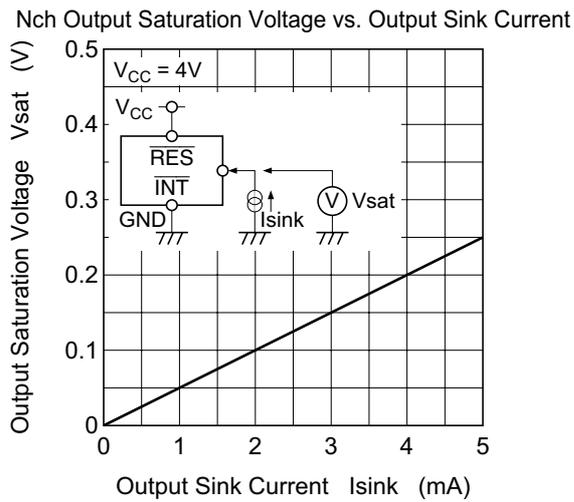
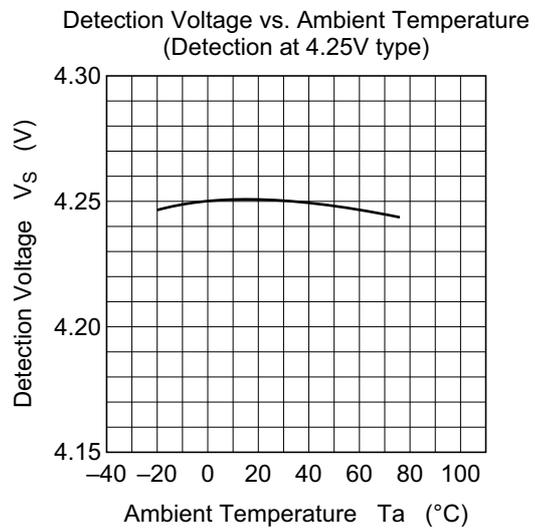
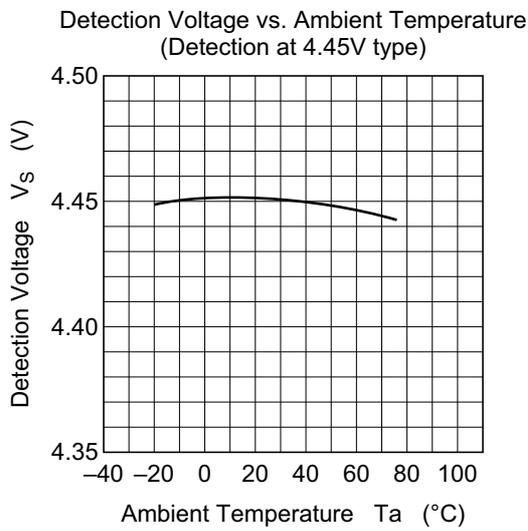
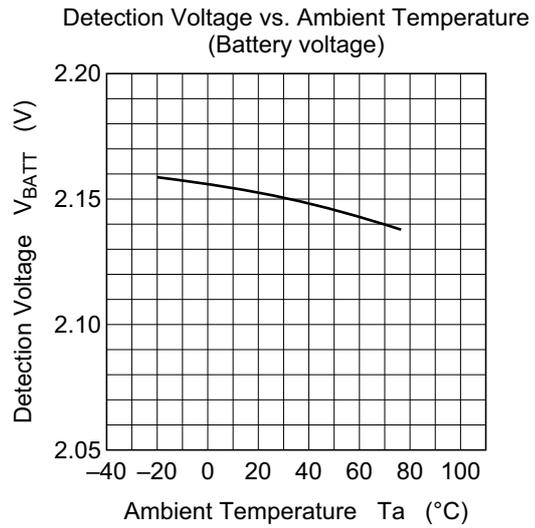
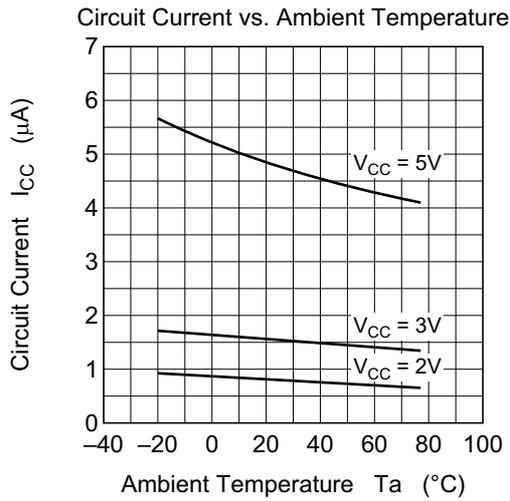
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V <sub>S</sub>	4.30	4.45	4.60	V	Interruption level during V <sub>CC</sub> drop (Equivalent to V <sub>SL</sub> )
		4.05	4.25	4.45		
Battery voltage	V <sub>BATT</sub>	2.00	2.15	2.30		Reset level at backup
Hysteresis voltage	ΔV <sub>S</sub>	—	100	—	mV	ΔV <sub>S</sub> = V <sub>SH</sub> - V <sub>SL</sub>
Circuit current	I <sub>CC</sub>	—	5.0	20	μA	V <sub>CC</sub> = 5.0V: in normal mode
		—	1.0	4		V <sub>CC</sub> = 2.5V: in backup mode
Sink ability	V <sub>sat1</sub>	—	0.2	0.4	V	V <sub>CC</sub> = 4V, I <sub>o</sub> = 4mA (Output saturation voltage of N-ch transistor)
Source ability	V <sub>sat2</sub>	—	0.2	0.4		V <sub>CC</sub> = 4V, I <sub>o</sub> = 1mA (Output saturation voltage of P-ch transistor) [CMOS output] M62001, M62003, M62005, M62007
Delay time	t <sub>d</sub>	—	50	—	ms	External capacitance Cd = 0.33μF
Pulse width	t <sub>pw</sub>	—	7	10	μs	Output pulse width (M62001, M62002, M62003, M62004)
Reset output response time	t <sub>RESET</sub>	—	30	—	μs	Time between V <sub>CC</sub> (when falling) = V <sub>BATT</sub> and output of $\overline{\text{RESET}}$ signal
Interruption output reset time	t <sub>INT</sub>	—	100	—	μs	Time between V <sub>CC</sub> (when falling) = V <sub>S</sub> and output of $\overline{\text{INT}}$ signal

## Summary of M62001L/FP to M62008L/FP

Type No.	Supply Voltage Detection Level V <sub>S</sub> (V)	Battery Voltage Detection Level V <sub>BATT</sub> (V)	Output Form	Interruption Signal Output Mode
M62001L/FP	4.45	2.15	CMOS	Pulse output 
M62002L/FP			Open drain	
M62003L/FP	4.25	2.15	CMOS	Hold output 
M62004L/FP			Open drain	
M62005L/FP	4.45	2.15	CMOS	Hold output 
M62006L/FP			Open drain	
M62007L/FP	4.25	2.15	CMOS	Hold output 
M62008L/FP			Open drain	

### Typical Characteristics





## Operating Principle

### Description

In general, the memory backup function of a microcomputer, as shown in figure 1, uses two diodes to switch between main power supply and backup power supply. The M62001 to M62008 are ICs that, in such memory backup operation, monitor in two steps each voltage on the  $V_{DD}$  line.

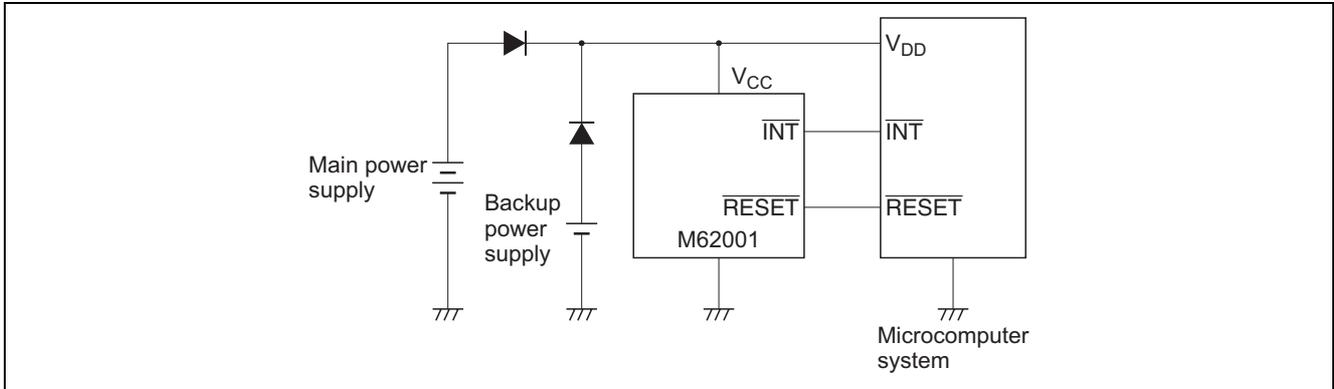


Figure 1

The ICs have an intelligent sequence such as substantial hysteresis action of  $\overline{\text{RESET}}$  toward normal state at restoration of supply voltage, as well as two-step detection in low power dissipation mode.

### Detailed Description

#### 1. Two-step detection

The ICs perform two-step detection of supply voltage and have two output pins ( $\overline{\text{INT}}$  and  $\overline{\text{RESET}}$ ). Although they have two comparators for two-step detection, they differ significantly from such that are simply provided with independent detectors, because the  $\overline{\text{RESET}}$  output signal is dependent at power-up and the like upon the  $\overline{\text{INT}}$  output signal.

#### 2. $\overline{\text{INT}}$ output (Detection of 4.45 V and 4.25 V)

The  $\overline{\text{INT}}$  output at the power-up of supply voltage detects  $V_{SH}$  (4.45 V/4.25 V) to inform the microcomputer system of the fact that the supply voltage has reached its normal level. When the supply voltage drops from its normal level to  $V_{SL}$  (4.45 V/4.25 V) an interruption signal is output to alter the microcomputer system into RAM backup mode. The microcomputer at this point enters sleep state and secures memory by a stop command issued by the interruption signal. These detection voltage,  $V_{SH}$  the rise, and  $V_{SL}$  the fall, of supply voltage, have a 100 mV hysteresis voltage between themselves.

$$V_{SH} - V_{SL} \approx 100 \text{ (mV)}$$

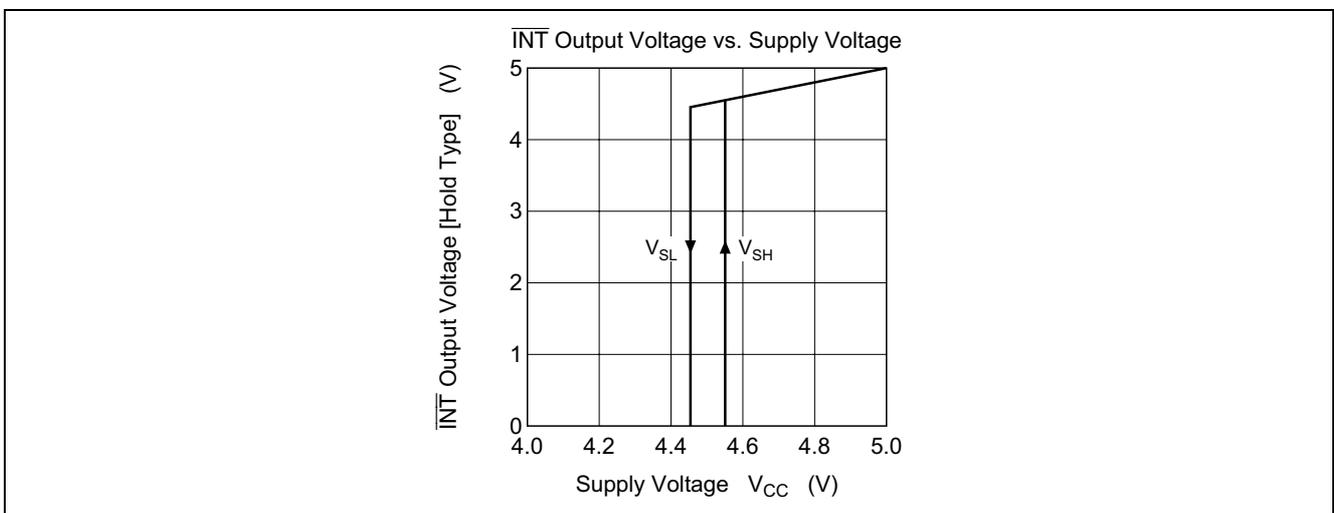


Figure 2  $\overline{\text{INT}}$  Output (Detection of 4.45 V and 4.25 V)

3.  $\overline{\text{RESET}}$  output (Detection of 2.15 V)

The  $\overline{\text{RESET}}$  outputs a signal to prevent the microcomputer from malfunctioning due to a drop in supply voltage.

When powering up,  $\overline{\text{RESET}}$  is kept at low level until the supply voltage reaches  $V_{\text{SH}}$ . If the supply voltage rises to  $V_{\text{SH}}$ ,  $\overline{\text{RESET}}$  is set to high level. By inserting a capacitor between the Cd pin and GND, it is possible to produce a desired delay time ( $t_d$ ). To set a delay time, equation below is used.

$$t_d \approx 1.52 \times 10^5 \times C \text{ (s)}$$

Once the supply voltage has exceeded  $V_{\text{SH}}$  and the  $\overline{\text{RESET}}$  output is set to high level,  $\overline{\text{RESET}}$  maintains the high level until the supply voltage drops to  $V_{\text{BATT}}$ . When the supply voltage drops to  $V_{\text{BATT}}$ ,  $\overline{\text{RESET}}$  goes low thereby resetting and initializing the microcomputer.

The  $\overline{\text{RESET}}$  output has a large hysteresis voltage of approximately 2 V between the rise in supply voltage at power-up and its fall.

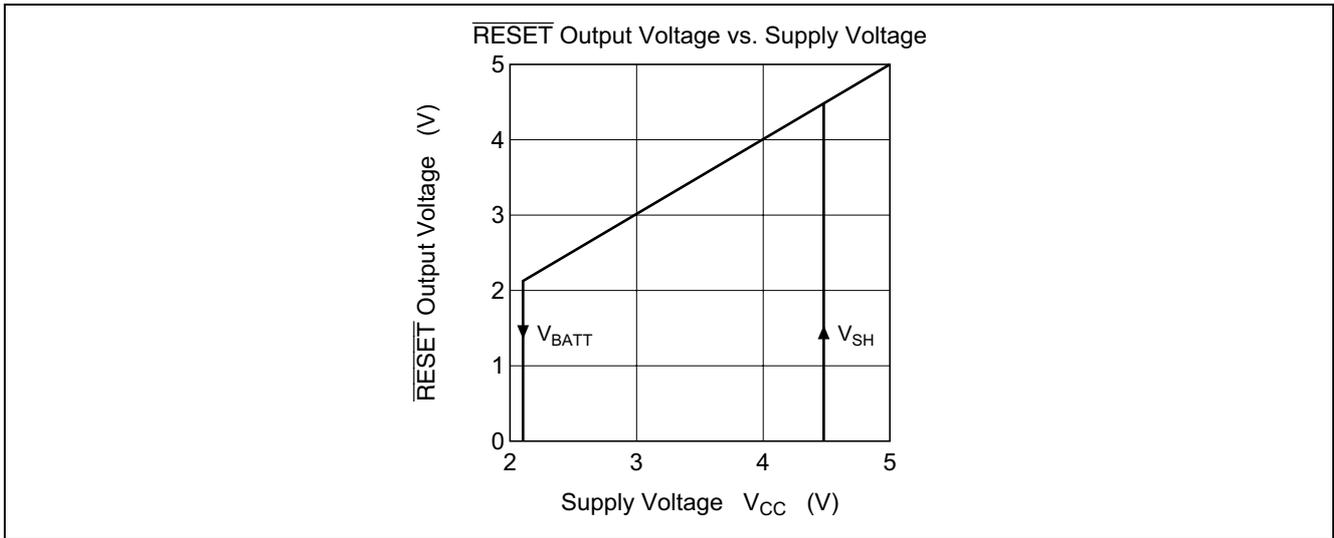


Figure 3  $\overline{\text{RESET}}$  Output (Detection of 2.15 V)

### Operating Description

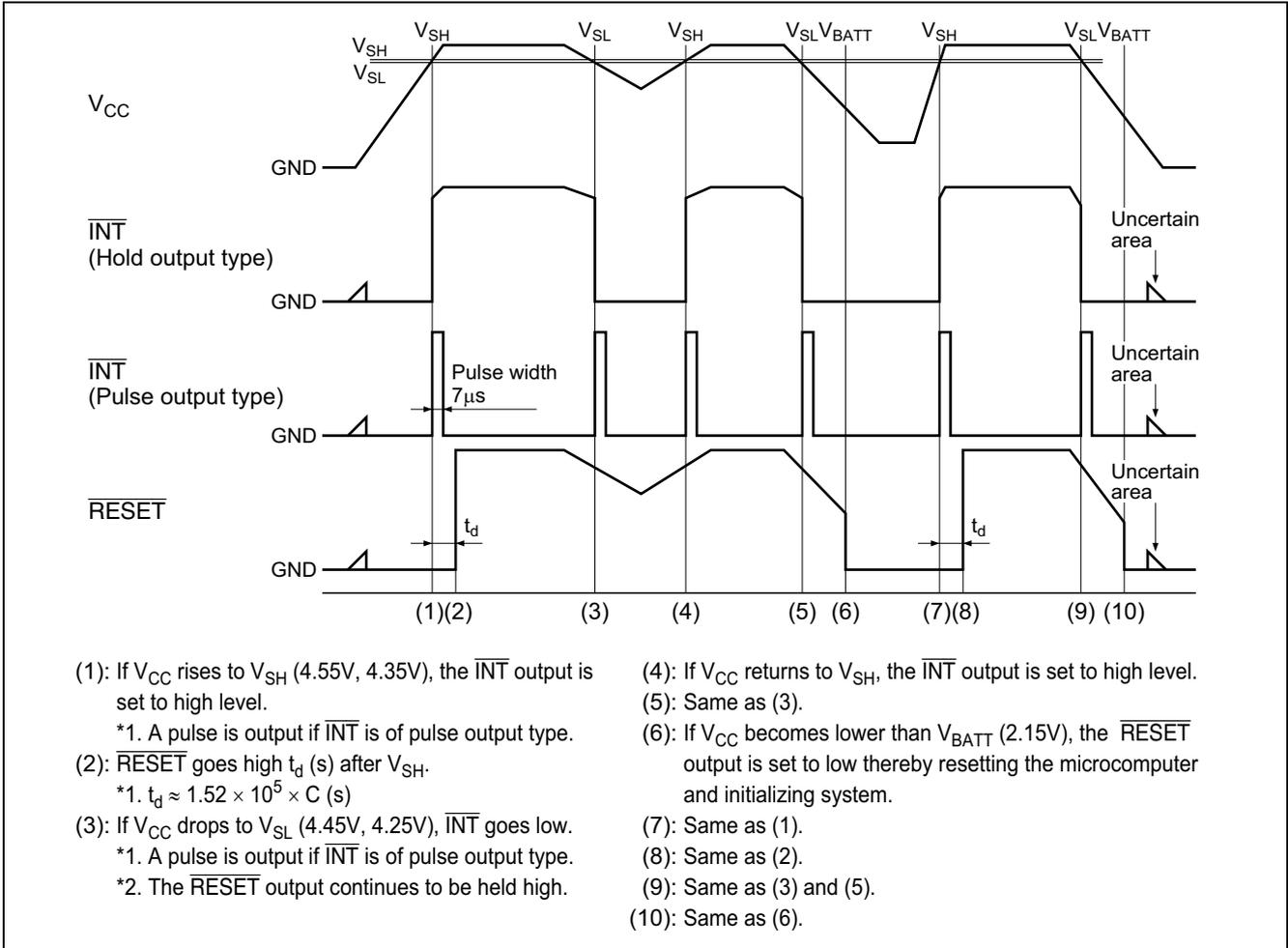


Figure 4 Operating Waveform

### Application Example

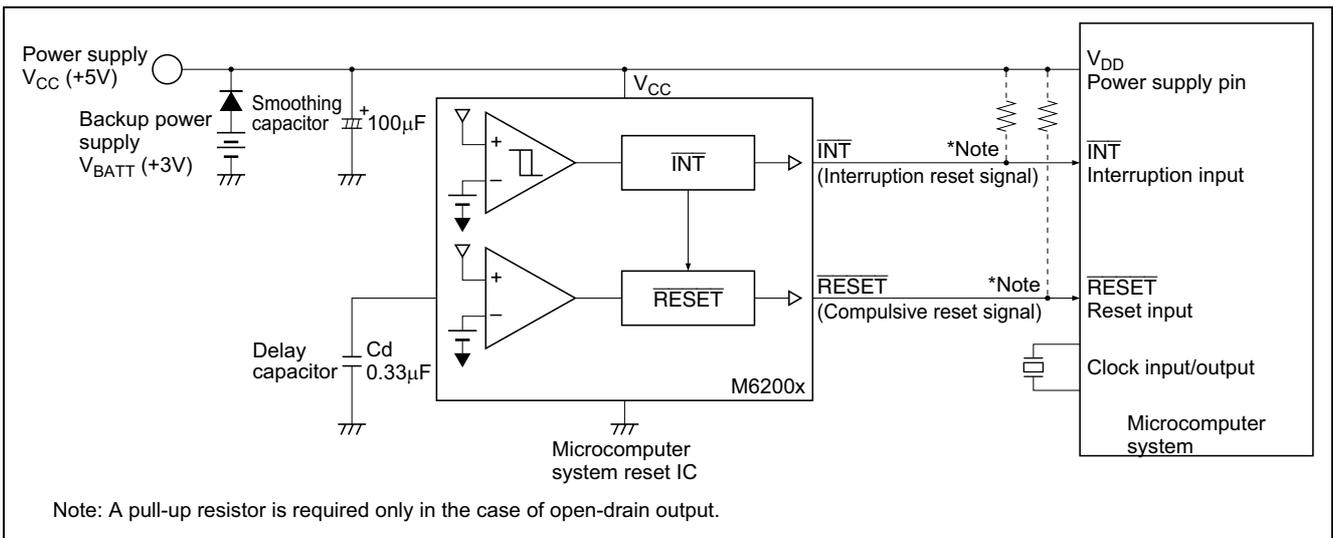
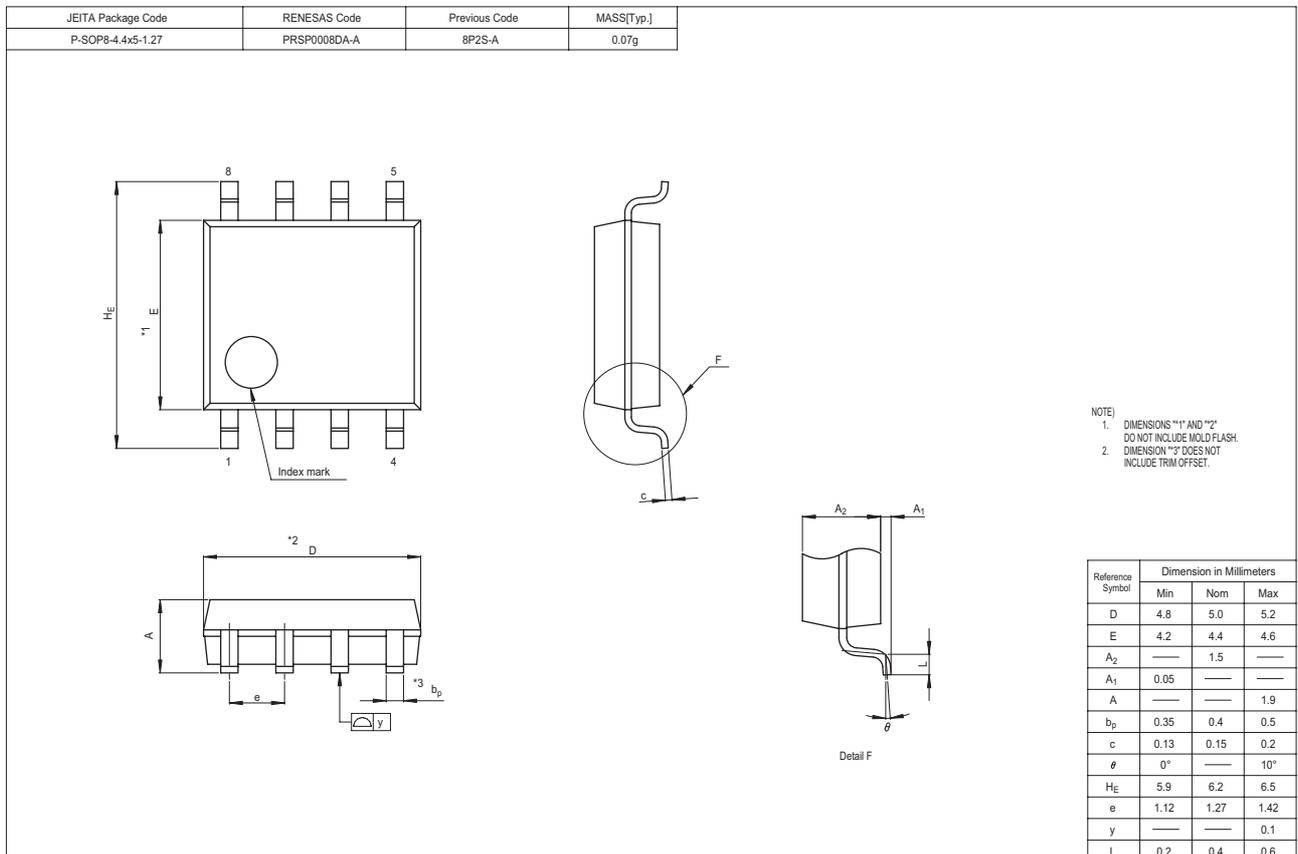
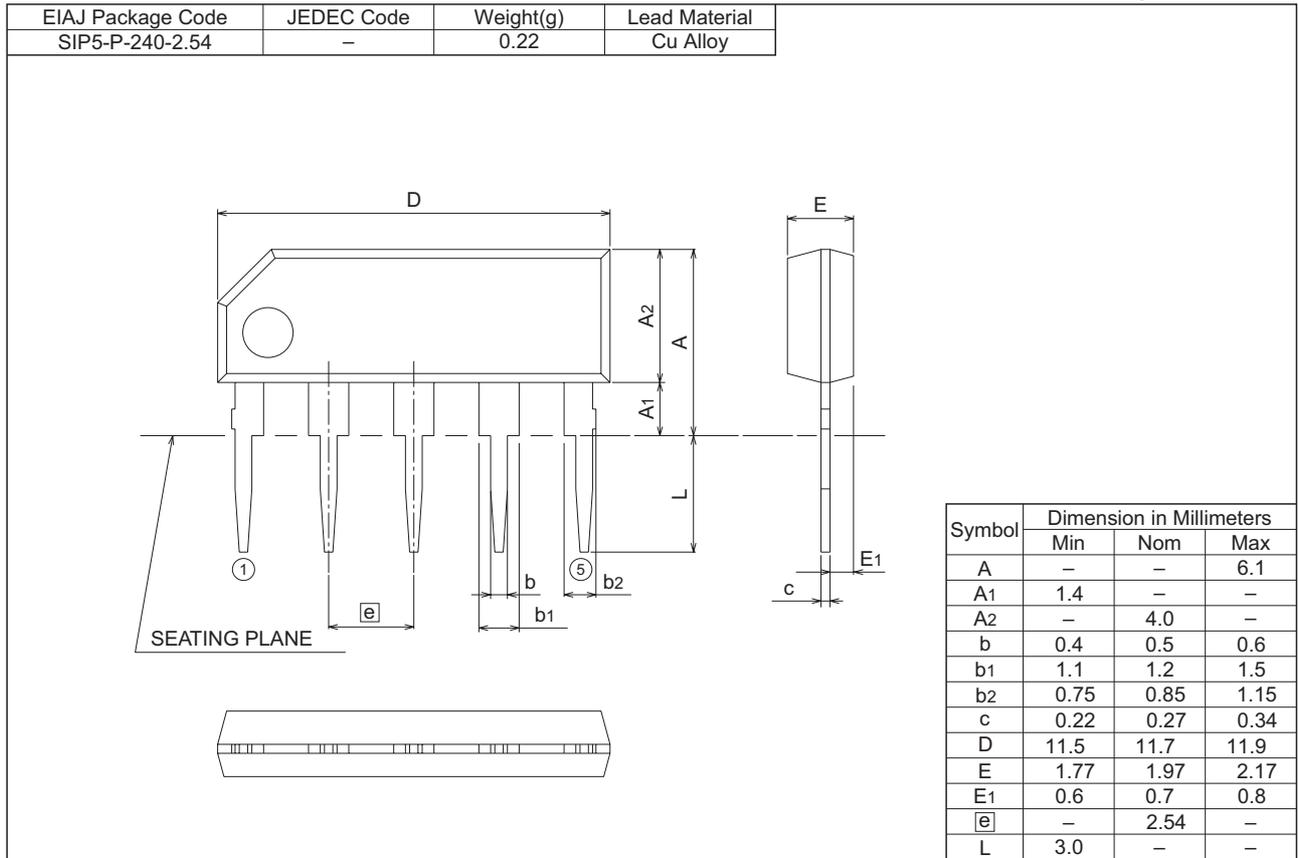


Figure 5 Application Example

Package Dimensions

5P5T

Plastic 5pin 240mil SIP



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