I-Cube®

IQX Family Data Sheet

Features

- SRAM-based, in-system programmable
- Switch Matrix
  - Non-Blocking
  - Identical and predictable delays
  - One-to-one, one-to-many and many-to-one connections
- I/O Ports
  - Individually programmable as input, output or bidirectional
  - For each I/O Port, clock, clock enable, input enable and output enable can be selected independently from a large pool of common control signals
  - 16 mA current drive
  - Separated I/O power pins for easy interfacing between 5V and 3V signals
- Clocked, Latched and Flow-through Dataflow Modes
  - As fast as 6 ns port-to-port delay in flow-through mode and 150 MHz clock rate in registered mode
- RapidConfigure™ parallel interface for fast, incremental configuration of Switch Matrix and I/O Port attributes
- 100% JTAG compliant
- Pin compatible with the IQ family devices

Description

The IQX family of SRAM-based bit-oriented switching devices is manufactured using a 0.6µm CMOS process. These devices offer clock speed of up to 150 MHz and fastest pin-to-pin delay of 6 ns.

The IQX devices are used in applications requiring dynamic switching and flexible routing /interconnection of signals. These applications include communication switches, network systems, image processing engines, file/video servers, testers and emulators.

At the heart of IQX devices is a non-blocking Switch Matrix. A line in the Switch Matrix can be connected to one or more other lines. The Switch Matrix lines are connected to I/O Ports with programmable functional attributes.

The RapidConfigure parallel interface allows connections in the Switch Matrix to be changed quickly and incrementally. This interface can also be used to configure I/O Port attributes individually and incrementally. In either case, data integrity is maintained on all unchanged signal paths through the device.

The IQX devices support the industry standard JTAG (IEEE 1149.1) interface for boundary scan testing. The same interface is also used for serially downloading the configuration bit stream into the devices.

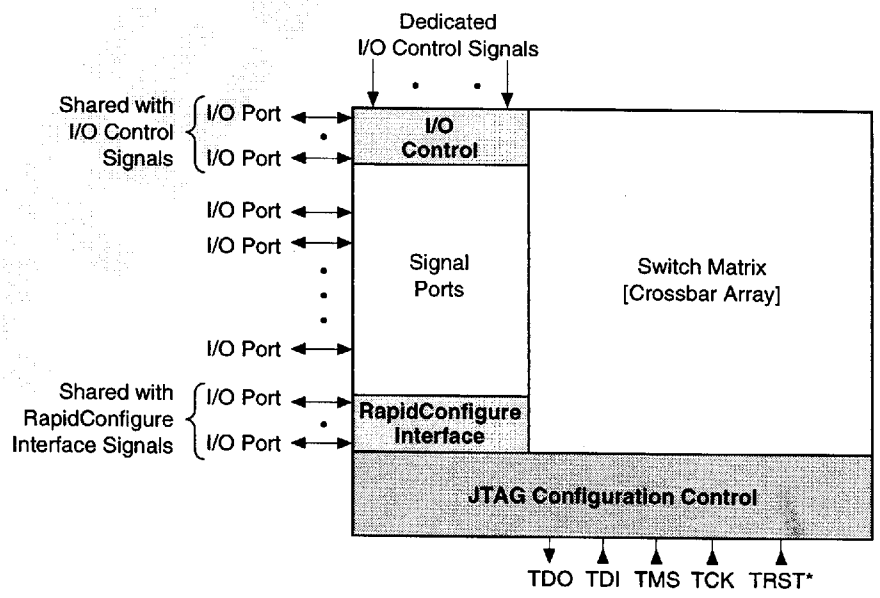


Figure 1: IQX Functional Block Diagram

Table of Contents

Architecture

IQX devices are SRAM-based bit-oriented switching matrices. The devices can be configured and controlled in-system by storing appropriate data into the internal SRAM cells and configuration registers. As shown in Figure 1, the main functional blocks of the device are the non-blocking Switch Matrix, Programmable I/O Ports, I/O Control signal block, RapidConfigure Configuration Interface and a JTAG-based Configuration Controller.

The full-featured programmable I/O Ports are connected to the corresponding lines in the Switch Matrix. The I/O Port control signals such as clock, clock enable, input enable, and output enable are used to control the flow of data through the I/O Ports.

The JTAG-based configuration controller is used to download the configuration bit stream serially into the I/O Port configuration registers and Switch Matrix SRAM cells, thereby establishing the desired functional attributes for the I/O Ports and connections among them through the Switch Matrix. Alternatively, the RapidConfigure parallel interface may be used to load the configuration data in the I/O Port Configuration Registers and Switch Matrix SRAM cells. The use of RapidConfigure interface enables quick configuration changes.

Non-blocking Switch Matrix

The Switch Matrix is an x-y routing structure (or grid). Each horizontal signal trace is *hardwired* to a corresponding vertical signal trace as shown by the junction dots in Figure 2. An I/O Port pin connects to this horizontal-vertical trace pair through a programmable buffer. Signal paths through the Switch Matrix are very well balanced, resulting in predictable and uniform pin-to-pin delays.

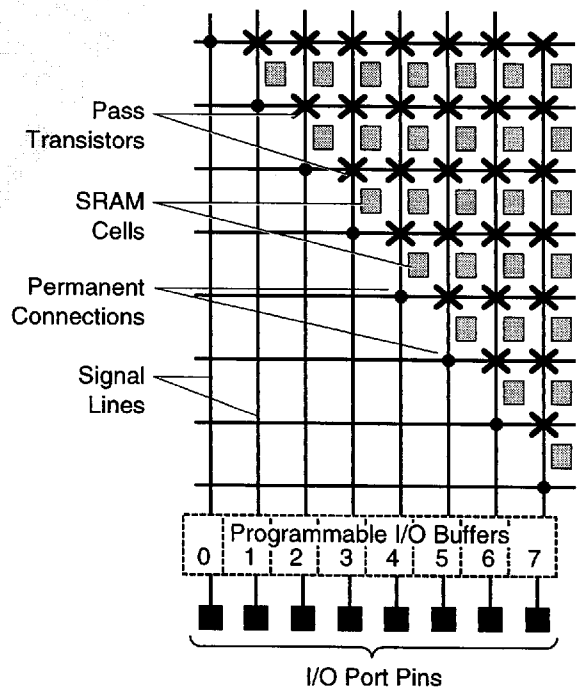


Figure 2: Switch Matrix Structure

A pass transistor whose ON/OFF state is controlled by a dedicated SRAM cell is placed at the intersection of two different signal lines. Signal multicasting/broadcasting operation is supported by allowing a Switch Matrix line carrying an incoming signal to be connected to multiple Switch Matrix lines carrying outgoing signals. Signal multiplexing is supported by allowing multiple Switch Matrix lines carrying incoming signals (controlled using input enable signals) to be connected to the same Switch Matrix line carrying an outgoing signal. It is also possible to create a common internal node among multiple Switch Matrix lines by making all pair-wise connections among these signal lines, and driving such a node by configuring the corresponding I/O Ports in the Bus Repeater mode. Refer to the section on "I/O Port Functional Modes" for more details.

Switch Control

As shown in Figure 3, there are two possible switch and SRAM cell locations for a connection between any two Switch Matrix lines. For example, the two possible switch (and SRAM cell) locations controlling a connection between signal lines i and j are row i (word i) and column j (bit j), or row j and column i. Only one location is populated with a switch and the controlling SRAM cell. This location is called the *real* location while the other one is referred to as the *ghost* location. The real cell locations form a unique pattern on the device die as described in Appendix A. The section on "RapidConfigure Interface" explains how this knowledge can be used to reduce the time it takes to change Switch Matrix connections.

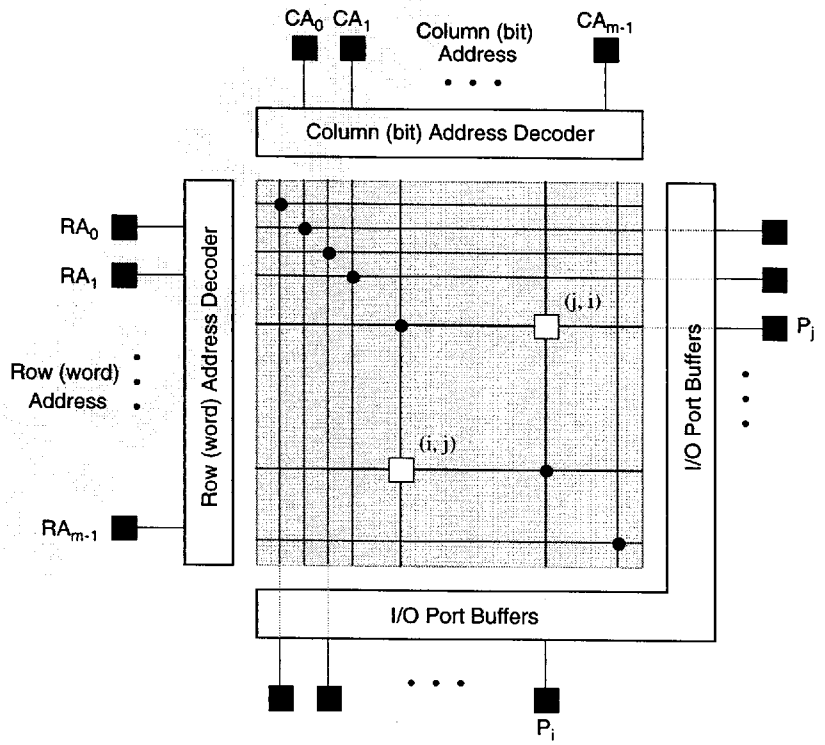


Figure 3: Switch Matrix Control

Programmable I/O Port

Each signal line in the Switch Matrix is connected to a programmable I/O Port. The functional attributes of individual I/O Ports can be programmed independently. The I/O Port attributes include its signal direction (in, out or bidirectional), data flow mode (flow-through, registered or latched), and pull-up current. Figure 4 shows the structure of the programmable I/O Port. The sources for the four control signals: clock (CLK), clock enable (CKE), input enable(IE), and output enable ($\overline{OE}$) are also programmable and are described later in the section on I/O Control Signals.

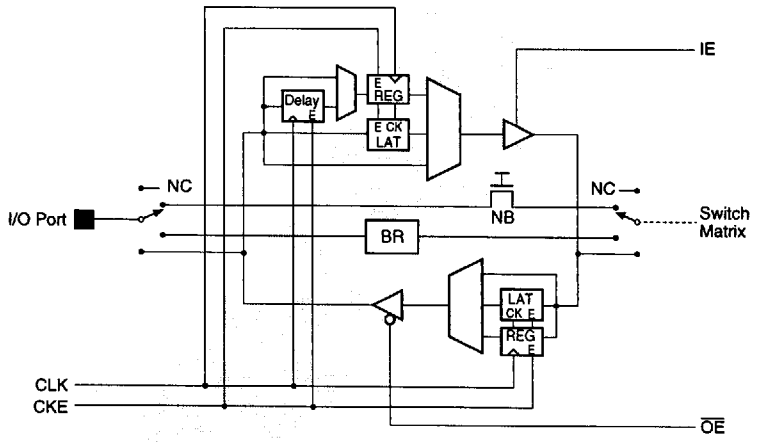


Figure 4: Programmable I/O Port

Programmable Pull-up Current

As shown in Figure 5, the I/O Port contains several n-channel pull-up devices. The normal pull-up current is supplied by a device which is switched on/off by internally generated control signal. An additional *static* pull-up current (I_{PU-WK}) or (I_{PU-SG}) can be programmed at each I/O Port pin. This additional pull-up current is primarily used for but not restricted to the Bus Repeater (BR) mode.

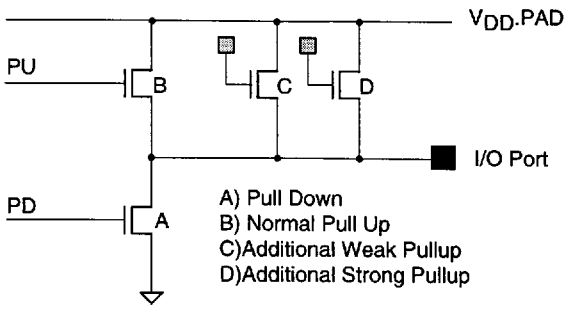


Figure 5: IQX Output Driver and Pull-Up Current

Pin and Array side Trickle Current

N-channel devices are used as a trickle current source (nominally 10µA) on the pin side and array side for each I/O Port. Upon reset, these current sources are turned ON. They can be turned OFF by configuring the I/O Port.

I/O Port Functional Modes

Table 1 describes the various modes of the I/O Port and the specification used by the I-Cube Development System Software for proper bit stream generation.

Legend:

Ax - Switch Matrix Signal
Px - I/O Port Signal
IE - Input Enable
$\overline{OE}$ - Output Enable
CLK - Clock
CKE - Clock Enable

Table 1: Summary of Programmable I/O Attributes for IQX Devices

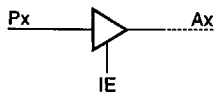
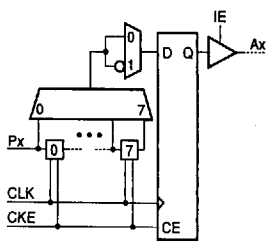
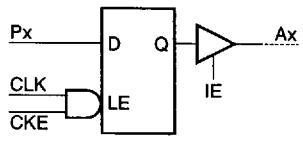
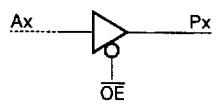
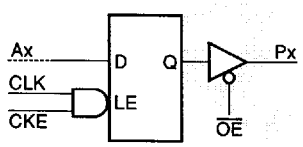
Symbol	I/O Port Function	Mnemonic
	**Input** - The external signal is buffered from the I/O Port pin to the corresponding Switch Matrix line. In this mode an optional input enable (IE) can be selected. Either polarity can be selected for IE. The default level is a logic 1.	IN
	**Registered Input** (with variable length shift register and inversion) - The external signal at the I/O Port pin is registered into a 7-bit edge-triggered shift register within the I/O Port. An 8-to-1 mux selects either the input (bit 0) or one of the 7 output bits of the shift register and connects it to the corresponding signal line in the Switch Matrix through a register. Any tap on the shift register can be selected. The true or complement of the incoming signal can be selected. The default is bit 0, true value. A clock source is required in this mode. Either edge of CLK can be selected. The default for CLK is rising edge. A clock enable (CKE) and input enable (IE) are also available but not required. Either polarity can be selected for IE and CKE. The default level for IE and CKE is a logic 1. The outputs of the shift register are unknown after hardware reset (TRST* = 0).	RI& [bit = value]& [INV = value]
	**Latched Input** - The external signal at the I/O Port pin is latched by a level-sensitive flip-flop within the I/O Port. A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE, and at least one must be specified. An input enable (IE) is also available but not required. Either polarity can be selected for CLK, CKE and IE. The default level for all three is a logic 1. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	LI
	**Output** - The internal signal is buffered from the corresponding Switch Matrix line to the I/O Port pin. In this mode an optional output enable ($\overline{OE}$) can be selected. Either polarity can be selected for OE. The default level is a logic 0.	OP
	**Latched Output**- The internal signal on the Switch Matrix line is latched by a level-sensitive flip-flop within the I/O Port. A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE, and at least one must be specified. An output enable ($\overline{OE}$) is also available but not required. Either polarity can be selected for CLK and CKE. The default level for both is a logic 1. Either polarity can be selected for $\overline{OE}$. The default level is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	LO

Table 1: Summary of Programmable I/O Attributes for IQX Devices

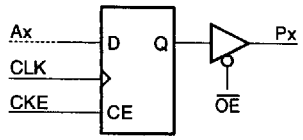
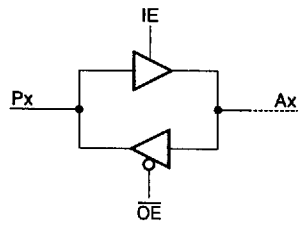
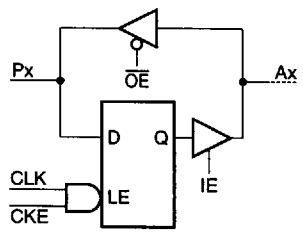
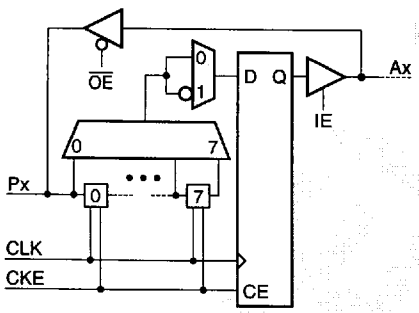
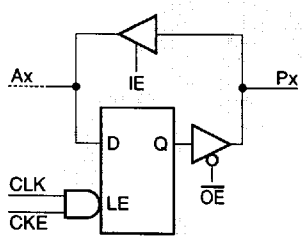
Symbol	I/O Port Function	Mnemonic
	**Registered Output** - The internal signal on the Switch Matrix line is registered by an edge-triggered flip-flop within the I/O Port. A clock source is required in this mode. Either edge of CLK can be selected. The default for CLK is rising edge. A clock enable (CKE) and output enable ($\overline{OE}$) are also available but not required. Either polarity can be selected for CKE and $\overline{OE}$. The default level for CKE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	RO
	**Bidirectional Transceiver** - In this mode, the I/O buffer acts as a bidirectional transceiver between the I/O Port pin and the corresponding Switch Matrix line. This mode requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for each but the default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. When the same source (with default polarities) is used for IE and $\overline{OE}$, it effectively acts as direction control. When the same control signal (with one polarity inverted) is used for IE and $\overline{OE}$, it effectively acts as a Bus Repeater (BR) (see below) when both are enabled, and as No Connect (NC) when neither is enabled.	BT
	**Bidirectional Transceiver with Latched Input** - This mode combines Latched Input (LI) and output buffer (OP). A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE, and at least one must be specified. Either polarity can be selected for CLK and CKE. The default level for both is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&LI
	**Bidirectional Transceiver with Registered Input** - This mode combines Registered Input with programmable tap and inversion (RI) and buffered Output (OP). A clock source is required in this mode. Either edge of CLK can be selected. The default for CLK is rising edge. A clock enable (CKE) is available but not required. Either polarity can be selected. The default level for CKE is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for each. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&RI& [bit = value]& [INV = value]
	**Bidirectional Transceiver with Latched Output** - This mode combines Latched Output (LO) and input buffer (IN). A latch enable source is required in this mode. The latch enable source is composed of CLK and CKE. At least one must be specified. Either polarity can be selected for CLK and CKE. The default level for both is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&LO

Table 1: Summary of Programmable I/O Attributes for IQX Devices

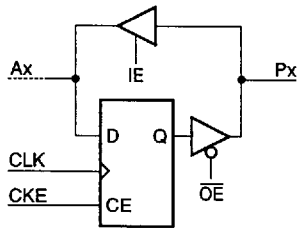
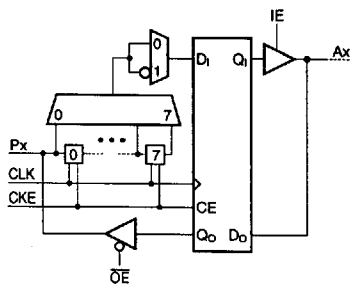
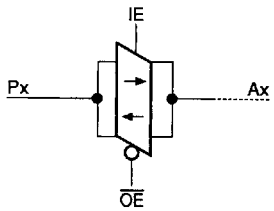
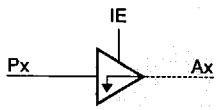
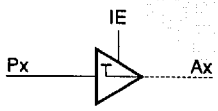
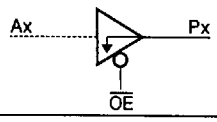
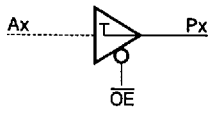
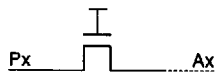
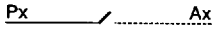
Symbol	I/O Port Function	Mnemonic
	**Bidirectional Transceiver with Registered Output** - This mode combines Registered Output (RO) and buffered Input (IN). A clock source is required in this mode. Either edge of CLK can be selected although the default is rising edge. A clock enable (CKE) is available but not required. Either polarity can be selected but the default level is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flop is unknown after hardware reset (TRST* = 0).	BT&RO
	**Bidirectional Transceiver with Registered I/O**- This mode is a combination of Registered Input (RI) with programmable tap and inversion, and Registered Output (RO). A clock source is required in this mode. Either edge of CLK can be selected. The default is rising edge. A clock enable (CKE) is available but not required. Either polarity can be selected for CKE. The default level is a logic 1. This mode also requires an input enable (IE) and output enable ($\overline{OE}$). Either polarity can be selected for IE and $\overline{OE}$. The default level for IE is a logic 1 and the default level for $\overline{OE}$ is a logic 0. The output of the flip-flops is unknown after hardware reset (TRST* = 0).	BT&RI& [bit = value]& [INV = value] &RO
	Other BT Modes- Other combinations of I/O Port modes (not covered in this table) are less likely but can be used. The mnemonic is BT [&RI | &LI] [&RO | &LO], where the specification inside the brackets "[ ]" is optional and "|" stands for either or. Insure that control signal requirements are met. In these modes, the output of the flip-flops is unknown after hardware reset (TRST* = 0).	
	**Bus Repeater** - In the Bus Repeater mode, the I/O Port behaves as a wire (with a non-zero propagation delay). This unique feature patented by I-Cube incorporates a self-sensing circuit to determine signal direction and does not require a direction control signal. When multiple I/O Ports, configured as "Bus Repeater", are connected together through the Switch Matrix to form a single internal node, an (open collector or tristatable) external signal appearing at any one of the I/O Ports gets repeated (or broadcast) to other I/O Ports. The Bus Repeater mode requires a pull-up current source (see section on "Programmable Pull-Up Current") to operate properly. For more details, refer to the Technical Note: "The Bus Repeater Mode" in the "Programmable Switching and Interconnect Devices - Applications Handbook".	BR
	**Array Side Force 0** - In this input mode, the Switch Matrix line is forced low (logic 0), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected. Either polarity can be selected for IE. The default level is a logic 1.	A0
	**Array Side Force 1** - In this input mode, the Switch Matrix line is forced high (logic 1), regardless of the signal on the corresponding I/O Port. In this mode an optional input enable (IE) can be selected. Either polarity can be selected for IE. The default level is a logic 1.	A1

Table 1: Summary of Programmable I/O Attributes for IQX Devices

Symbol	I/O Port Function	Mnemonic
	**Pin Side Force 0** - In this output mode, the I/O Port pin is forced low (logic 0), regardless of the signal on the corresponding Switch Matrix line. In this mode an optional output enable ($\overline{OE}$) can be selected. Either polarity can be selected for $\overline{OE}$. The default level is a logic 0.	F0
	**Pin Side Force 1** - In this output mode, the I/O Port pin is forced high (logic 1), regardless of the signal on the corresponding Switch Matrix line. In this mode an optional output enable ($\overline{OE}$) can be selected. Either polarity can be selected for $\overline{OE}$. The default level is a logic 0.	F1
	**Non-Buffered** - In this mode, the I/O Port pin is directly connected to the corresponding line in the Switch Matrix through a pass transistor, bypassing the buffer. This mode is not controlled by any of the four control signals (CLK, CKE, IE, and $\overline{OE}$) and is not used for passing digital signals.	NB
	**No Connect** - In this mode, the I/O Port pin is isolated from the Switch Matrix. This is done by tristating both the input and output part of the I/O buffer.	NC

I/O Control Signals

The IQX family has a structure that gives the user a lot of flexibility in controlling the behavior of each I/O Port. As shown in Figure 6 and described below, Clock (CLK), Clock Enable (CKE), Input Enable (IE) and Output Enable ($\overline{OE}$) signals for each I/O Port can be selected from multiple sources. The control polarity can also be individually selected.

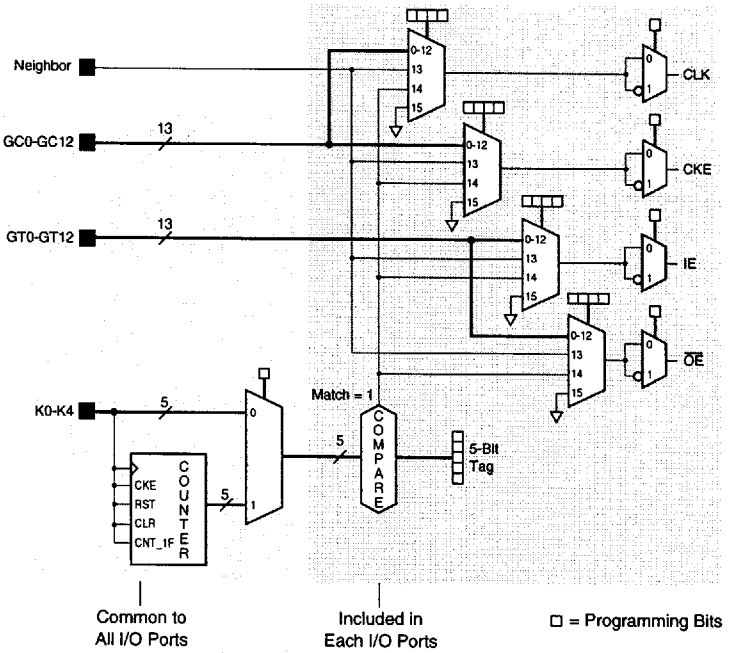


Figure 6: I/O Control

Clock Control

An I/O Port can be individually programmed to select its clock (CLK) and clock enable (CKE) signals from sixteen sources. The source can either be the two (four for IQX320 only) dedicated pins - GC0 and GC1 (GC0 through GC3 for IQX320), 11 (9 for IQX320) clock pins that are shared with signal I/O pins - GC2 through GC12 (GC4 through GC12 for IQX320), the nearest neighboring I/O Port, or the MATCH signal generated using Key Control (K0 - K4) pins.

Tristate Control

An I/O Ports can be individually programmed to select its Input Enable (IE) and Output Enable ($\overline{OE}$) signals from sixteen signals. The source can either be the four (five for IQX320 only) dedicated tristate pins - GT0 through GT3 (GT0 through GT4 for IQX320), nine (eight for IQX320) tristate pins that are shared with signal I/O pins - GT4 through GT12 (GT5 through GT12 for IQX320), the nearest neighboring I/O Port, or the MATCH signal generated using Key Control (K0 - K4) pins.

Neighboring I/O Port As A Control Source

A physically adjacent I/O Port on the die can be used as a source for any of the I/O control signals. Port 1 is the control source for Port 0, Port 2 is the control source for Port 1 and so on. Port 0 is the control source for the highest number I/O Port on the device *die*. Note that due to bondout restrictions the neighboring I/O Port may not always be brought out to a package pin on the IQ240B, IQ128B and IQ64B devices.

Key Control Pins As A Control Source

The Key Control feature on the IQX devices allows the user to encode mutually exclusive control signals for use as I/O control signals. The Key pins, K0 through K4 are shared with I/O Ports. This feature, shown schematically in Figure 6, works as follows:

Each I/O Port contains a 5-bit *tag* which can be programmed with a unique value when the I/O Ports are configured. A comparator in each I/O Port continuously compares the programmed tag value with the signals present on the Key pins or the output of the internal 5-bit counter. The output of the comparator, which produces a logic 1 on a match, can be selected as a control signal.

The Key Control is intended for use with level sensitive signals such as IE, $\overline{OE}$, CKE (in registered modes only). If Key Control is used in situations where a short glitch on the internal "Match" signal is unacceptable (i.e., using the Key Port for CLK in *registered* modes and CLK and/or CKE in *latched* modes), it is recommended that one of the Key pins be used as a qualifier and its value changed after the other Key pins have stabilized to prevent glitches on the internal "Match" signal. Note that when key match is used as Output Enable ($\overline{OE}$) the match will disable the driver, while a non-match will enable it. This can be reversed by configuring the I/O Port to use reverse polarity for $\overline{OE}$.

Depending on the value of the Counter Enable bit in the Mode Control Register (see Table 10, the key input to the 5-bit comparator comes either directly from the Key Pins (K0 through K4) or from the output of an internal 5-bit *up* counter. If the counter is selected by setting the Counter Enable bit to a logic 1, the Key pins serve as control inputs to the counter as described below.

K0/KCLK - Counter Clock input

K1/KCKE - Counter Clock Enable

K2/$\overline{KRST}$ - Counter (Synchronous) Reset

K3/$\overline{KCLR}$ - Counter (Asynchronous) Clear

K4/K1F - Counter Select "1F" Hex

The counter is a 5-bit modulo up counter controlled by the rising edge on the counter clock pin (KCLK). It counts up to the 5-bit value programmed in the Mode Control Register and then resets to zero on the following clock edge. KCKE pin is used to qualify the clock. Clocking is enabled when KCKE is high and disabled when low. When the K1F pin is asserted (high), the output of the counter is forced to "11111" regardless of the internal count. During this time the counter continues to count up in response to the clock input. When the $\overline{KRST}$ pin is asserted, the counter is reset on the following clock edge. $\overline{KCLR}$ on the other hand is an asynchronous clear. When asserted, the counter is immediately reset to zero. When the device is reset, the Counter Enable bit and the five Count Value bits are reset to zero.

Default Values for Control Signals

When the device is reset all I/O Ports are set to the default configuration of flow-through input (IN), This is achieved by setting the 16-to-1 muxes shown in Figure 6, to select input 15 (V_{ss}); while the 2-to-1 muxes used for polarity selections are set to select non-inverted value for Clock (CLK) and Clock Enable (CKE), and inverted value for Input Enable (IE) and Output Enable ($\overline{OE}$).

RapidConfigure (RC) Interface

The RapidConfigure (RC) Interface allows Switch Matrix connections and I/O Port configurations to be changed quickly. A single Switch Matrix connection can be made or broken in a single RapidConfigure cycle; while a single I/O Port or group of 2, 4, 8 or 16 I/O Ports (having the same configuration) can be configured in a minimum of one or maximum of eight RapidConfigure cycles.

The RapidConfigure interface shown in Figure 7 is a write only interface. Its operation is some what similar to a memory write cycle in a microprocessor system - it uses address, data and control signals to write to the Switch Matrix SRAM cells and I/O Port configuration registers. The Control bus, {P/$\overline{S}$, C[1:0]} defines the type of operation performed by the RapidConfigure cycle, while the Row Address, RA[m-1:0], and Column Address, CA[m-1:0], provide the necessary addresses and/or data for the different operations. The value "m" is different for different devices as shown in Table 2. $\overline{WE}$ (Write Enable) acts as chip select while $\overline{STROBE}$ is the write strobe.

Feature	IQX320	IQX240B	IQX160	IQX128B	IQX96	IQX64B
Total Number of I/O Ports	320	240	160	128	96	64
I/O Ports Used for RC Interface	22	22	20	18	18	16
Row Address and Column Address Bus Widths	9	9	8	7	7	6
I/O Ports whose connections can be changed using RC interface (1)	296	216	140	102	78	48

Table 2: RapidConfigure Interface Pin Count

Note:
(1) Due to the requirements for compatibility with the IQ Family and/or bondout restrictions, this number is lower than (# in row 1 - # in row 2) for some devices.

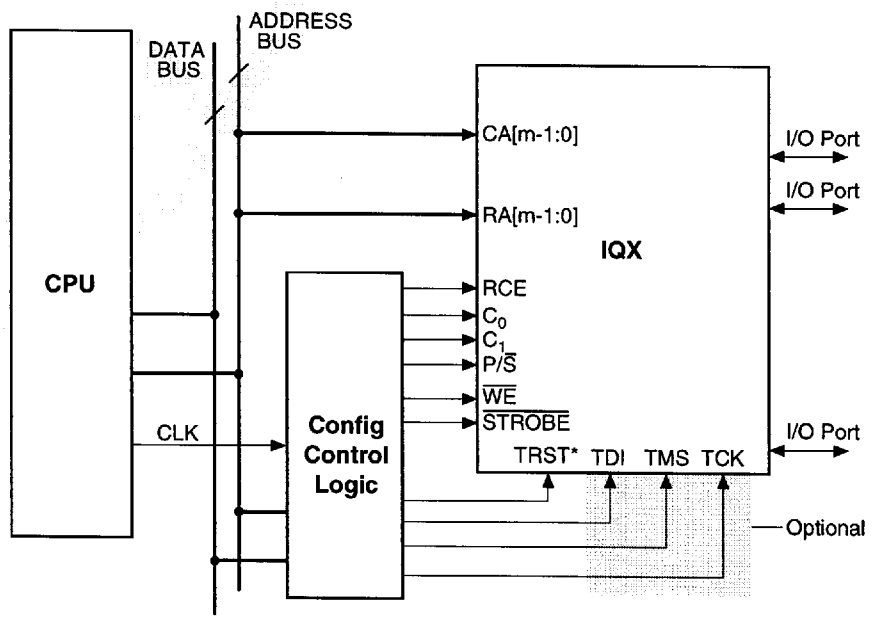


Figure 7: IQX RapidConfigure System Interface

In a typical system, an embedded processor will compute the required Row Address, Column Address and Control values and apply them to the IQX device. Alternatively, these values could be computed before hand using the I-Cube supplied development system software (Part# IDS100), and stored in a lookup table.

The RapidConfigure mode is enabled or disabled by correctly setting the RC *bit* in the Mode Control Register. Table 3 shows the different RapidConfigure options, depending on the values of the "RC" and "RM" *bits* in the Mode Control Register. During hardware reset (TRST* = 0) these bits are set to the signal value on the "RCE" *pin*. The values of these *bits* can then be changed if required using the JTAG serial interface. Note that the "P/$\overline{S}$" signal shown in Figure 7 is required only if the RapidConfigure interface is used for changing I/O Port configuration, i.e., when RC *bit* = 1 and RM *bit* = 1. The pin is available for use as signal I/O pin (I/O Port) when RM bit = 0. The following table summarizes the different options. Compatibility with the IQ family devices is achieved by connecting the RCE *pin* to V_{SS} on the board.

RC Bit	RM Bit	Operation
0	X	RapidConfigure Mode is disabled. The device can only be configured using the JTAG-based serial interface. In this case, the I/O Ports used for RapidConfigure Interface can be used for as signal I/O Ports.
1	0	RapidConfigure Mode is enabled for changing Switch Matrix connections but not for I/O Port configuration. The I/O Ports can only be configured using the JTAG-based serial interface. The signal coming from the P/$\overline{S}$ pin is forced to logic 0 internally. The P/$\overline{S}$ pin is available as a signal I/O Port.
1	1	RapidConfigure Mode is enabled for changing Switch Matrix connections and I/O Port configurations.

Table 3: RapidConfigure Options

The user must ensure that the I/O Ports used for the RapidConfigure interface are in the Input (IN) mode and any connections to corresponding signal lines in the Switch Matrix are cleared before attempting to configure the device using this interface. During device reset, the I/O Ports used for the RapidConfigure interface are set to the required Input (IN) and all connections in the Switch Matrix are cleared.

Switch Matrix Connection Changes

As indicated earlier, the Switch Matrix SRAM cells that control the connections among I/O Ports form a two dimensional array. Every SRAM cell location in the Switch Matrix that is being written to is uniquely identified by its Row (or Word) Address and Column (or Bit) Address. The *real* SRAM cell responsible for the connection between two I/O Port numbers "i" and "j" on the device *die* has the Row Address of Binary (i) and Column Address of Binary (j), or vice versa. Furthermore, when dealing with the bondout devices IQX240B, IQX128B and IQX64B, the I/O Port numbers on the device *package* must first be mapped to the I/O Port number on the device *die* to determine the Row and Column Address of the *real* SRAM cell. Refer to Appendix A for the tables and decision logic used to determine the location of the real SRAM cell, and the mapping of I/O Port numbers on the device package to I/O Port numbers on the device die.

The Control bus, {P/$\overline{S}$=0, C[1:0]} specifies the type of connection change, either make or break; the Row and Column Addresses are the values corresponding to the two I/O Port numbers as determined using the tables in Appendix A. P/$\overline{S}$ is set to 0 when changing Switch Matrix connections using RapidConfigure.

As indicated in Table 4, when the control bit C1 is held low during a make or break operation, the remaining SRAM cells belonging to the word addressed by the Row Address are automatically cleared. This feature can be used to speed up connection changes as described below.

In one common crossbar application, the signal I/O Ports on the device are divided into equal groups of inputs and outputs, and a pin in the output group is required to be connected to any pin in the input group. By judicious assignment of the I/O Ports to the output group, one can ensure that for *every* output port, the *real* SRAM cells controlling the connection between that output port and *all* ports in the input group fall on the word corresponding to the output port number. With this assignment, when establishing a new connection using RapidConfigure, any existing connection to that output I/O Port is automatically broken (C1=0). Thus a connection change, i.e., breaking an existing connection and then making a new one, can be accomplished in one RapidConfigure cycle. Tables in Appendix A provide information on determining the word locations of real SRAM cells. Refer to Technical Note #D-32-014, "Switching A Connection In One RapidConnect Cycle" for more details.

Attempting to alter the contents of the SRAM cells responsible for connections to the I/O Ports used for the RapidConfigure Interface will result in unpredictable results.

Operation	Control Bus {P/$\overline{S}$, C[1:0]}	Row Address RA[m-1:0]	Column Address CA[m-1:0]
Break the connection between I/O Ports i & j by writing a "0" to the SRAM cell location whose Row Address is i and Column Address is j, [0 ≤ i, j ≤ r]. Other SRAM cells are unchanged, i.e., no other connections are affected.[2,3]	0 10	BINARY(i)[1]	BINARY(j)
Make the connection between I/O Ports i & j by writing a "1" to the SRAM cell location whose Row Address is i and Column Address is j, [0 ≤ i, j ≤ r]. Other SRAM cell are unchanged, i.e., no other connections are affected.[2,3]	0 11	BINARY(i)	BINARY(j)
Break the connection between I/O Ports i & j by writing a "0" to the SRAM cell location whose Row Address is i and Column Address is j, [0 ≤ i, j ≤ r]. Clear all SRAM cells on row i; i.e., break all the connections controlled by the *real* SRAM cells belonging to row i.[2,3]	0 00	BINARY(i)	BINARY(j)
Make the connection between I/O Ports i & j by writing a "1" to the SRAM cell location whose Row Address is i and Column Address is j, [0 ≤ i, j ≤ r]. Clear all SRAM cells on row i; i.e., break all the connections controlled by the *real* SRAM cells belonging to row i.[2,3]	0 01	BINARY(i)	BINARY(j)

Table 4: Changing Switch Matrix Connections Using RapidConfigure

Notes:
(1) Binary(i) is the m-bit binary equivalent value of i. Right most bit is LSB. m equals Row/Column Address width. "i" and "j" refer to the I/O Port number on the device *die*.
(2) r is the I/O Port number on the die corresponding the highest available signal I/O Port.
(3) Assumes the real SRAM cell controlling the connection has Row Address = Binary(i)

I/O Port Configuration

Configuring I/O Ports using the RapidConfigure interface involves two steps. During the first step the 50-bit I/O Port Configuration Holding Register, consisting of seven 8-bit segments, is loaded with the configuration data. The loading is accomplished one 8-bit segment at a time, and may take up to 7 RapidConfigure cycles to

load this register. In the second step, the data in the I/O Port Configuration Holding Register is completely transferred to the individual I/O Ports in a single RapidConnect cycle. A single I/O Port, or a group of 2, 4, 8 or 16 *contiguous* I/O Ports with a starting address of modulo 2, 4, 8 or 16 respectively, (and requiring the same configuration) can be configured in a single RapidConfigure cycle during this step.

When using RapidConfigure for configuring I/O Ports, the Control bus, {P/$\overline{S}$ = 1, C[1:0]} specifies the type of operation; and the Row and Column Addresses provide the information about the I/O Port, or the group of ports to be configured. P/$\overline{S}$ is set to 1 when configuring I/O Ports using RapidConfigure. Refer to Table 5 for details. The I/O Port information specified in the Row and Column address values applies to the I/O pad location on the *die*. When using the RapidConfigure interface for configuring bondout versions such as the IQX240B, IQX128B and IQX64B, proper translation for I/O Port number on the package to the corresponding I/O Port number on the die must first be made. Refer to Appendix A for the mapping.

I/O Ports used for the RapidConfigure interface P/$\overline{S}$, C[1:0], RA, CA, $\overline{WE}$ and $\overline{STROBE}$, cannot be configured using the RapidConfigure interface. Combinations not listed in Table 5 may result in unpredictable results and should be avoided.

Operation	Control Bus {P/$\overline{S}$, C[1:0]}	IQX320, IQX240B		IQX160		IQX128B	
		Row Add. RA[8:0]	Col. Add. CA[8:0]	Row Add. RA[7:0]	Col. Add. CA[7:0]	Row Add. RA[6:0]	Col. Add. CA[6:0]
Load Configuration Register[1]	1 10	000000sss	0ddddddd	0000sssd	0ddddddd	000sssd	ddddddd
Configure Port i [0 ≤ i ≤ r][2, 3]	1 11	ppppppppp	000000001	ppppppppp	00000001	ppppppp	0000001
Configure 2 I/O Port Group	1 11	pppppppp0	000000011	pppppppp0	00000011	pppppp0	0000011
Configure 4I/O Port Group	1 11	ppppppp00	000000111	ppppppp00	00000111	ppppp00	0000111
Configure 8 I/O Port Group	1 11	pppppp000	000001111	ppppp000	00001111	pppp000	0001111
Configure 16 I/O Port Group	1 11	ppppp0000	000011111	pppp0000	00011111	ppp0000	0011111

Operation	Control Bus {P/$\overline{S}$, C[1:0]}	IQX96		IQX64B	
		Row Add. RA[6:0]	Col. Add. CA[6:0]	Row Add. RA[5:0]	Col. Add. CA[5:0]
Load Configuration Register[1]	1 10	00sssdd	0ddddddd	0sssdd	dddddd
Configure Port i [0 ≤ i ≤ r][2, 3]	1 11	ppppppp	0000001	pppppp	000001
Configure 2 I/O Port Group	1 11	pppppp0	0000011	ppppp0	000011
Configure 4I/O Port Group	1 11	ppppp00	0000111	pppp00	000111
Configure 8 I/O Port Group	1 11	pppp000	0001111	ppp000	001111
Configure 16 I/O Port Group	1 11	ppp0000	0011111	pp0000	011111

Table 5: Configuring I/O Ports Using RapidConfigure Interface

Notes:

(1) "sss" is the 8-bit segment in the 50-bit I/O Port Configuration Holding Register and ddddddddd is the 8-bit data to be loaded. Right most bits are LSBs.

(2) "ppppp...." is the I/O Port or I/O Port Group number to be configured. This vector is 9-bits long or less, depending on the device and size of the I/O Port Group. The I/O Port Group is a contiguous group of I/O Ports with the lowest I/O Port number being (ppppp....) multiplied by (Number of Ports in the Group).

(3) "r" is the I/O Port number on the die corresponding to the highest I/O Port number on the package that can be configured using RapidConfigure.

I/O Port Configuration Holding Register

I/O Port Configuration Holding Register is a 50-bit register that holds I/O Port configuration data. It consists of seven 8-bit segments and is loaded 8-bits at a time using RapidConfigure interface. The data in this holding register is loaded into I/O Port configuration cells during the I/O Port configuration operation using RapidConfigure. Table 6 describes the I/O Port programming bits and shows their location in the I/O Port Configuration Holding Register. Table 7 shows the bit values for the various I/O Port configurations.

Table 6: I/O Port Configuration Bits

Name	Seg #	Bit #	Group Function	Default Value	Description
IES0	0	0	Input Group	1	Input Enable (IE) Source Bit 0 (LSB).
IES1	0	1		1	Input Enable (IE) Source Bit 1.
IES2	0	2		1	Input Enable (IE) Source Bit 2.
IES3	0	3		1	Input Enable (IE) Source Bit 3 (MSB).
INV_IE	0	4		1	Invert Polarity for Input Enable; Default is Active High.
IN	0	5		1	Input Port Mode.
A0	0	6		0	Force Array Side Low.
A1	0	7		0	Force Array Side High.
OES0	1	0	Output Group	1	Output Enable ($\overline{OE}$) Source Bit 0 (LSB).
OES1	1	1		1	Output Enable ($\overline{OE}$) Source Bit 1.
OES2	1	2		1	Output Enable ($\overline{OE}$) Source Bit 2.
OES3		3		1	Output Enable ($\overline{OE}$) Source Bit 3 (MSB).
INV_OE	1	4		0	Invert Polarity for Output Enable, Default is Active Low.
OP	1	5		0	Output Port Mode.
F0	1	6		0	Force Pin Side Low.
F1	1	7		0	Force Pin Side High.
CLKS0	2	0	Clock, Register, and Latch Group	1	Clock (CLK) Source Bit 0 (LSB).
CLKS1	2	1		1	Clock (CLK) Source Bit 1.
CLKS2	2	2		1	Clock (CLK) Source Bit 2.
CLKS3	2	3		1	Clock (CLK) Source Bit 3 (MSB).
LO	2	4		0	Latched Output Mode.
LI	2	5		0	Latched Input Mode.
RO	2	6		0	Registered Output Mode.
RI	2	7		0	Registered Input Mode.

Table 6: I/O Port Configuration Bits

Name	Seg #	Bit #	Group Function	De-fault Value	Description
CKES0	3	0	Clock Enable Group	1	Clock Enable (CKE) Source Bit 0 (LSB).
CKES1	3	1		1	Clock Enable (CKE) Source Bit 1.
CKES2	3	2		1	Clock Enable (CKE) Source Bit 2.
CKES3	3	3		1	Clock Enable (CKE) Source Bit 3 (MSB).
INV_CKE	3	4		1	Invert Polarity for Clock Enable; Default is enabled when high for Register and transparent when High for Latch.
INV_CLK	3	5		0	Invert Polarity for Clock; Default is Rising Edge Triggered for Register and Transparent when High for Latch.
INV_PI	3	6		0	Invert Input Data in Registered Input (RI) mode.
reserved	3	7		0	Reserved for internal use. Must be set to default value.
K0	4	0	Key Control and Pipeline Delay Group	0	Key Tag Bit 0 (LSB).
K1	4	1		0	Key Tag Bit 1.
K2	4	2		0	Key Tag Bit 2.
K3	4	3		0	Key Tag Bit 3.
K4	4	4		0	Key Tag Bit 4 (MSB).
DELAY0	4	5		0	Input Pipeline Delay Bit 0 (LSB).
DELAY1	4	6		0	Input Pipeline Delay Bit 1.
DELAY2	4	7		0	Input Pipeline Delay Bit 2 (MSB).
BR	5	0	Misc. Group	0	Bus Repeater Mode.
IAS	5	1		1	Array Side Trickle Current.
IPS	5	2		1	Pin Side Trickle Current.
PU_WK	5	3		0	Weak Static Pull Up Current.
PU_SG	5	4		0	Strong Static Pull Up Current.
NB	5	5		0	Non-Buffered Mode.
reserved	5	6		1	Reserved for internal use. Must be set to default value.
reserved	5	7		1	Reserved for internal use. Must be set to default value.
reserved	6	0	Test Group	0	Reserved for internal use. Must be set to default value.
reserved	6	1		0	Reserved for internal use. Must be set to default value.
reserved	6	2-7		0	Reserved, Currently Not Implemented.
reserved	7	0-7		0	Reserved, Currently Not Implemented.

I/O Port Configurations and Holding Register Contents

The contents of the Configuration Register for the different I/O Port configurations are shown in Table 7 below. All other combinations not listed are illegal and may result in improper operation or damage to the device.

I/O Mode	Mnemonic	Note	Seg 6 Bit 76543210	Seg 5 Bit 76543210	Seg 4 Bit 76543210	Seg 3 Bit 76543210	Seg 2 Bit 76543210	Seg 1 Bit 76543210	Seg 0 Bit 76543210
			....	..NPPIIB ..BUUPAR .....SS. ...SW... ...GK...	DDDKKKKK EEE43210 LLL..... AAA..... YYY..... 210.....	.IIICCCC .NNNKKKK .VVVEEEE ..CCSSSS .PLK3210 .IKE....	RRLLCCCC IOIOLLLL ....KKKK ....SSSS 3210	FFOIOOOO 10PNEEEE ...VSSSS ...O3210 ...E....	AAIIIIII 10NNEEEE ...VSSSS ...I3210 ...E....
After Reset Default			00000000	11000110	00000000	01111111	00001111	00001111	00111111
Input	IN	1	00000000	11000110	00000000	00011111	00001111	00001111	001*TTTT
Latched Input	LI	1,2	00000000	11000110	000KKKKK	00~#EEEE	0010CCCC	00001111	001*TTTT
Registered Input	RI	1,2,3	00000000	11000110	DDDKKKKK	0/~#EEEE	1000CCCC	00001111	001*TTTT
Output	OP	1,6	00000000	110SW110	00000000	01111111	00001111	001*TTTT	00011111
Latched Output	LO	1,2,6	00000000	110SW110	000KKKKK	00~#EEEE	0001CCCC	001*TTTT	00011111
Registered Output	RO	1,2,6	00000000	110SW110	000KKKKK	00~#EEEE	0100CCCC	001*TTTT	00011111
Bidirectional Transceiver	BT	1,4,6	00000000	110SW110	00000000	01111111	00001111	001*TTTT	001*TTTT
Bidirectional Transceiver with Latched Input	BT&LI	1,2, 4,6	00000000	110SW110	000KKKKK	00~#EEEE	0010CCCC	001*TTTT	001*TTTT
Bidirectional Transceiver with Registered Input	BT&RI	1,2, 3,4,6	00000000	110SW110	000KKKKK	00~#EEEE	1000CCCC	001*TTTT	001*TTTT
Bidirectional Transceiver with Latched Output	BT&LO	1,2, 4,6	00000000	110SW110	000KKKKK	00~#EEEE	0001CCCC	001*TTTT	001*TTTT
Bidirectional Transceiver with Registered Output	BT&RO	1,2, 4,6	00000000	110SW110	000KKKKK	00~#EEEE	0010CCCC	001*TTTT	001*TTTT
Pin side Force 0 or 1	F0, F1	1,5	00000000	11000110	00000000	01111111	00001111	FF0*TTTT	00011111
Array side Force 0 or 1	A0, A1	1,5	00000000	11000110	00000000	01111111	00001111	00001111	AA0*TTTT
Bus Repeater	BR	6	00000000	110SW111	00000000	01111111	00001111	00001111	00011111
Non-Buffered	NB		00000000	11100110	00000000	01111111	00001111	00001111	00011111
No Connect	NC		00000000	11000110	00000000	01111111	00001111	00001111	00011111

Table 7: I/O Configuration Register Contents

Notes:

(1) Tristate Enable (TTTT) source for Input and Output modes is selected as follows: 0 - 12 selects GT0 - GT12, 13 selects Key Match with a Key Value of KKKKK, 14 selects Next Neighbor. 15 is the power on reset "Park" state. * = 1 inverts polarity. Set * = 1, TTTT = 1111 and KKKKK = 00000 for the Input modes when Input Enable (IE) control is not used. Set * = 0, TTTT = 1111 and KKKKK = 00000 for the Output modes when Output Enable ($\overline{OE}$) control is not used.

(2) Clock (CCCC) or Clock Enable (EEEE) sources are selected as follows: 0 - 12 selects GC0 - GC12, 13 selects Key Match with a Key Value of KKKKK, 14 selects Next Neighbor, 15 the reset "Park" state acts as latched state for Latched Input. Set /, ~ and # to 1 to invert polarity.

(3) Additional Pipeline Delay (DDD) is specified in number of clock ticks (1 through 7). Set DDD = 000 when no additional delay is required.

(4) Input Enable and Output Enable may use a different source (i.e., different values for TTTT). When the same source is used, it effectively acts as direction control.

(5) FF = 01 for F0, FF = 10 for F1, AA = 01 for A0 and AA = 10 for A1.

(6) S and W bits can be either 0 or 1. The source for additional static pullup current is disabled when the bit is 0.

Reset Commands

The RapidConfigure interface can also be used to quickly clear the Switch Matrix and reset the I/O Ports to their default state. Refer to the table below for details. When RapidConfigure is used for resetting the I/O Ports the contents of the configuration holding register are set to the default state shown in Table 7, however the contents of the Mode Control Register and the state of the JTAG controller are not affected.

Operation	Control Bus {P/$\overline{S}$, C[1:0]}	IQX320, IQX240B		IQX160		IQX128B	
		Row Add. RA[8:0]	Col. Add. CA[8:0]	Row Add. RA[7:0]	Col. Add. CA[7:0]	Row Add. RA[6:0]	Col. Add. CA[6:0]
Clear All Switch Matrix SRAM Cells (Break Connections)	1 11	000000000	000100000	00000000	00100000	0000000	0100000
Clear All Switch Matrix SRAM Cells (Break Connections) and Set All I/O Ports to Power-on Default Function [Input (IN)]	1 11	000000000	001100000	00000000	01100000	0000000	1100000

Operation	Control Bus {P/$\overline{S}$, C[1:0]}	IQX96		IQX64B	
		Row Add. RA[6:0]	Col. Add. CA[6:0]	Row Add. RA[5:0]	Col. Add. CA[5:0]
Clear All Switch Matrix SRAM Cells (Break Connections)	1 11	0000000	0100000	Not Available(1)	Not Available(1)
Clear All Switch Matrix SRAM Cells (Break Connections) and Set All I/O Ports to Power-on Default Function [Input (IN)]	1 11	0000000	1100000	Not Available(1)	Not Available(1)

Table 8: RapidConfigure Reset Commands

Note:
(1) Due to bondout restrictions, the RCE pin is not available on the IQX96 and IQX64B.

JTAG-based Configuration Controller

In the IQX devices, the I/O attributes and Switch Matrix connections can be programmed using the JTAG serial bus. Additionally, the RapidConfigure Interface, used for quickly changing I/O Port Configurations and Switch Matrix connections, can be enabled or disabled using the JTAG serial bus.

The JTAG-based serial mode is always available for configuration regardless of whether the RapidConfigure mode is enabled or disabled. However proper care must be taken when switching between JTAG and RapidConfigure for configuring the devices. The user must ensure that the RapidConfigure mode is first disabled by using JTAG serial mode to set the RC bit to zero in the Mode Control Register before attempting to change Switch Matrix connections or I/O Port configuration through JTAG.

In most cases, the user does not need to know the details of the JTAG protocol. The I-Cube supplied software will automatically generate the necessary bit stream from a higher-level textual description of the required configuration.

JTAG Interface

The JTAG interface is a serial interface and uses five pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), Test Mode Select (TMS) and Test Reset (TRST*). TCK is used to clock data in and out of TDI and TDO. TMS, in conjunction with TDI implements a state machine that controls the various operations of the JTAG protocol. Data on the TDI and TMS pins is clocked into the IQX device on the rising edge of the TCK signal, while the valid data appears on the TDO pin after the falling edge of TCK. On the IQX devices, TRST* is used to reset both the device and the JTAG controller.

I/O Port Configuration

I/O Port configuration is accomplished by loading the appropriate bit stream into the programming registers present at each I/O Port. The JTAG serial bus is used to load configuration data into the I/O Port programming registers, one I/O Port at a time.

Switch Matrix Configuration

The contents of the SRAM cells controlling Switch Matrix connections can be modified using the JTAG. This is accomplished by loading the configuration data, one word at a time into the SRAM cells in the Switch Matrix.

Mode Control Register Configuration

The IQX device contains a Mode Control Register. Some bits in the register are used to store user flags such as RapidConfigure Enable, and certain non-user flags required for proper functioning of the device. The contents of this register can be changed using the JTAG interface. Refer to Table 10 for details.

Miscellaneous Details

Device Reset

To ensure proper operation, the device reset pin, TRST* must be held low during power up. The reset pulse must be at least 200 ns long. The IQX device is ready for configuration as soon as it comes out of reset. The recommended reset circuitry is shown in Figure 8.

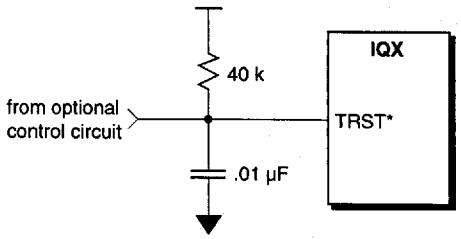


Figure 8: Reset Circuit

When the device is in operation, different functional blocks can be reset using one of following methods. Each method performs a slightly different action as shown in Table 9 below.

Reset Method	Switch Matrix	I/O Ports	I/O Config. Holding Register	JTAG State Machine	RapidConfigure Interface
Pulsing TRST* low	Cleared	Set to Input (IN)	Set to Input (IN)	Reset	Enabled if RCE pin = 1
Shifting in the "Device Reset" instruction using JTAG	Cleared	Set to Input (IN)	Set to Input (IN)	Unchanged	Enabled if RCE pin = 1
Applying "I/O Port and Switch Matrix Reset" instruction using RapidCOnfigure interface	Cleared	Set to Input (IN)	Set to Input (IN)	Unchanged	Stays Enabled
Applying "Switch Matrix Reset" instruction using RapidCOnfigure interface	Cleared	Unchanged	Unchanged	Unchanged	Stays Enabled

Table 9: Device Reset

In any of the above reset methods the edge and level-sensitive flip-flops in the I/O Port buffers are not cleared and will have unknown output values.

Mixed Voltage Operation

There are multiple sources for power on the IQX device. The first one called V_{DD} is a 5V source and is used to power the device core, including the Switch Matrix SRAM cells, I/O Port logic (excluding the I/O buffer driver), I/O control logic, JTAG logic and other circuitry. The I/O buffer drivers are powered by a different source called V_{DD}.PAD. The number of V_{DD}.PAD sources depends on the device. Table 13 shows the number of V_{DD}.PAD sources and the I/O Ports controlled by them. The V_{DD}.PAD pins can be connected to either a 5V or 3V supply. This makes it easy to interface IQX device to 5V and/or 3V logic levels.

Power Pin V_{DD}.X

The IQX devices contain a pin marked V_{DD}.X. In the initial versions of these devices, this pin must be *externally* connected to a 5V supply. In the future versions of the devices that contain an on-chip charge pump, a 6.2V ± 5% Zener diode is required to be connected between the V_{DD}.X pin (cathode) and V_{SS} (anode). To minimize rework, appropriate provisions should be made on the printed circuit boards to handle both possibilities.

Mode Control Register

The IQX device contains a 16-bit Mode Control Register. It stores the RapidConfigure Enable and certain other non-user flags which must be set correctly for the proper functioning of the device. Table 10 shows the bit assignment and their function. A special JTAG instruction is used to write to the Mode Control Register. When this register is written using JTAG the least significant bit (Bit 0) is shifted in first.

Bit #	Name	Default	Description
0	KCNT	0	Uses internal 5-bit counter to provide Key Address
1	RM	*	Used to enable IOB configuration through RapidConfigure interface. Default value equals the RCE pin value on Reset.
2	RC	*	Enables or disables RapidConfigure mode. Default value equals the RCE pin value on Reset.
3	INTERNAL	1	For internal use. Should not be changed by the user.
4	INTERNAL	1	For internal use. Should not be changed by the user.
5	INTERNAL	1	For internal use. Should not be changed by the user.
6	RESERVED	0	For internal use. Should not be changed by the user.
7	INTERNAL	0	For internal use. Should not be changed by the user.
8	INTERNAL	0	For internal use. Should not be changed by the user.
9	INTERNAL	0	For internal use. Should not be changed by the user.
10	INTERNAL	0	For internal use. Should not be changed by the user.
11	KVAL0	0	Terminal count value bit 0 (LSB) when internal counter is used as Key Address
12	KVAL1	0	Terminal count value bit 1 when internal counter is used as Key Address
13	KVAL2	0	Terminal count value bit 1 when internal counter is used as Key Address
14	KVAL3	0	Terminal count value bit 1 when internal counter is used as Key Address
15	KVAL4	0	Terminal count value bit 4 (MSB) when internal counter is used as Key Address

Table 10: Mode Control Register Bit Assignment

In System Configuration Using JTAG-based Configuration Controller

The JTAG-based configuration mode allows the user to initialize the device, configure the I/O Ports, establish connections through the Switch Matrix and set the contents of the Mode Control Register.

Configuring the device using JTAG involves two steps. In the first step the user generates the bit stream. Two different software options - off-line and embedded bit stream generation - are available to accomplish this task. The choice depends on the target application. The second step is the actual downloading of the bit stream into the device. The downloading circuitry can take on different forms, depending on the target application.

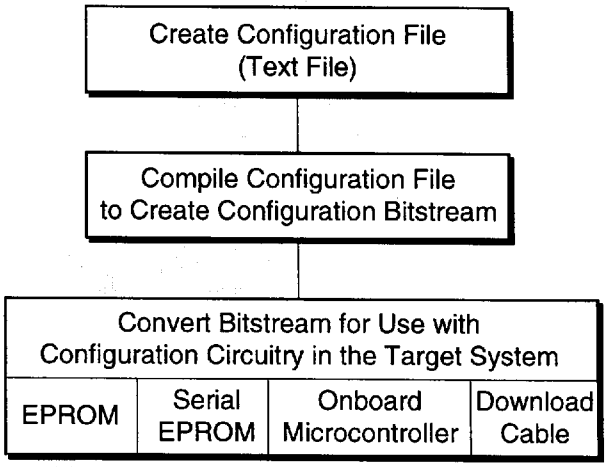


Figure 9: Off-line Bit Stream Generation

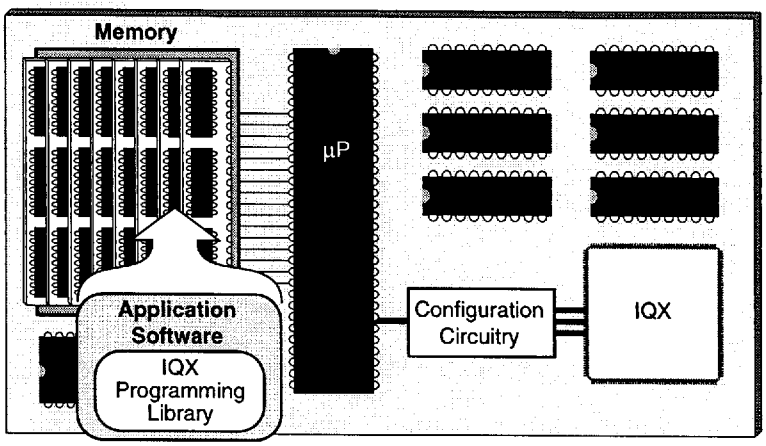


Figure 10: Embedded Bit Stream Generation

Bit Stream Generation

The configuration bit stream can be generated off-line or in-system by an embedded CPU using one of the following methods:

- By using I-Cube Development System Software products IDS100 or IDS 200.
- By using I-Cube's "Programming Library for IQX Devices" software product IDS600, and an embedded processor.
- By user written code based on the information provided in the "IQX Register-level Programming Users Guide".

If the bit stream is generated off-line then, depending on the application, it is either stored in non-volatile memory or directly downloaded from a host processor such as a PC connected to the target hardware.

The software used for off-line generation accepts a text file describing the desired configuration - connections between different I/O Ports, functional attributes of each I/O Port, and settings of certain user flags - and generates a file containing the bit stream.

Bit Stream Downloading

The bit stream can be downloaded into the IQX device using several different hardware schemes. The choice depends on the end application. All these schemes use the standard JTAG protocol and timing. As per the JTAG protocol, the clock signal (TCK) must be supplied externally.

If the target hardware is controlled by a computer such as a PC, the parallel port on the computer can be used to download the bit stream. I-Cube provides a software utility to perform the downloading. Under this scheme, the necessary data for TDI and TMS pins as well as the (software generated) TCK clock signal are sent over the parallel port.

An on-board byte-wide EPROM or E^2PROM, or a serial E^2PROM can be used to store the bit stream. Using minimal external logic, the bit stream stored in one of these devices can be downloaded into the IQX device(s) over the TDI and TMS pins, with the TCK pin used for synchronization. The clock signal for the TCK pin is generated by the external logic.

If the target system has an on-board microcontroller, the bit stream data can be read from memory and downloaded into the IQX device(s) using 3 I/O pins on the microcontroller to generate the required TDI, TMS and TCK signals. For real-time applications, the microcontroller/microprocessor can *generate* the bit stream (using the I-Cube supplied software library or user written code) and then download it into the IQX device in a single operation.

The actual time required to download the configuration bit stream and program a IQX device depends on the device(s) used, the user's specific configuration pattern, and JTAG clock frequency. Table 11 shows the number of JTAG cycles and configuration time required for some typical operations. The size of the memory (number of bytes) required is two (one each for TDI and TMS) times the number of JTAG cycles divided by eight.

Operation	IQX320			IQX240B			IQX160			IQX128B			IQX96			IQX64B		
	JTAG Cycles	Config. Time	Bitstream Size	JTAG Cycles	Config. Time	Bitstream Size	JTAG Cycles	Config. Time	Bitstream Size	JTAG Cycles	Config. Time	Bitstream Size	JTAG Cycles	Config. Time	Bitstream Size	JTAG Cycles	Config. Time	Bitstream Size
JTAG Reset Sequence (TMS = "11111")	5	250 ns	10 bits	5	250 ns	10 bits	5	250 ns	10 bits	5	250 ns	10 bits	5	250 ns	10 bits	5	250 ns	10 bits
Enable or Disable RapidConfigure	42	2.1 µs	84 bits	42	2.1 µs	84 bits	42	2.1 µs	84 bits	42	2.1 µs	84 bits	42	2.1 µs	84 bits	42	2.1 µs	84 bits
Change IOB attributes of ONE I/O Port	76	3.8 µs	152 bits	76	3.8 µs	152 bits	76	3.8 µs	152 bits	76	3.8 µs	152 bits	76	3.8 µs	152 bits	76	3.8 µs	152 bits
Change IOB attributes of ALL I/O Ports	24 K	1.2 ms	6 KB	18 K	0.9 ms	4.5 KB	12 K	0.6 ms	4 KB	10 K	0.5 ms	2.5 KB	8 K	0.4 ms	2 KB	5 K	0.25 ms	1.25 KB
Reset JTAG Controller + Reset ALL I/O Ports + Clear ALL SRAM cells	32	1.6 µs	64 bits	32	1.6 µs	64 bits	32	1.6 µs	64 bits	32	1.6 µs	64 bits	32	1.6 µs	64 bits	32	1.6 µs	64 bits
Connect or disconnect two I/O Ports	346	17.3 µs	692 bits	346	17.3 µs	692 bits	186	9.3 µs	372 bits	186	9.3 µs	372 bits	122	6.1 µs	244 bits	122	6.1 µs	244 bits
Configure Entire Switch Matrix	110 K	5.5 ms	27.5 KB	84 K	4.2 ms	21 KB	30 K	1.5 ms	7.5 KB	24 K	1.2 ms	6 KB	12 K	0.6 ms	3 KB	8 K	0.4 ms	2 KB
Completely Configure the Device (All I/O and All Switch Matrix Connections)	134 K	6.7 ms	34 KB	102 K	5.01 ms	26 KB	42 K	2.1 ms	11 KB	34 K	1.7 ms	9 KB	20 K	1.0 ms	5 KB	13 K	0.65 ms	3.5 KB

Table 11: Number of JTAG Cycles and Configuration Time (using a 20 MHz JTAG Clock)

Configuring Multiple IQX Devices

The JTAG-based controller allows a single device or multiple IQX devices connected in a chain to be configured in a single operation. For multiple device configuration, the pins are connected as shown in Figure 11.

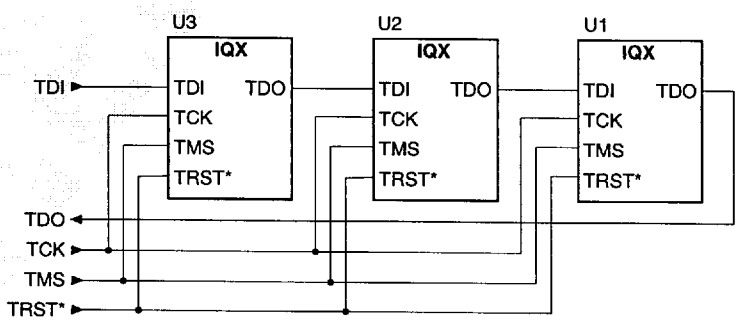


Figure 11: Configuring Multiple IQX Devices

During the initial configuration sequence, the internal controllers on all IQX devices are first brought to their reset state by pulsing the TRST* reset pin low. This is followed by the actual configuration bit stream, which is downloaded into the IQX devices over the TDI and TMS pins.

Pin Summary

IQX320	IQX240B	IQX160	IQX128B	IQX96	IQX64B	DIR	Description
P000 - P259	P000 - P193	P000 - P103	P000 - P083	P000 - P037	P000 - P021	I/O	**Dedicated I/O Ports**
P260 P261 P263 P265 P267	P194 P195 P196 P197 P198	P104 P105 P106 P108 P109	P84 -P88	P38 -P42	P22 - P26	I/O	**Shared I/O Ports** I/O Ports shared with General Tristate Control GT12 - GT8, used for Input Enable (IE) and Output Enable ($\overline{OE}$) Signals.
P268 - P272	P199 - P203	P110 P111 P112 P114 P115	P89 -P93	P43 - P47	P27 -P 31	I/O	**Shared I/O Ports** I/O Ports shared with General Clock Control GC12 - GC8, used for Clock (CLK) and Clock Enable (CKE) Signals.
P273 P275 P277 P279 P281	P204 - P208	P116 P117 P120 P121 P122	P94 -P98	P48 - P52	P32 - P36	I/O	**Shared I/O Ports** I/O Ports shared with Key Control K4 - K0, used for generating Clock (CLK), Clock Enable (CKE), Input Enable (IE) and Output Enable ($\overline{OE}$) signals.
P283 P285 P287 P289	P209 - P212	P125 -P128 P138 P137	P99 - P102 P108 P107	P53 - P56 P62 P61	P37 - P40 P46 P45	I/O	**Shared I/O Ports** I/O Ports shared with General Clock Control GC7 - GC4 for IQX320 and IQX240B and GC7 - GC2 for remaining devices, used for Clock (CLK) and Clock Enable (CKE) Signals.
P291 P293 P295	P213 - P215	P131 - P134	P103 - P106	P57 - P60	P41 - P44	I/O	**Shared I/O Ports** I/O Ports shared with General Tristate Control GT7 - GT5 for IQX320 and IQX240B and GT7 - GT4 for remaining devices, used for Input Enable (IE) and Output Enable ($\overline{OE}$) Signals.
GT4 - GT0	GT4 - GT0	GT3 - GT0	GT3 - GT0	GT3 - GT0	GT3 - GT0	I	**(Dedicated) General Tristate Control Pins** Used for Input Enable (IE) and Output Enable ($\overline{OE}$) Signals.
GC3 - GC0	GC3 - GC0	GC1 - GC0	GC1 - GC0	GC1 - GC0	GC1 - GC0	I	**(Dedicated) General Clock Control Pins** Used for Clock (CLK) and Clock Enable (CKE) signals.
P296 - P304 CA0 - CA8	P216 - P224 CA0 - CA8	P140 - P147 CA0 - CA7	P110 - P116 CA0 - CA6	P78 - P84 CA0 - CA6	P48 - P53 CA0 - CA5	I/O	**Shared I/O Ports** I/O Ports shared with Column Address (CA) Bus

IQX320	IQX240B	IQX160	IQX128B	IQX96	IQX64B	DIR	Description
P306 - P314 RA0 - RA8	P226 - P234 RA0 - RA8	P148 - P155 RA0 - RA7	P117 - P123 RA0 - RA6	P85 - P91 RA0 - RA6	P54 - P59 RA0 - RA5	I/O	**Shared I/O Ports** I/O Ports shared with Row Address (RA) Bus
P315 - P317	P235 - P237	P139 P156 P157	P109 P124 P125	P63 P92 P93	P47 P60 P61	I/O	**Shared I/O Ports** I/O Ports shared with P/$\overline{S}$, C0 AND C1
P318 P319	P238 P239	P158 P159	P126 P127	P94 P95	P62 P63	I/O	**Shared I/O Ports** RapidConfigure Write Enable ($\overline{WE}$) and Write Strobe ($\overline{STROBE}$)
TRST*	TRST*	TRST*	TRST*	TRST*	TRST*	I	**Hardware Reset** Device Reset
TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	TDI, TMS, TCK, TDO	I I O	**JTAG Pins** For downloading the serial configuration bitstream
RCE	RCE	RCE	RCE	RCE	RCE	I	**RapidConfigure Enable Pin** For Enabling RapidConfigure interface after reset
V_{DD}	V_{DD}.PAD1	V_{DD}.PAD1	V_{DD}.PAD1	V_{DD}.PAD1	V_{DD}.PAD1	P	**Power & Ground Pins** Power Pins for Group 1 I/O Buffer Drivers.
	V_{DD}.PAD2	V_{DD}.PAD2	V_{DD}.PAD2	V_{DD}.PAD2	V_{DD}.PAD2	P	Power Pins for Group 2 I/O Buffer Drivers.
	V_{DD}.PAD3					P	Power Pins for Group 3 I/O Buffer Drivers.
	V_{DD}.PAD4					P	Power Pins for Group 4 I/O Buffer Drivers.
V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	P	Power Pins for on-chip circuitry other than I/O Buffer Drivers.
V_{DD}.X	V_{DD}.X	V_{DD}.X	V_{DD}.X	V_{DD}.X	V_{DD}.X	P	Source for Switch Matrix; must be connected to V_{DD} *externally*.
V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	P	Ground Pins.

Table 12: IQX Pin Summary

Supply Voltage	Pins Powered by Supply Voltage					
	IQX320	IQX240B	IQX160	IQX128B	IQX96	IQX64B
V_{DD}	TDI, TMS, TCK, TDO, TRST*, GC0 - GC3, GT0 - GT4, P000:P319	TDI, TMS, TCK, TDO, TRST*, GC0 - GC3, GT0 - GT4	TDI, TMS, TCK, TDO, TRST*, GC0, GC1, GT0 - GT3	TDI, TMS, TCK, TDO, TRST*, GC0, GC1, GT0 - GT3	TDI, TMS, TCK, TDO, TRST*, GC0, GC1, GT0 - GT3	TDI, TMS, TCK, TDO, TRST*, GC0, GC1, GT0 - GT3
V_{DD}.PAD1		P000:P059	P000:P079	P000:P063	P000:P047	P000:P031
V_{DD}.PAD2		P060:P119	P080:P159	P064:P127	P048:P095	P032:P063
V_{DD}.PAD3		P120:P179				
V_{DD}.PAD4		P180:P239				

Table 13: Supply Voltage Source

PAGE(S) INTENTIONALLY BLANK

Electrical Specifications

Absolute Maximum Ratings (1)

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	-0.3 to +7.0	V
V_{DD}.X	Supply Voltage for Switch Matrix	-0.3 to +7.0	V
V_{DD}.PAD	Supply Voltage for I/O Buffer Driver	-0.3 to +7.0	V
V_{IN} (2,3)	Input Voltage	-0.3 to (V_{DD}.PAD + 0.3)	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
I_{OS}	Current per Port Pin	± 100	mA

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply Voltage to Ground	4.75 to 5.25	V
V_{DD}.PAD	Supply Voltage for I/O Buffer Driver (V_{DD}.PAD1 and V_{DD}.PAD2 can operate at different voltages)	4.75 to 5.25 or 2.7 to 3.3	V V
T_A	Operating Temperature	0 to +70	°C

Capacitance (4)

Symbol	Parameter	IQX320		IQX240B		IQX160		IQX128B		IQX96		IQX64B		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C_{IN}	Input Capacitance (JTAG pins)	-	8	-	8	-	8	-	8	-	8	-	8	pF
C_{OUT}	Output Capacitance (TDO pin)	-	8	-	8	-	8	-	8	-	8	-	8	pF
C_{PORT}	I/O Signal Port	-	10	-	10	-	10	-	10	-	10	-	10	pF
C_{CNTL}	Dedicated General Clock and General Tristate Pin Capacitance	-	10	-	10	-	10	-	10	-	10	-	10	pF

Notes:
(1) Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) A maximum overshoot and undershoot of 2V for a maximum duration of 20 ns is acceptable.
(3) For IQX320, V_{DD} and V_{DD}.PAD are connected on the package and are therefore one and the same.
(4) Capacitance measured at 25°C. Sample-tested only.

DC Electrical Specifications

(T_A = 0°C to 70°C, V_{DD} = 5V±5%; V_{DD}.PAD = 5V±5%, or V_{DD}.PAD = 3V±10%) (3)

Symbol	Parameter	Conditions	IQX320, IQX240B		IQX160, IQX128B		IQX96, IQX64B		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	V_{DD}.PAD + 0.3	2.0	V_{DD}.PAD + 0.3	2.0	V_{DD}.PAD + 0.3	V
V_{IL}	Low-Level Input Voltage		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
V_{OH}	High-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 4.75 I_{OH} = - 8 mA	2.4	-	2.4	-	2.4	-	V
	High-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 2.7 I_{OH} = - 4mA	2.4	-	2.4	-	2.4	-	V
V_{OL}	Low-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 4.75 I_{OL} = 16 mA	-	0.4	-	0.4	-	0.4	V
	Low-Level Output Voltage	V_{DD} = Min, V_{DD}.PAD = 2.7 I_{OL} = 16 mA	-	0.4	-	0.4	-	0.4	V
$\|I_{IH}\|$, $\|I_{IL}\|$	Input Leakage Current for I/O ports	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}.PAD	-	5	-	5	-	5	µA
I_{PT}	I/O Port Trickling Current (1)	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}.PAD	-	-25	-	-25	-	-25	µA
$\|I_{OZ}\|$	Tristate Output Off-State Current	V_{DD} = Max, 0 ≤ V_{IN} ≤ V_{DD}.PAD	-	5	-	5	-	5	µA
I_{PU-WK}	Programmed-Weak Additional Pull-Up Current	V_{DD} = Min, V_O = GND	2.5	4.0	2.5	4.0	2.5	4.0	mA
I_{PU-SG}	Programmed-Strong Additional Pull-Up Current	V_{DD} = Min, V_O = GND	9	13.5	9	13.5	9	13.5	mA
I_{OS}	Short Circuit Current (1, 2)	V_{DD} = Max, V_O = GND	-60	-	-60	-	-60	-	mA
I_{DDQ}	Quiescent Power Supply Current	V_{DD} = Max, V_O = GND	-	3.0	-	3.0	-	3.0	mA
Q_{DDD}	Dynamic Power Supply Current per Input (1)	V_{DD} = Min, No Load, Connect one output per input @ 50% duty cycle with all other inputs at GND or V_{DD}	-	0.3	-	0.15	-	0.1	mA/ MHz

Notes:

(1) These parameters are guaranteed but not tested in production.

(2) No more than one output should be tested at a time and the duration of the test should be limited to less than one second.

(3) For IQX320, V_{DD} and V_{DD}.PAD are connected on the package and are therefore one and the same.

AC Electrical Specifications for IQX320 and IQX240B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%; V_{DD}.PAD = 5V±5%, or V_{DD}.PAD = 3V±10%)

(Assume two I/O Ports connected through the Switch Matrix with 35 pF external loading.)

Speed Grade		-7		-10		-12		-15		Units	Ref. Timing Diag.
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
f_{RIO}	Register Input/Output, Clock Frequency (1, 2)		133		100		80		66	MHz	
$t_{W\text{-}RIO}$	Register Input/Output, Clock Pulse Width, Low or High (1, 2)	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RIO}$	Register Input/Output, Data Setup Time to CLK	2.0		2.5		3.0		3.5		ns	1
$t_{H\text{-}RIO}$	Register Input/Output, CLK to Data Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{CO\text{-}RIO}$	Register Input/Output, Clock to Output Data Valid		6.0		7.0		9.0		12.0	ns	
f_{RI}	Register Input, Clock Frequency (1)		100		80		66		50	MHz	
$t_{W\text{-}RI}$	Register Input, Clock Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RI}$	Register Input, Data Setup Time to CLK	2.0		2.5		3.0		3.5		ns	2
$t_{H\text{-}RI}$	Register Input, CLK to Data Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{CO\text{-}RI}$	Register Input, Clock to Output Data Valid		10.0		12.5		15.0		18.0	ns	
f_{RO}	Register Output, Clock Pulse Frequency (1)		133		100		80		66	MHz	
$t_{W\text{-}RO}$	Register Output, Clock Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RO}$	Register Output, Data Setup Time to CLK	4.0		4.5		5.0		5.5		ns	3
$t_{H\text{-}RO}$	Register Output, CLK to Data Hold Time	0.0		0.0		0.0		0.0		ns	
$t_{CO\text{-}RO}$	Register Output, Clock to Output Data Valid		6.0		7.0		9.0		12.0	ns	
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay		7.5		10.0		12.5		15.0	ns	
Δt_{BR}	Additional Delay in Bus Repeater (BR) Mode (1, 2)		0.0		0.0		0.0		0.0	ns	
t_{SK}	Skew Between Output Ports (1)		1.5		1.5		1.5		1.5	ns	
t_{W+}	Input Flow Through Positive Pulse Width (2)	3.5		4.5		6.0		7.5		ns	4
t_{W-}	Input Flow Through Negative Pulse Width (2)	5.5		6.5		8.0		10.0		ns	
R_{DATA}	NRZ Data Rate (1, 2)		180		150		125		100	Mb/s	
$t_{PZH\text{-}IT}$, $t_{PZL\text{-}IT}$	Input Enable (GT) to Data Valid		8.5		10.5		13.0		15.0	ns	5
$t_{PZH\text{-}OT}$, $t_{PZL\text{-}OT}$	Output Enable (GT) to Data Valid		7.0		8.5		10.5		12.5	ns	
$t_{PHZ\text{-}OT}$, $t_{PLZ\text{-}OT}$	Output Enable (GT) to Output at High Z (1)		7.0		8.5		10.5		12.5	ns	6
$t_{W\text{-}LI}$	Latch Input, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LI}$	Latch Input, Data Setup Time to Latch Enable (GC) Trailing Edge	2.0		2.5		3.0		3.5		ns	
$t_{H\text{-}LI}$	Latch Input, Data to Latch Enable (GC) Trailing Edge Hold Time	2.0		2.0		2.0		2.0		ns	7
$t_{CO\text{-}LI}$	Latch Input, Latch Enable (GC) Leading Edge to Data Out Delay		10.0		12.5		15.0		18.0	ns	
$t_{P\text{-}LIT}$	Latch Input, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
$t_{W\text{-}LO}$	Latch Output, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LO}$	Latch Output, Data Setup Time to Latch Enable (GC) Trailing Edge	4.0		4.5		5.0		5.5		ns	
$t_{H\text{-}LO}$	Latch Output, Data to Latch Enable (GC) Trailing Edge Hold Time	0.0		0.0		0.0		0.0		ns	8
$t_{CO\text{-}LO}$	Latch Output, Latch Enable (GC) Leading Edge to Data Out Delay		6.0		7.0		9.0		12.0	ns	
$t_{P\text{-}LOT}$	Latch Output, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
$t_{KW\text{-}RI}$	Register Input, Minimum Pulse Width of KEY as Clock Enable, Low or High	5.0		6.0			7.0		8.0	ns	
$t_{KS\text{-}RI}$	Register Input, Clock Enable (Key) Setup Time to CLK (GC)	2.5		3.0		3.5		4.5		ns	9
$t_{KH\text{-}RI}$	Register Input, CLK (GC) to Clock Enable (Key) Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{KCO\text{-}RI}$	Register Input, Key Clock to Output Data Valid		10.5		13.0		15.5		19.0	ns	

Speed Grade		-7		-10		-12		-15		Units	Ref. Timing Diag.
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{KW-RO}	Register Output, Minimum Pulse Width of KEY as Clock Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-RO}	Register Output, Clock Enable (Key) Setup Time to CLK (GC)	4.5		5.0		5.5		6.5		ns	10
t_{KH-RO}	Register Output, CLK (GC) to Clock Enable (Key) Hold Time	0.0		0.0		0.0		0.0		ns	
t_{KCO-RO}	Register Output, Key Clock to Output Data Valid		6.5		7.5		9.5		13.0	ns	
$t_{KPZH-IT}$ $t_{KPZL-IT}$	Input Enable (Key) to Data Valid		9.0		11.0		13.5		16	ns	11
$t_{KPZH-OT}$ $t_{KPZL-OT}$	Output Enable (Key) to Data Valid		7.5		9.0		11.0		13.5	ns	
$t_{KPHZ-OT}$ $t_{KPLZ-OT}$	Output Enable (Key) to Output at High Z (1)		7.5		9.0		11.0		13.5	ns	12
t_{KW-LI}	Latch Input, Minimum Pulse Width of KEY as Latch Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-LI}	Latch Input, Data Setup Time to Latch Enable (Key) Trailing Edge	2.5		3.0		3.5		4.5		ns	
t_{KH-LI}	Latch Input, Data to Latch Enable (Key) Trailing Edge Hold Time	2.0		2.0		2.0		2.0		ns	13
t_{KCO-LI}	Latch Input, Latch Enable (Key) Leading Edge to Data Out		10.5		13.0		15.5		19.0	ns	
t_{KP-LIT}	Latch Input, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
t_{KW-LO}	Latch Output, Minimum Pulse Width of KEY as Latch Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-LO}	Latch Output, Data Setup Time to Latch Enable (Key) Trailing Edge	4.5		5.0		5.5		6.5		ns	
t_{KH-LO}	Latch Output, Data to Latch Enable (Key) Trailing Edge Hold Time	0.0		0.0		0.0		0.0		ns	14
t_{KCO-LO}	Latch Output, Latch Enable (Key) Leading Edge to Data Out		6.5		7.5		9.5		13.0	ns	
t_{KP-LOT}	Latch Output, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
f_{KCNT}	Key Counter, Input Clock Frequency		80		66		50		40	MHz	
t_{WKCNT}	Key Counter Clock, Pulse Width	5.0		6.0		7.0		8.0		ns	
t_{S_KCKE}	Key Counter, Enable Setup Time to KCLK	2.0		2.5		3.5		4.0		ns	
t_{H_KCKE}	Key Counter, KCLK to Enable Hold Time	0.0		0.0		0.0		0.0		ns	
t_{S_KRST}	Key Counter, Reset Setup Time to KCLK	2.0		2.5		3.5		4.0		ns	
t_{H_KRST}	Key Counter, KCLK to Reset Hold Time	0.0		0.0		0.0		0.0		ns	15
t_{KCLK_OE}	Key Counter, Clock to Output Data Valid or Output High Z		8.0		9.5		11.5		14.5	ns	
t_{KCLK_IE}	Key Counter, Clock to Input Data Valid		9.5		11.5		14.0		17.0	ns	
t_{P_KCLR}	Key Counter, Clear to Output Active / High Z Delay		9.5		11.5		13.5		15.0	ns	
t_{P_KF1F}	Key Counter, Force 0x1F to Output Active / High Z Delay		8.5		10.5		12.5		14.0	ns	
T_{RC}	RapidConnect Strobe Period	20.0		22.5		25.0		30.0		ns	
$t_{W+\text{-}RC}$ $t_{W-\text{-}RC}$	RapidConnect Strobe Pulse Width	5.0		6.0		7.0		8.0		ns	
t_{S-RC}	RapidConnect Address and Data Setup Time to Strobe	4.0		4.5		5.0		5.5		ns	16
t_{H-RC}	RapidConnect Address and Data Hold Time to Strobe	0.0		0.0		0.0		0.0		ns	
t_{P-RC}	RapidConfig Strobe Falling Edge to Data Valid (Make Connection)		13.0		15.0		17.0		20.0	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency		20		20		20		20	MHz	
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20.0		20.0		20.0		20.0		ns	
t_{S-JTAG}	JTAG Setup Time	4.0		4.0		4.0		4.0		ns	17
t_{H-JTAG}	JTAG Hold Time	0.0		0.0		0.0		0.0		ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15.0		15.0		15.0		15.0		ns	

Notes:
(1) These parameters are guaranteed but not tested in production.
(2) The timing parameters are specified for a configuration where an Input Port is driving one Output Port. For configurations where an Input Port is driving two or more Output Ports, the timing parameters are de-rated as shown below. These parameters are guaranteed but not tested in production.

AC Electrical Specifications for IQX160 and IQX128B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%; V_{DD}.PAD = 5V±5%, or V_{DD}.PAD = 3V±10%)

(Assume two I/O Ports connected through the Switch Matrix with 35 pF external loading.)

Speed Grade		-7		-10		-12		-15		Units	Ref. Timing Diag.
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
f_{RIO}	Register Input/Output, Clock Frequency (1, 2)		133		100		80		66	MHz	
$t_{W\text{-}RIO}$	Register Input/Output, Clock Pulse Width, Low or High (1, 2)	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RIO}$	Register Input/Output, Data Setup Time to CLK	2.0		2.5		3.0		3.5		ns	1
$t_{H\text{-}RIO}$	Register Input/Output, CLK to Data Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{CO\text{-}RIO}$	Register Input/Output, Clock to Output Data Valid		6.0		7.0		9.0		12.0	ns	
f_{RI}	Register Input, Clock Frequency (1)		100		80		66		50	MHz	
$t_{W\text{-}RI}$	Register Input, Clock Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RI}$	Register Input, Data Setup Time to CLK	2.0		2.5		3.0		3.5		ns	2
$t_{H\text{-}RI}$	Register Input, CLK to Data Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{CO\text{-}RI}$	Register Input, Clock to Output Data Valid		10.0		12.5		15.0		18.0	ns	
f_{RO}	Register Output, Clock Pulse Frequency (1)		133		100		80		66	MHz	
$t_{W\text{-}RO}$	Register Output, Clock Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RO}$	Register Output, Data Setup Time to CLK	4.0		4.5		5.0		5.5		ns	3
$t_{H\text{-}RO}$	Register Output, CLK to Data Hold Time	0.0		0.0		0.0		0.0		ns	
$t_{CO\text{-}RO}$	Register Output, Clock to Output Data Valid		6.0		7.0		9.0		12.0	ns	
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay		7.5		10.0		12.5		15.0	ns	
Δt_{BR}	Additional Delay in Bus Repeater (BR) Mode (1, 2)		0.0		0.0		0.0		0.0	ns	
t_{SK}	Skew Between Output Ports (1)		1.5		1.5		1.5		1.5	ns	
t_{W+}	Input Flow Through Positive Pulse Width (2)	3.5		4.5		5.0		6.5		ns	4
t_{W-}	Input Flow Through Negative Pulse Width (2)	4.5		5.0		6.0		7.5		ns	
R_{DATA}	NRZ Data Rate (1, 2)		200		180		150		125	Mb/s	
$t_{PZH\text{-}IT}$, $t_{PZL\text{-}IT}$	Input Enable (GT) to Data Valid		8.5		10.5		13.0		15.0	ns	5
$t_{PZH\text{-}OT}$, $t_{PZL\text{-}OT}$	Output Enable (GT) to Data Valid		7.0		8.5		10.5		12.5	ns	
$t_{PHZ\text{-}OT}$, $t_{PLZ\text{-}OT}$	Output Enable (GT) to Output at High Z (1)		7.0		8.5		10.5		12.5	ns	6
$t_{W\text{-}LI}$	Latch Input, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LI}$	Latch Input, Data Setup Time to Latch Enable (GC) Trailing Edge	2.0		2.5		3.0		3.5		ns	
$t_{H\text{-}LI}$	Latch Input, Data to Latch Enable (GC) Trailing Edge Hold Time	2.0		2.0		2.0		2.0		ns	7
$t_{CO\text{-}LI}$	Latch Input, Latch Enable (GC) Leading Edge to Data Out Delay		10.0		12.5		15.0		18.0	ns	
$t_{P\text{-}LIT}$	Latch Input, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
$t_{W\text{-}LO}$	Latch Output, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LO}$	Latch Output, Data Setup Time to Latch Enable (GC) Trailing Edge	4.0		4.5		5.0		5.5		ns	
$t_{H\text{-}LO}$	Latch Output, Data to Latch Enable (GC) Trailing Edge Hold Time	0.0		0.0		0.0		0.0		ns	8
$t_{CO\text{-}LO}$	Latch Output, Latch Enable (GC) Leading Edge to Data Out Delay		6.0		7.0		9.0		12.0	ns	
$t_{P\text{-}LOT}$	Latch Output, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
$t_{KW\text{-}RI}$	Register Input, Minimum Pulse Width of KEY as Clock Enable, Low or High	5.0		6.0			7.0		8.0	ns	
$t_{KS\text{-}RI}$	Register Input, Clock Enable (Key) Setup Time to CLK (GC)	2.5		3.0		3.5		4.5		ns	9
$t_{KH\text{-}RI}$	Register Input, CLK (GC) to Clock Enable (Key) Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{KCO\text{-}RI}$	Register Input, Key Clock to Output Data Valid		10.5		13.0		15.5		19.0	ns	

Speed Grade		-7		-10		-12		-15		Units	Ref. Timing Diag.
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{KW-RO}	Register Output, Minimum Pulse Width of KEY as Clock Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-RO}	Register Output, Clock Enable (Key) Setup Time to CLK (GC)	4.5		5.0		5.5		6.5		ns	10
t_{KH-RO}	Register Output, CLK (GC) to Clock Enable (Key) Hold Time	0.0		0.0		0.0		0.0		ns	
t_{KCO-RO}	Register Output, Key Clock to Output Data Valid		6.5		7.5		9.5		13.0	ns	
$t_{KPZH-IT}$ $t_{KPZL-IT}$	Input Enable (Key) to Data Valid		9.0		11.0		13.5		16	ns	11
$t_{KPZH-OT}$ $t_{KPZL-OT}$	Output Enable (Key) to Data Valid		7.5		9.0		11.0		13.5	ns	
$t_{KPHZ-OT}$ $t_{KPLZ-OT}$	Output Enable (Key) to Output at High Z (1)		7.5		9.0		11.0		13.5	ns	12
t_{KW-LI}	Latch Input, Minimum Pulse Width of KEY as Latch Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-LI}	Latch Input, Data Setup Time to Latch Enable (Key) Trailing Edge	2.5		3.0		3.5		4.5		ns	
t_{KH-LI}	Latch Input, Data to Latch Enable (Key) Trailing Edge Hold Time	2.0		2.0		2.0		2.0		ns	13
t_{KCO-LI}	Latch Input, Latch Enable (Key) Leading Edge to Data Out		10.5		13.0		15.5		19.0	ns	
t_{KP-LIT}	Latch Input, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
t_{KW-LO}	Latch Output, Minimum Pulse Width of KEY as Latch Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-LO}	Latch Output, Data Setup Time to Latch Enable (Key) Trailing Edge	4.5		5.0		5.5		6.5		ns	
t_{KH-LO}	Latch Output, Data to Latch Enable (Key) Trailing Edge Hold Time	0.0		0.0		0.0		0.0		ns	14
t_{KCO-LO}	Latch Output, Latch Enable (Key) Leading Edge to Data Out		6.5		7.5		9.5		13.0	ns	
t_{KP-LOT}	Latch Output, Transparent Mode Propagation Delay		7.5		10.0		12.5		15.0	ns	
f_{KCNT}	Key Counter, Input Clock Frequency		80		66		50		40	MHz	
t_{WKCNT}	Key Counter Clock, Pulse Width	5.0		6.0		7.0		8.0		ns	
t_{S_KCKE}	Key Counter, Enable Setup Time to KCLK	2.0		2.5		3.5		4.0		ns	
t_{H_KCKE}	Key Counter, KCLK to Enable Hold Time	0.0		0.0		0.0		0.0		ns	
t_{S_KRST}	Key Counter, Reset Setup Time to KCLK	2.0		2.5		3.5		4.0		ns	
t_{H_KRST}	Key Counter, KCLK to Reset Hold Time	0.0		0.0		0.0		0.0		ns	15
t_{KCLK_OE}	Key Counter, Clock to Output Data Valid or Output High Z		8.0		9.5		11.5		14.5	ns	
t_{KCLK_IE}	Key Counter, Clock to Input Data Valid		9.5		11.5		14.0		17.0	ns	
t_{P_KCLR}	Key Counter, Clear to Output Active / High Z Delay		9.5		11.5		13.5		15.0	ns	
t_{P_KF1F}	Key Counter, Force 0x1F to Output Active / High Z Delay		8.5		10.5		12.5		14.0	ns	
T_{RC}	RapidConnect Strobe Period	20.0		22.5		25.0		30.0		ns	
t_{W+-RC} t_{W--RC}	RapidConnect Strobe Pulse Width	5.0		6.0		7.0		8.0		ns	
t_{S-RC}	RapidConnect Address and Data Setup Time to Strobe	4.0		4.5		5.0		5.5		ns	16
t_{H-RC}	RapidConnect Address and Data Hold Time to Strobe	0.0		0.0		0.0		0.0		ns	
t_{P-RC}	RapidConfig Strobe Falling Edge to Data Valid (Make Connection)		13.0		15.0		17.0		20.0	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency		20		20		20		20	MHz	
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20.0		20.0		20.0		20.0		ns	
t_{S-JTAG}	JTAG Setup Time	4.0		4.0		4.0		4.0		ns	17
t_{H-JTAG}	JTAG Hold Time	0.0		0.0		0.0		0.0		ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15.0		15.0		15.0		15.0		ns	

Notes:

(1) These parameters are guaranteed but not tested in production.

(2) The timing parameters are specified for a configuration where an Input Port is driving one Output Port. For configurations where an Input Port is driving two or more Output Ports, the timing parameters are de-rated as shown below. These parameters are guaranteed but not tested in production.

AC Electrical Specifications for IQX96 and IQX64B

(T_A = 0°C to 70°C, V_{DD} = 5V±5%; V_{DD}.PAD = 5V±5%, or V_{DD}.PAD = 3V±10%)

(Assume two I/O Ports connected through the Switch Matrix with 35 pF external loading.)

Speed Grade		-6		-10		-12		-15		Units	Ref. Timing Diag.
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
f_{RIO}	Register Input/Output, Clock Frequency (1, 2)		150		100		80		66	MHz	
$t_{W\text{-}RIO}$	Register Input/Output, Clock Pulse Width, Low or High (1, 2)	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RIO}$	Register Input/Output, Data Setup Time to CLK	2.0		2.5		3.0		3.5		ns	1
$t_{H\text{-}RIO}$	Register Input/Output, CLK to Data Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{CO\text{-}RIO}$	Register Input/Output, Clock to Output Data Valid		6.0		7.0		9.0		12.0	ns	
f_{RI}	Register Input, Clock Frequency (1)		100		80		66		50	MHz	
$t_{W\text{-}RI}$	Register Input, Clock Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RI}$	Register Input, Data Setup Time to CLK	2.0		2.5		3.0		3.5		ns	2
$t_{H\text{-}RI}$	Register Input, CLK to Data Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{CO\text{-}RI}$	Register Input, Clock to Output Data Valid		8.0		10.0		12.0		15.0	ns	
f_{RO}	Register Output, Clock Pulse Frequency (1)		133		100		80		66	MHz	
$t_{W\text{-}RO}$	Register Output, Clock Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}RO}$	Register Output, Data Setup Time to CLK	4.0		4.5		5.0		5.5		ns	3
$t_{H\text{-}RO}$	Register Output, CLK to Data Hold Time	1.0		1.0		1.0		1.0		ns	
$t_{CO\text{-}RO}$	Register Output, Clock to Output Data Valid		6.0		7.0		9.0		12.0	ns	
t_{PHL}, t_{PLH}	One Way Signal Propagation Delay		6.0		10.0		12.5		15.0	ns	
Δt_{BR}	Additional Delay in Bus Repeater (BR) Mode (1, 2)		0.0		0.0		0.0		0.0	ns	
t_{SK}	Skew Between Output Ports (1)		1.0		1.0		1.0		1.0	ns	
t_{W+}	Input Flow Through Positive Pulse Width (2)	3.0		4.0		5.0		6.5		ns	4
t_{W-}	Input Flow Through Negative Pulse Width (2)	3.5		4.5		6.0		7.5		ns	
R_{DATA}	NRZ Data Rate (1, 2)		250		200		150		125	Mb/s	
$t_{PZH\text{-}IT}$, $t_{PZL\text{-}IT}$	Input Enable (GT) to Data Valid		6.5		8.5		10.0		12.5	ns	5
$t_{PZH\text{-}OT}$, $t_{PZL\text{-}OT}$	Output Enable (GT) to Data Valid		6.0		8.0		10.0		12.0	ns	
$t_{PHZ\text{-}OT}$, $t_{PLZ\text{-}OT}$	Output Enable (GT) to Output at High Z (1)		6.0		8.0		10.0		12.0	ns	6
$t_{W\text{-}LI}$	Latch Input, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LI}$	Latch Input, Data Setup Time to Latch Enable (GC) Trailing Edge	2.0		2.5		3.0		3.5		ns	
$t_{H\text{-}LI}$	Latch Input, Data to Latch Enable (GC) Trailing Edge Hold Time	2.0		2.0		2.0		2.0		ns	7
$t_{CO\text{-}LI}$	Latch Input, Latch Enable (GC) Leading Edge to Data Out Delay		8.0		10.5		12.5		15.0	ns	
$t_{P\text{-}LIT}$	Latch Input, Transparent Mode Propagation Delay		6.0		10.0		12.5		15.0	ns	
$t_{W\text{-}LO}$	Latch Output, Latch Enable (GC) Pulse Width, Low or High	3.3		4.5		5.5		6.5		ns	
$t_{S\text{-}LO}$	Latch Output, Data Setup Time to Latch Enable (GC) Trailing Edge	4.0		4.5		5.0		5.5		ns	
$t_{H\text{-}LO}$	Latch Output, Data to Latch Enable (GC) Trailing Edge Hold Time	1.0		1.0		1.0		1.0		ns	8
$t_{CO\text{-}LO}$	Latch Output, Latch Enable (GC) Leading Edge to Data Out Delay		6.0		7.0		9.0		12.0	ns	
$t_{P\text{-}LOT}$	Latch Output, Transparent Mode Propagation Delay		6.0		10.0		12.5		15.0	ns	
$t_{KW\text{-}RI}$	Register Input, Minimum Pulse Width of KEY as Clock Enable, Low or High	5.0		6.0			7.0		8.0	ns	
$t_{KS\text{-}RI}$	Register Input, Clock Enable (Key) Setup Time to CLK (GC)	2.5		3.0		3.5		4.5		ns	9
$t_{KH\text{-}RI}$	Register Input, CLK (GC) to Clock Enable (Key) Hold Time	2.0		2.0		2.0		2.0		ns	
$t_{KCO\text{-}RI}$	Register Input, Key Clock to Output Data Valid		8.5		10.5		12.5		15.5	ns	

Speed Grade		-6		-10		-12		-15		Units	Ref. Timing Diag.
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max		
t_{KW-RO}	Register Output, Minimum Pulse Width of KEY as Clock Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-RO}	Register Output, Clock Enable (Key) Setup Time to CLK (GC)	4.5		5.0		5.5		6.5		ns	10
t_{KH-RO}	Register Output, CLK (GC) to Clock Enable (Key) Hold Time	1.0		1.0		1.0		1.0		ns	
t_{KCO-RO}	Register Output, Key Clock to Output Data Valid		6.5		7.5		9.5		13.0	ns	
$t_{KPZH-IT}$ $t_{KPZL-IT}$	Input Enable (Key) to Data Valid		7.0		9.0		10.5		13.0	ns	11
$t_{KPZH-OT}$ $t_{KPZL-OT}$	Output Enable (Key) to Data Valid		6.5		8.5		10.5		12.5	ns	
$t_{KPHZ-OT}$ $t_{KPLZ-OT}$	Output Enable (Key) to Output at High Z (1)		6.5		8.5		10.5		12.5	ns	12
t_{KW-LI}	Latch Input, Minimum Pulse Width of KEY as Latch Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-LI}	Latch Input, Data Setup Time to Latch Enable (Key) Trailing Edge	2.5		3.0		3.5		4.5		ns	
t_{KH-LI}	Latch Input, Data to Latch Enable (Key) Trailing Edge Hold Time	2.0		2.0		2.0		2.0		ns	13
t_{KCO-LI}	Latch Input, Latch Enable (Key) Leading Edge to Data Out		8.5		11.0		13.0		15.5	ns	
t_{KP-LIT}	Latch Input, Transparent Mode Propagation Delay		8.0		10.5		12.5		15.0	ns	
t_{KW-LO}	Latch Output, Minimum Pulse Width of KEY as Latch Enable, Low or High	5.0		6.0		7.0		8.0		ns	
t_{KS-LO}	Latch Output, Data Setup Time to Latch Enable (Key) Trailing Edge	4.5		5.0		5.5		6.5		ns	
t_{KH-LO}	Latch Output, Data to Latch Enable (Key) Trailing Edge Hold Time	1.0		1.0		1.0		1.0		ns	14
t_{KCO-LO}	Latch Output, Latch Enable (Key) Leading Edge to Data Out		6.5		7.5		9.5		13.0	ns	
t_{KP-LOT}	Latch Output, Transparent Mode Propagation Delay		6.0		10.0		12.5		15.0	ns	
f_{KCNT}	Key Counter, Input Clock Frequency		80		66		50		40	MHz	
t_{WKCNT}	Key Counter Clock, Pulse Width	5.0		6.0		7.0		8.0		ns	
t_{S_KCKE}	Key Counter, Enable Setup Time to KCLK	2.0		2.5		3.5		4.0		ns	
t_{H_KCKE}	Key Counter, KCLK to Enable Hold Time	0.0		0.0		0.0		0.0		ns	
t_{S_KRST}	Key Counter, Reset Setup Time to KCLK	2.0		2.5		3.5		4.0		ns	
t_{H_KRST}	Key Counter, KCLK to Reset Hold Time	0.0		0.0		0.0		0.0		ns	15
t_{KCLK_OE}	Key Counter, Clock to Output Data Valid or Output High Z		6.5		8.5		10.5		12.5	ns	
t_{KCLK_IE}	Key Counter, Clock to Input Data Valid		7.0		9.0		10.5		13.0	ns	
t_{P_KCLR}	Key Counter, Clear to Output Active / High Z Delay		6.5		8.5		10.5		12.5	ns	
t_{P_KF1F}	Key Counter, Force 0x1F to Output Active / High Z Delay		6.5		8.5		10.5		12.5	ns	
T_{RC}	RapidConnect Strobe Period	20.0		22.5		25.0		30.0		ns	
$t_{W+\ -RC}$ $t_{W-\ -RC}$	RapidConnect Strobe Pulse Width	5.0		6.0		7.0		8.0		ns	
t_{S-RC}	RapidConnect Address and Data Setup Time to Strobe	4.0		4.5		5.0		5.5		ns	16
t_{H-RC}	RapidConnect Address and Data Hold Time to Strobe	0.0		0.0		0.0		0.0		ns	
t_{P-RC}	RapidConfig Strobe Falling Edge to Data Valid (Make Connection)		13.0		15.0		17.0		20.0	ns	
f_{JTAG}	JTAG Clock (TCK) Frequency		20		20		20		20	MHz	
t_{W-JTAG}	JTAG Clock (TCK) Pulse Width	20.0		20.0		20.0		20.0		ns	
t_{S-JTAG}	JTAG Setup Time	4.0		4.0		4.0		4.0		ns	17
t_{H-JTAG}	JTAG Hold Time	0.0		0.0		0.0		0.0		ns	
t_{P-JTAG}	JTAG Clock to Output Data Valid	15.0		15.0		15.0		15.0		ns	

Notes:

(1) These parameters are guaranteed but not tested in production.

(2) The timing parameters are specified for a configuration where an Input Port is driving one Output Port. For configurations where an Input Port is driving two or more Output Ports, the timing parameters are de-rated as shown below. These parameters are guaranteed but not tested in production.

Parameter De-rating For One-to-Many Connections

Symbol	Parameter	IQX320		IQX240B		IQX160		IQX128B		IQX96		IQX64B		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
CN_{MAX}	Maximum Number of Connections Per Input	-	32	-	32	-	64	-	64	-	64	-	64	
Δt_{PD}	Increase in t_{PD} for Every Additional Output Port Connected to an Input Port	-	0.35	-	0.35	-	0.25	-	0.25	-	0.25	-	0.25	ns
Δt_W	Increase in tw+ and tw- for Every Additional Output Port Connected to an Input Port	-	100	-	100	-	80	-	80	-	80	-	80	ps
Δf	Decrease in Maximum Operating Frequency Every Additional Output Port Connected to an Input Port	-	1	-	1	-	0.75	-	0.75	-	0.75	-	0.75	MHz

Test Circuit and Timing Diagrams

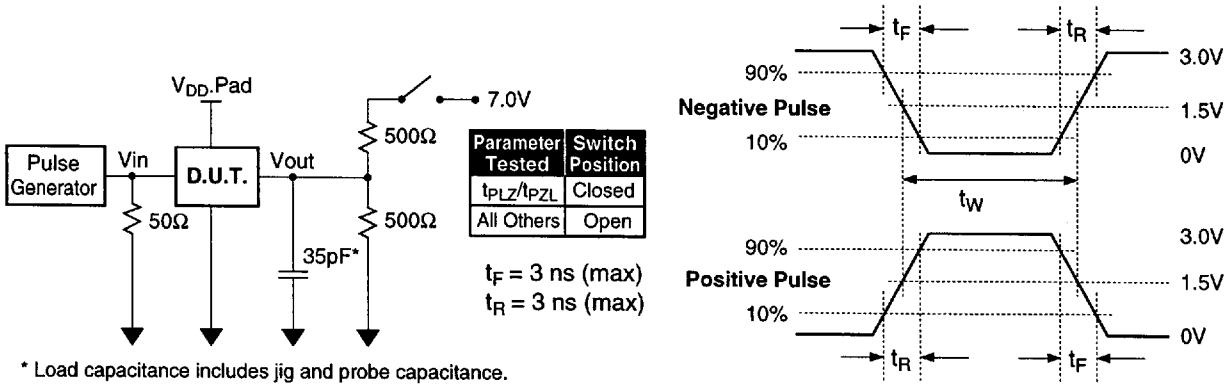
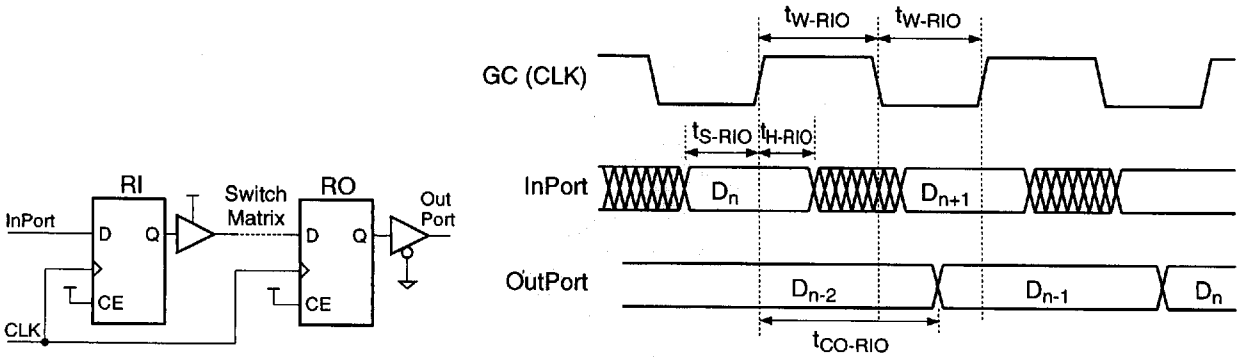
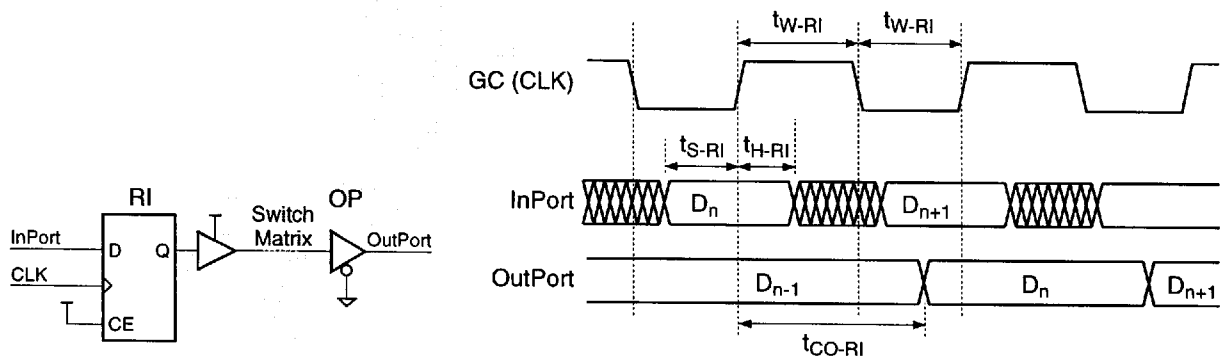


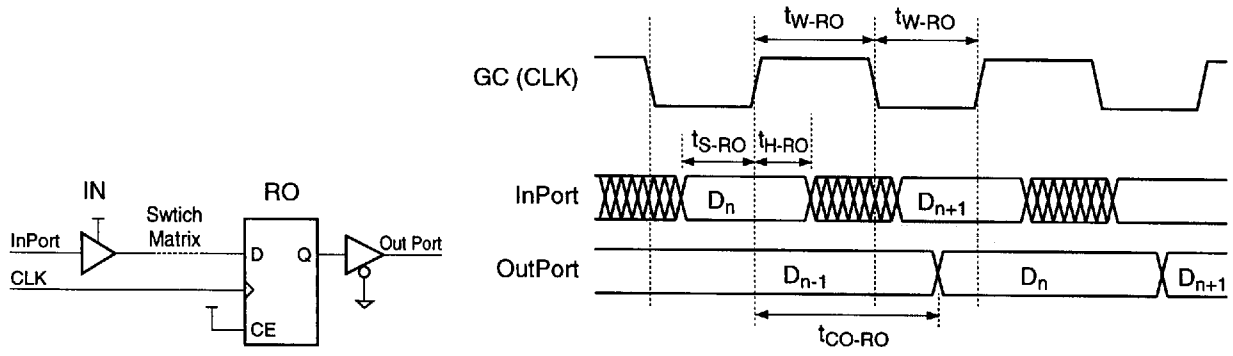
Figure 15: Test Circuit and Waveform Definition



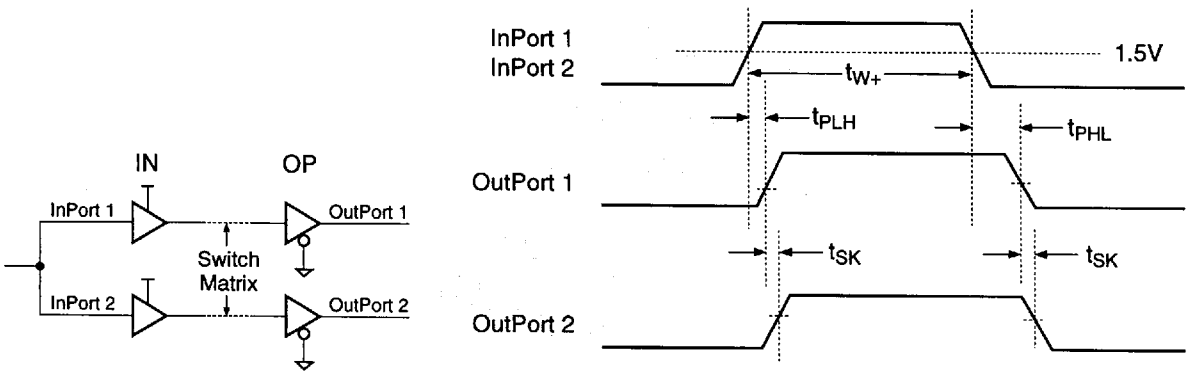
Timing Diagram 1:Registered Input and Registered Output Mode Timing (ICLK and OCLK are Synchronized)



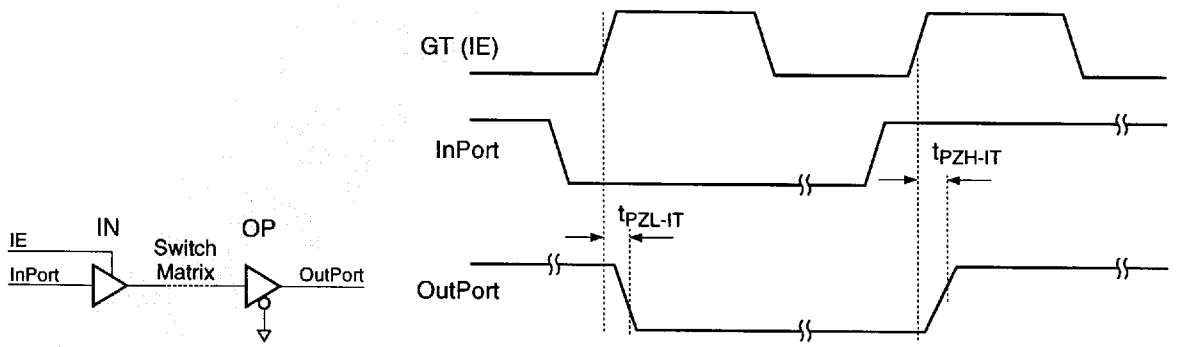
Timing Diagram 2:Registered Input Mode Timing



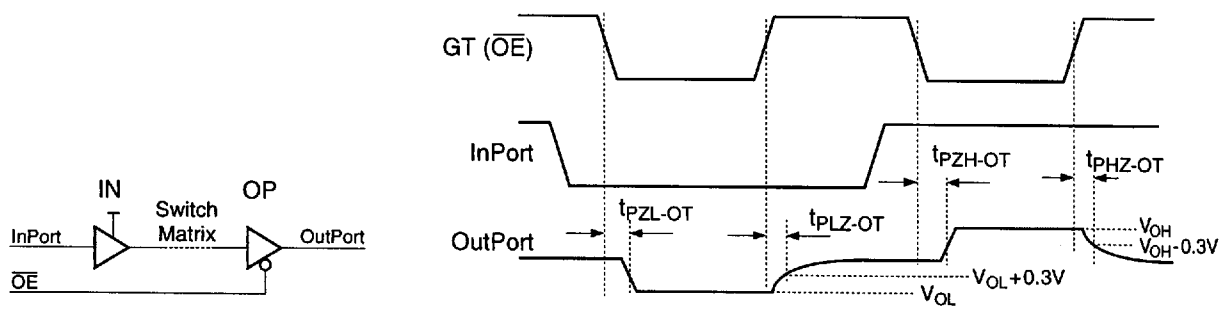
Timing Diagram 3: Registered Output Mode Timing



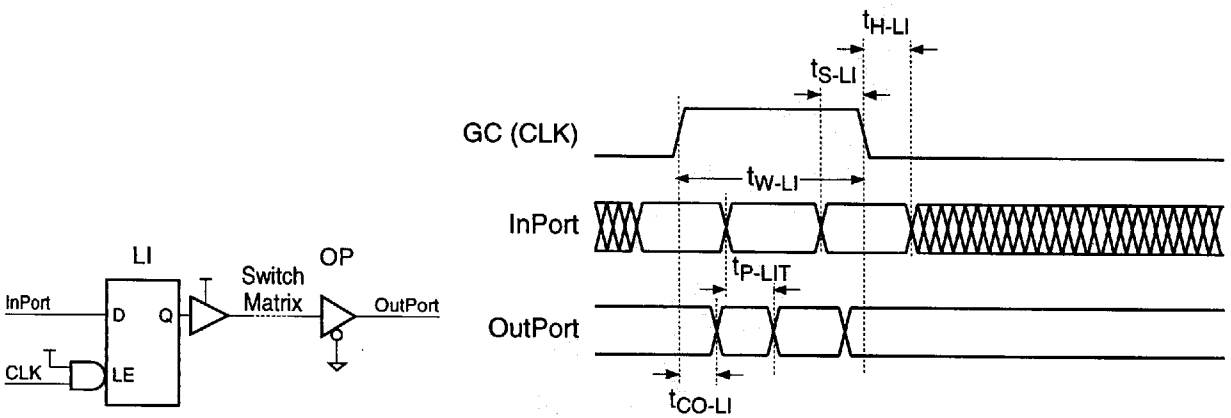
Timing Diagram 4: I/O Port Timing (Flow–through Mode)



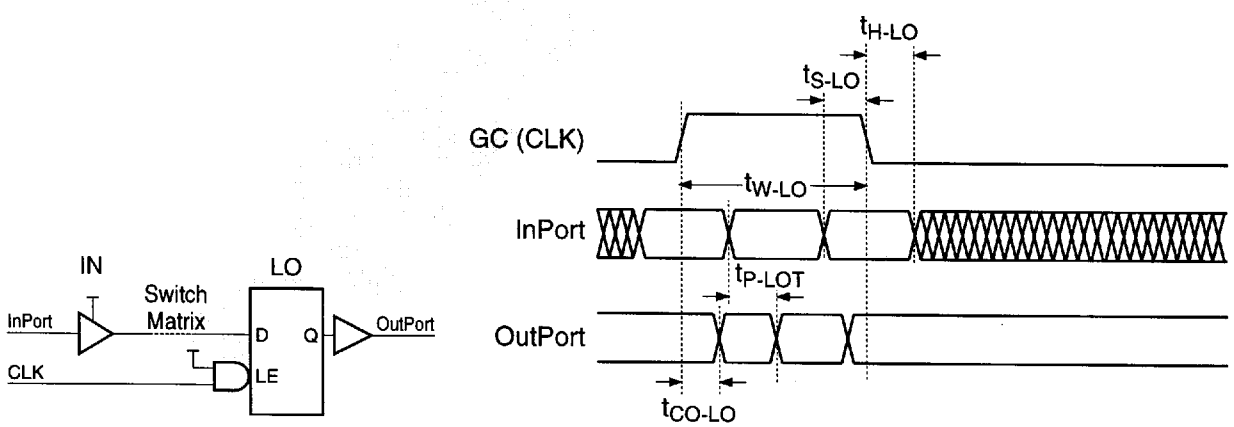
Timing Diagram 5:Input Enable Timing (Flow–through Mode)



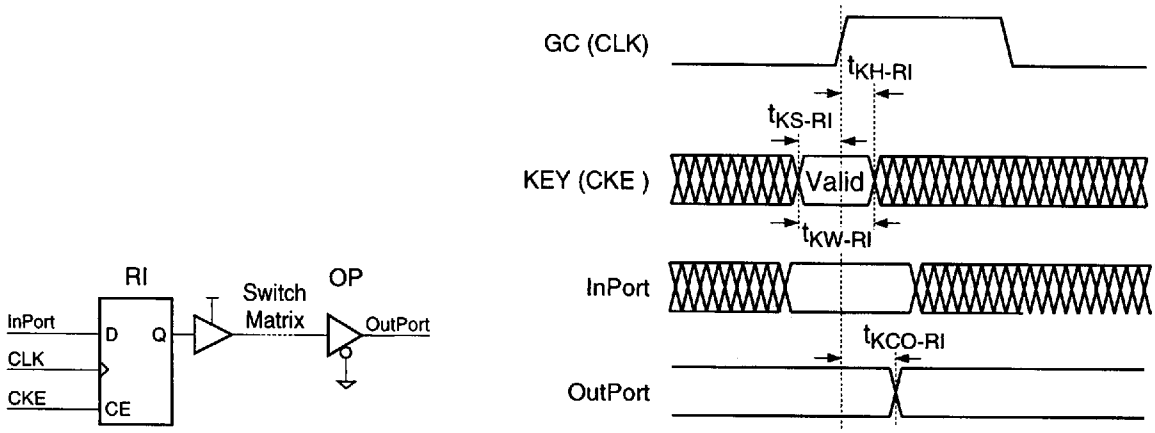
Timing Diagram 6:Output Enable Timing (Flow–through Mode)



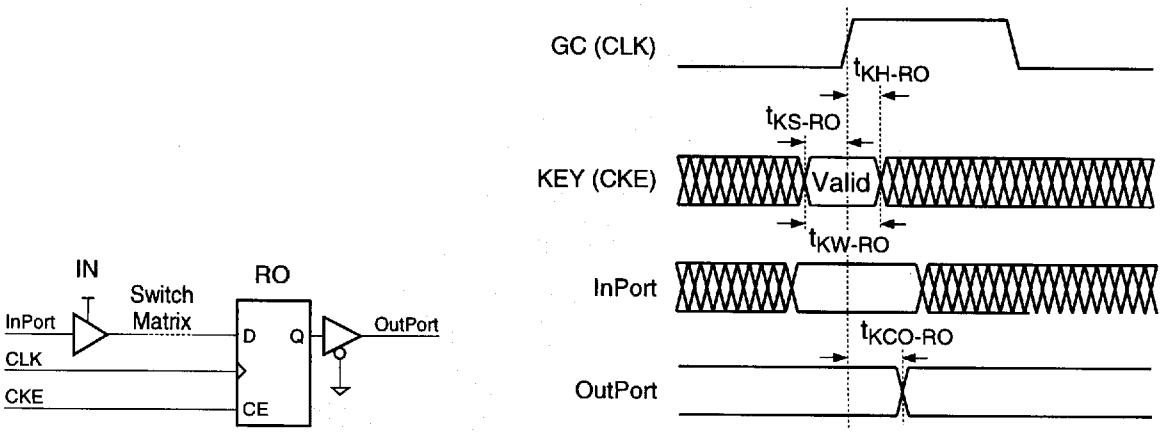
Timing Diagram 7: Latched Input Mode Timing



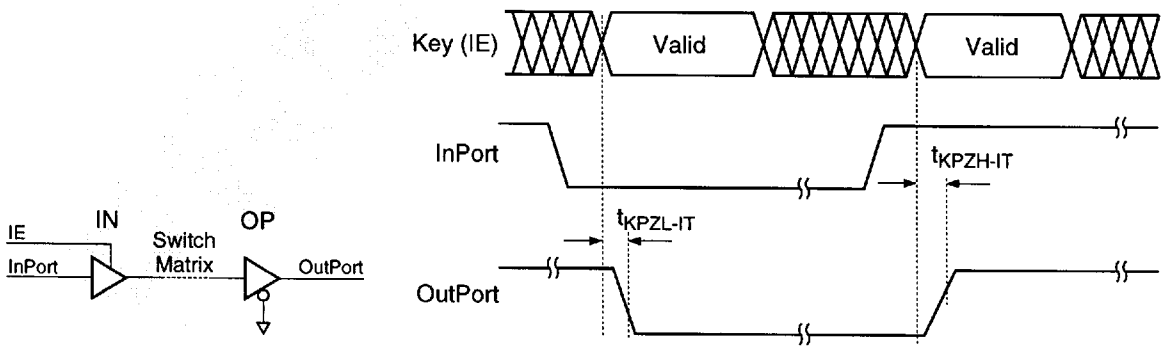
Timing Diagram 8: Latched Output Mode Timing



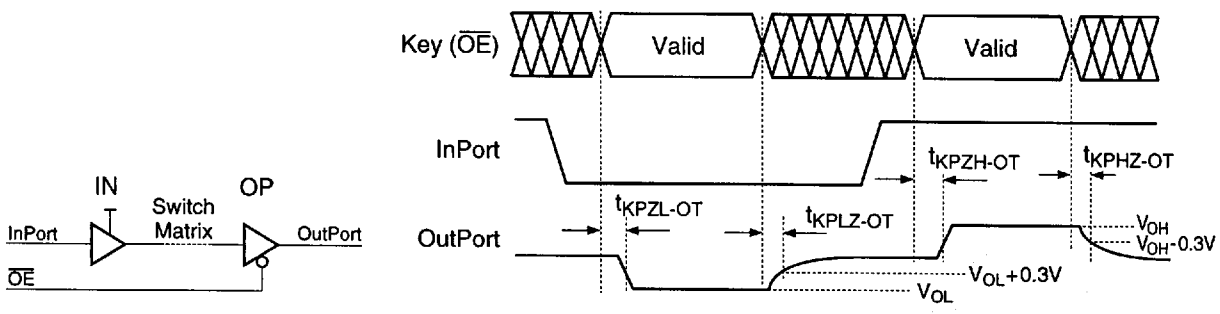
Timing Diagram 9:Key Timing for Register Input, Clock Enable (CKE)



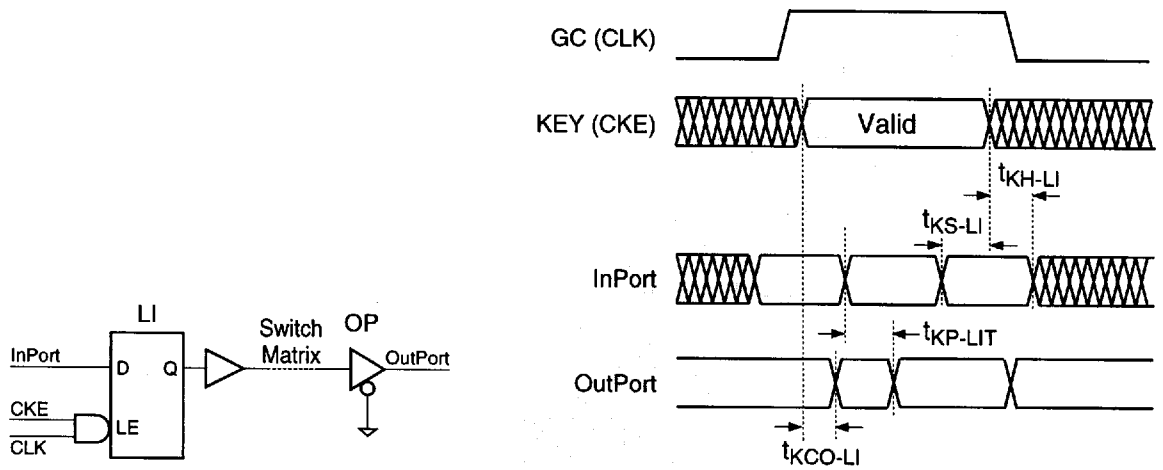
Timing Diagram 10:Key Timing for Register Output, Clock Enable (CKE)



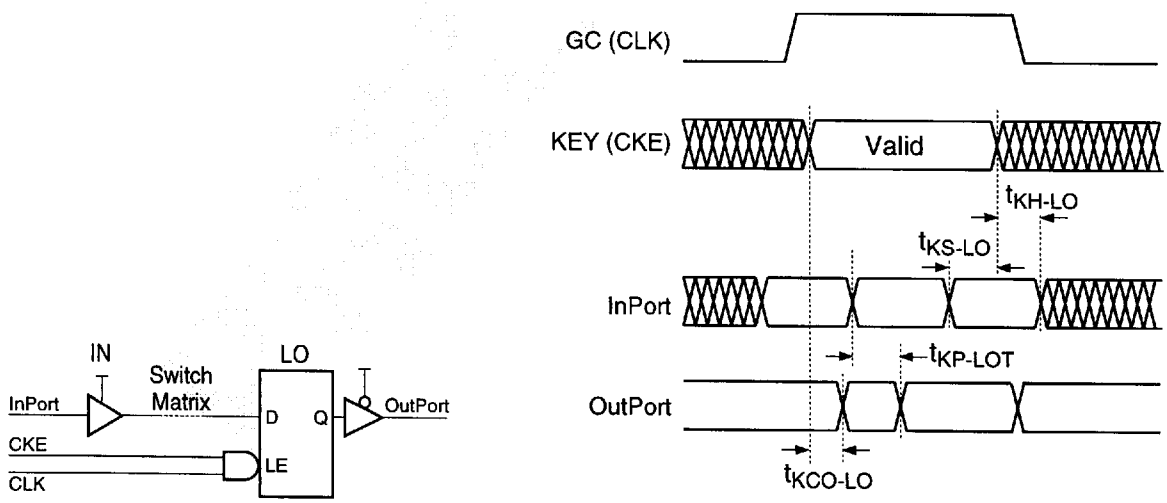
Timing Diagram 11:Key Timing for Input Enable



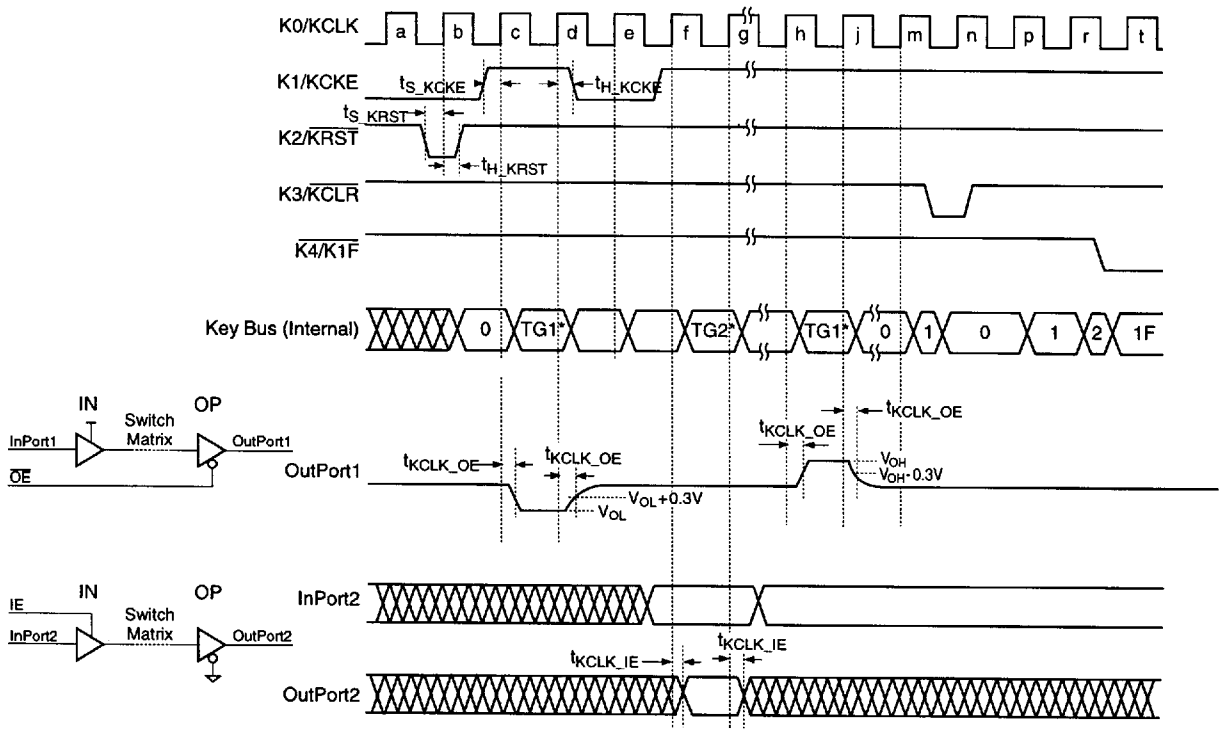
Timing Diagram 12:Key Timing for Output Enable



Timing Diagram 13:Key Timing for Latch Input, Enable (CKE)

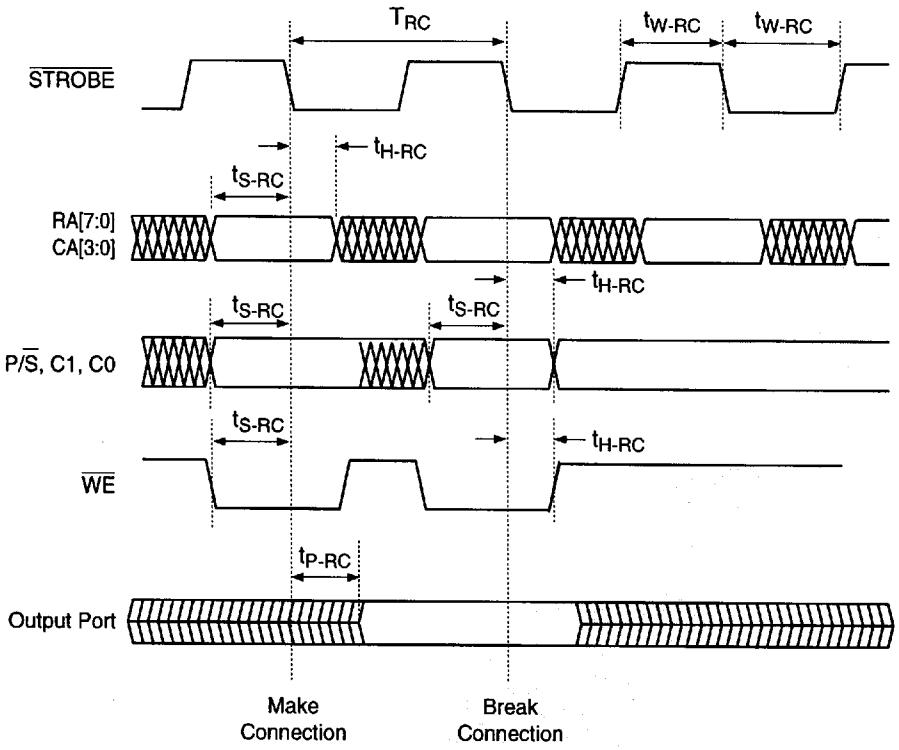


Timing Diagram 14:Key Timing for Latch Output, Enable (CKE)

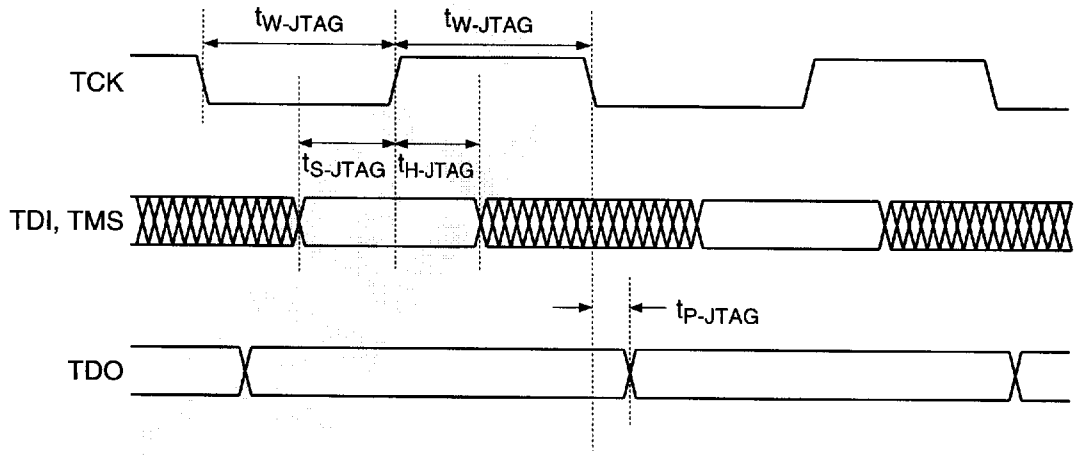


* TG1 and TG2 are the 5-bit tag values programmed in the I/O Ports OutPort1 and InPort2 respectively.

Timing Diagram 15: Key Counter Timing



Timing Diagram 16: RapidConfigure Timing



Timing Diagram 17: JTAG Timing

Pinout

IQX320 [PPGA/391L] Package Pinout by Name

Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#
GC0	K6	P041	D20	P091	L29	P141	AD30	P191	AL21	P241	AL7	P291GT7	T6	V_{DD}	AR3
GC1	J5	P042	A21	P092	K32	P142	AH32	P192	AM20	P242	AJ7	P292	P2	V_{DD}	AR31
GC2	G5	P043	F20	P093	L31	P143	AE31	P193	AK20	P243	AP2	P293/GT6	R5	V_{DD}	AR35
GC3	J7	P044	C21	P094	K34	P144	AK34	P194	AP20	P244	AH6	P294	M2	V_{DD}	AR7
GT0	C33	P045	E21	P095	M30	P145	AE29	P195	AL19	P245	AM4	P295/GT5	R7	V_{DD}	C35
GT1	G31	P046	B22	P096	L33	P146	AK32	P196	AN19	P246	AK2	P296/CA0	N3	V_{DD}	E1
GT2	AN3	P047	G21	P097	N29	P147	AF32	P197	AJ19	P247	AM2	P297/CA1	P4	V_{DD}	G35
GT3	AJ5	P048	B24	P098	M32	P148	AL33	P198	AR19	P248	AJ3	P298/CA2	K2	V_{DD}	J1
GT4	H6	P049	D22	P099	N31	P149	AF30	P199	AM18	P249	AK4	P299/CA3	P6	V_{DD}	L35
P000	F8	P050	C23	P100	M34	P150	AM34	P200	AP18	P250	AG7	P300/CA4	L3	V_{DD}	N1
P001	B6	P051	F22	P101	P30	P151	AG31	P201	AK18	P251	AL3	P301/CA5	N5	V_{DD}	R35
P002	C7	P052	B26	P102	N33	P152	AL31	P202	AN17	P252	AG5	P302/CA6	H2	V_{SS}	AA35
P003	G9	P053	E23	P103	P32	P153	AG29	P203	AL17	P253	AH4	P303/CA7	N7	V_{SS}	AC1
P004	E9	P054	C25	P104	P34	P154	AK30	P204	AR17	P254	AH2	P304/CA8	J3	V_{SS}	AE35
P005	B8	P055	G23	P105	R29	P155	AH30	P205	AJ17	P255	AF6	P305	M4	V_{SS}	AJ35
P006	C9	P056	B2 8	P106	R33	P156	AN33	P206	AP16	P256	AG3	P306/RA0	G3	V_{SS}	AL1
P007	F10	P057	D24	P107	R31	P157	AJ31	P207	AM16	P257	AE7	P307/RA1	M6	V_{SS}	AR1
P008	D10	P058	C27	P108	T32	P158	AL29	P208	AR15	P258	AF4	P308/RA2	H4	V_{SS}	AR25
P009	G11	P059	F24	P109	T30	P159	AJ29	P209	AK16	P259	AE5	P309/RA3	L5	V_{SS}	AR29
P010	B10	P060	C29	P110	T34	P160	AK28	P210	AN15	P260/GT12	AF2	P310/RA4	F2	V_{SS}	AR33
P011	E11	P061	E25	P111	U31	P161	AP34	P211	AL15	P261/GT11	AD6	P311/RA5	L7	V_{SS}	AR5
P012	C11	P062	D28	P112	U33	P162	AP30	P212	AP14	P262	AE3	P312/RA6	F4	V_{SS}	AR9
P013	F12	P063	G25	P113	U29	P163	AM32	P213	AJ15	P263/GT10	AC7	P313/RA7	E3	V_{SS}	B2
P014	D12	P064	B30	P114	U35	P164	AN29	P214	AP12	P264	AD4	P314/RA8	D2	V_{SS}	J35
P015	G13	P065	D26	P115	V32	P165	AP32	P215	AM14	P265/GT9	AC5	P315/ P/$\overline{S}$	E5	V_{SS}	L1
P016	B12	P066	D30	P116	V34	P166	AJ27	P216	AN13	P266	AD2	P316/C0	F6	V_{SS}	N35
P017	E13	P067	F26	P117	V30	P167	AM30	P217	AK14	P267/GT8	AB6	P317/C1	C3	V_{SS}	R1
P018	C13	P068	C31	P118	W33	P168	AL27	P218	AP10	P268/GC12	AC3	P318/$\overline{WE}$	E7	V_{SS}	A11
P019	F14	P069	E27	P119	W31	P169	AN31	P219	AL13	P269/GC11	AB4	P319/$\overline{STROBE}$	G7	V_{SS}	A23
P020	B14	P070	B32	P120	W35	P170	AP28	P220	AN11	P270/GC10	AB2	TCK	C5	V_{SS}	A27
P021	D14	P071	G27	P121	W29	P171	AM28	P221	AJ13	P271/GC9	AA7	TDI	D4	V_{SS}	A3
P022	C15	P072	E31	P122	Y34	P172	AN27	P222	AP8	P272/GC8	AA3	TDO	D6	V_{SS}	A31
P023	G15	P073	F28	P123	Y32	P173	AK26	P223	AM12	P273/K4	AA5	TMS	B4	V_{SS}	A35
P024	A15	P074	F30	P124	AA33	P174	AM26	P224	AN9	P274	Y4	TRST*	D8	V_{SS}	A7
P025	E15	P075	E29	P125	Y30	P175	AJ25	P225	AK12	P275/K3	Y6	V_{DD}	A13	V_{SS}	AG1
P026	D16	P076	G29	P126	AB34	P176	AP26	P226	AN7	P276	Y2	V_{DD}	A25	V_{SS}	AN35
P027	F16	P077	B34	P127	AA31	P177	AL25	P227	AL11	P277/K2	W5	V_{DD}	A29	V_{SS}	AR13
P028	B16	P078	H30	P128	AD34	P178	AN25	P228	AM8	P278	W3	V_{DD}	A33	V_{SS}	C1
P029	E17	P079	D32	P129	AA29	P179	AK24	P229	AJ11	P279/K1	W7	V_{DD}	A5	V_{SS}	E35
P030	C17	P080	F34	P130	AC33	P180	AM24	P230	AP6	P280	W1	V_{DD}	A9	V_{SS}	G1
P031	G17	P081	D34	P131	AB32	P181	AJ23	P231	AM10	P281/K0	V4	V_{DD}	AA1	V_{DD}-X	K4
P032	A17	P082	G33	P132	AF34	P182	AP24	P232	AM6	P282	V2	V_{DD}	AC35		
P033	D18	P083	F32	P133	AB30	P183	AL23	P233	AK10	P283/GC7	V6	V_{DD}	AE1		
P034	B18	P084	J29	P134	AE33	P184	AN23	P234	AN5	P284	U3	V_{DD}	AG35		
P035	F18	P085	E33	P135	AC31	P185	AK22	P235	AL9	P285/GC6	U5	V_{DD}	AJ1		
P036	C19	P086	J31	P136	AH34	P186	AP22	P236	AP4	P286	U1	V_{DD}	AL35		
P037	E19	P087	H32	P137	AC29	P187	AM22	P237	AJ9	P287/GC5	U7	V_{DD}	AN1		
P038	A19	P088	H34	P138	AG33	P188	AN21	P238	AL5	P288	T2	V_{DD}	AR11		
P039	G19	P089	K30	P139	AD32	P189	AJ21	P239	AK8	P289/GC4	T4	V_{DD}	AR23		
P040	B20	P090	J33	P140	AJ33	P190	AR21	P240	AK6	P290	R3	V_{DD}	AR27		

IQX320 [PPGA/391L] Package Pinout by Location

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
A3	V_{SS}	C33	GT0	F28	P073	M2	P294	W5	P277/K2	AF6	P255	AK30	P154	AN25	P178
A5	V_{DD}	C35	V_{DD}	F30	P074	M4	P305	W7	P279/K1	AF30	P149	AK32	P146	AN27	P172
A7	V_{SS}	D2	P314/RA8	F32	P083	M6	P307/RA1	W29	P121	AF32	P147	AK34	P144	AN29	P164
A9	V_{DD}	D4	TDI	F34	P080	M30	P095	W31	P119	AF34	P132	AL1	V_{SS}	AN31	P169
A11	V_{SS}	D6	TDO	G1	V_{SS}	M32	P098	W33	P118	AG1	V_{SS}	AL3	P251	AN33	P156
A13	V_{DD}	D8	TRST*	G3	P306/RA0	M34	P100	W35	P120	AG3	P256	AL5	P238	AN35	V_{SS}
A15	P024	D10	P008	G5	GC2	N1	V_{DD}	Y2	P276	AG5	P252	AL7	P241	AP2	P243
A17	P032	D12	P014	G7	P319/STROBE	N3	P296/CA0	Y4	P274	AG7	P250	AL9	P235	AP4	P236
A19	P038	D14	P021	G9	P003	N5	P301/CA5	Y6	P275/K3	AG29	P153	AL11	P227	AP6	P230
A21	P042	D16	P026	G11	P009	N7	P303/CA7	Y30	P125	AG31	P151	AL13	P219	AP8	P222
A23	V_{SS}	D18	P033	G13	P015	N29	P097	Y32	P123	AG33	P138	AL15	P211	AP10	P218
A25	V_{DD}	D20	P041	G15	P023	N31	P099	Y34	P122	AG35	V_{DD}	AL17	P203	AP12	P214
A27	V_{SS}	D22	P049	G17	P031	N33	P102	AA1	V_{DD}	AH2	P254	AL19	P195	AP14	P212
A29	V_{DD}	D24	P057	G19	P039	N35	V_{SS}	AA3	P272/GC8	AH4	P253	AL21	P191	AP16	P206
A31	V_{SS}	D26	P065	G21	P047	P2	P292	AA5	P273/K4	AH6	P244	AL23	P183	AP18	P200
A33	V_{DD}	D28	P062	G23	P055	P4	P297/CA1	AA7	P271/GC9	AH30	P155	AL25	P177	AP20	P194
A35	V_{SS}	D30	P066	G25	P063	P6	P299/CA3	AA29	P129	AH32	P142	AL27	P168	AP22	P186
B2	RCE	D32	P079	G27	P071	P30	P101	AA31	P127	AH34	P136	AL29	P158	AP24	P182
B4	TMS	D34	P081	G29	P076	P32	P103	AA33	P124	AJ1	V_{DD}	AL31	P152	AP26	P176
B6	P001	E1	V_{DD}	G31	GT1	P34	P104	AA35	V_{SS}	AJ3	P248	AL33	P148	AP28	P170
B8	P005	E3	P313/RA7	G33	P082	R1	V_{SS}	AB2	P270/GC10	AJ5	GT3	AL35	V_{DD}	AP30	P162
B10	P010	E5	P315 / P/$\overline{S}$	G35	V_{DD}	R3	P290	AB4	P269/GC11	AJ7	P242	AM2	P247	AP32	P165
B12	P016	E7	P318/$\overline{WE}$	H2	P302/CA6	R5	P293/GT6	AB6	P267/GT8	AJ9	P237	AM4	P245	AP34	P161
B14	P020	E9	P004	H4	P308/RA2	R7	P295/GT5	AB30	P133	AJ11	P229	AM6	P232	AR1	V_{SS}
B16	P028	E11	P011	H6	GT4	R29	P105	AB32	P131	AJ13	P221	AM8	P228	AR3	V_{DD}
B18	P034	E13	P017	H30	P078	R31	P107	AB34	P126	AJ15	P213	AM10	P231	AR5	V_{SS}
B20	P040	E15	P025	H32	P087	R33	P106	AC1	V_{SS}	AJ17	P205	AM12	P223	AR7	V_{DD}
B22	P046	E17	P029	H34	P088	R35	V_{DD}	AC3	P268/GC12	AJ19	P197	AM14	P215	AR9	V_{SS}
B24	P048	E19	P037	J1	V_{DD}	T2	P288	AC5	P265/GT9	AJ21	P189	AM16	P207	AR11	V_{DD}
B26	P052	E21	P045	J3	P304/CA8	T4	P289/GC4	AC7	P263/GT10	AJ23	P181	AM18	P199	AR13	V_{SS}
B28	P056	E23	P053	J5	GC1	T6	P291/GT7	AC29	P137	AJ25	P175	AM20	P192	AR15	P208
B30	P064	E25	P061	J7	GC3	T30	P109	AC31	P135	AJ27	P166	AM22	P187	AR17	P204
B32	P070	E27	P069	J29	P084	T32	P108	AC33	P130	AJ29	P159	AM24	P180	AR19	P198
B34	P077	E29	P075	J31	P086	T34	P110	AC35	V_{DD}	AJ31	P157	AM26	P174	AR21	P190
C1	V_{SS}	E31	P072	J33	P090	U1	P286	AD2	P266	AJ33	P140	AM28	P171	AR23	V_{DD}
C3	P317/C1	E33	P085	J35	V_{SS}	U3	P284	AD4	P264	AJ35	V_{SS}	AM30	P167	AR25	V_{SS}
C5	TCK	E35	V_{SS}	K2	P298/CA2	U5	P285/GC6	AD6	P261/GT11	AK2	P246	AM32	P163	AR27	V_{DD}
C7	P002	F2	P310/RA4	K4	V_{DD}.X	U7	P287/GC5	AD30	P141	AK4	P249	AM34	P150	AR29	V_{SS}
C9	P006	F4	P312/RA6	K6	GC0	U29	P113	AD32	P139	AK6	P240	AN1	V_{DD}	AR31	V_{DD}
C11	P012	F6	P316/C0	K30	P089	U31	P111	AD34	P128	AK8	P239	AN3	GT2	AR33	V_{SS}
C13	P018	F8	P000	K32	P092	U33	P112	AE1	V_{DD}	AK10	P233	AN5	P234	AR35	V_{DD}
C15	P022	F10	P007	K34	P094	U35	P114	AE3	P262	AK12	P225	AN7	P226		
C17	P030	F12	P013	L1	V_{SS}	V2	P282	AE5	P259	AK14	P217	AN9	P224		
C19	P036	F14	P019	L3	P300/CA4	V4	P281/K0	AE7	P257	AK16	P209	AN11	P220		
C21	P044	F16	P027	L5	P309/RA3	V6	P283/GC7	AE29	P145	AK18	P201	AN13	P216		
C23	P050	F18	P035	L7	P311/RA5	V30	P117	AE31	P143	AK20	P193	AN15	P210		
C25	P054	F20	P043	L29	P091	V32	P115	AE33	P134	AK22	P185	AN17	P202		
C27	P058	F22	P051	L31	P093	V34	P116	AE35	V_{SS}	AK24	P179	AN19	P196		
C29	P060	F24	P059	L33	P096	W1	P280	AF2	P260/GT12	AK26	P173	AN21	P188		
C31	P068	F26	P067	L35	V_{DD}	W3	P278	AF4	P258	AK28	P160	AN23	P184		

IQX320 [PBGA/416L] Package Pinout by Name

Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#
GC0	E2	P043	A18	P095	G26	P147	AA26	P199	AF15	P251	AB3	P303/CA7	H3	V_{DD}	P1
GC1	D1	P044	E15	P096	K24	P148	W23	P200	AD14	P252	X5	P304/CA8	L5	V_{DD}	P26
GC2	C3	P045	B18	P097	G27	P149	AA25	P201	AE15	P253	AC1	P305	G1	V_{DD}	P27
GC3	E3	P046	C16	P098	K25	P150	Y23	P202	AB14	P254	X4	P306/RA0	K4	V_{DD}	R2
GT0	D22	P047	C18	P099	H25	P151	AC27	P203	AE14	P255	AB2	P307/RA1	G2	V_{DD}	R3
GT1	E24	P048	D16	P100	L23	P152	U23	P204	AC14	P256	W5	P308/RA2	K5	V_{DD}	V1
GT2	AB5	P049	B19	P101	H26	P153	AB25	P205	AE13	P257	AA3	P309/RA3	G3	V_{DD}	W2
GT3	AA5	P050	E16	P102	L24	P154	AA24	P206	AD13	P258	W4	P310/RA4	J4	V_{DD}	W27
GT4	D2	P051	C19	P103	J25	P155	AC26	P207	AE12	P259	AA2	P311/RA5	F2	V_{DD}	X1
P000	D5	P052	C17	P104	L25	P156	AA23	P208	AC13	P260/GT12	V5	P312/RA6	J5	V_{DD}	X24
P001	E14	P053	B20	P105	J26	P157	AD25	P209	AE11	P261/GT11	Y3	P313/RA7	H5	V_{SS}	A6
P002	E6	P054	D17	P106	M25	P158	AB23	P210	AB13	P262	V4	P314/RA8	G4	V_{SS}	A11
P003	E11	P055	C20	P107	J27	P159	AC25	P211	AF10	P263/GT10	Y2	P315/ P/$\overline{S}$	G5	V_{SS}	A12
P004	D6	P056	E17	P108	M23	P160	AB22	P212	AC12	P264	V3	P316/C0	F4	V_{SS}	A16
P005	E9	P057	A21	P109	K26	P161	AD24	P213	AE10	P265/GT9	Y1	P317/C1	F5	V_{SS}	A17
P006	E8	P058	D18	P110	M24	P162	AC23	P214	AB12	P266	U5	P318/$\overline{WE}$	E5	V_{SS}	A20
P007	C6	P059	B21	P111	L26	P163	AE25	P215	AD10	P267/GT8	X3	P319/$\overline{STROBE}$	D3	V_{SS}	A22
P008	E7	P060	D19	P112	N23	P164	AB21	P216	AC11	P268/GC12	U4	TCK	A4	V_{SS}	AA1
P009	B6	P061	C21	P113	M26	P165	AE24	P217	AE9	P269/GC11	X2	TDI	B3	V_{SS}	AA27
P010	D7	P062	E18	P114	N24	P166	AC22	P218	AC10	P270/GC10	U3	TDO	C5	V_{SS}	AB24
P011	C7	P063	B22	P115	N27	P167	AD23	P219	AD9	P271/GC9	W3	TMS	B4	V_{SS}	AB26
P012	E10	P064	E19	P116	P25	P168	AC21	P220	AC9	P272/GC8	T5	TRST*	B5	V_{SS}	AC4
P013	B7	P065	C22	P117	N26	P169	AF24	P221	AE8	P273/K4	W1	V_{DD}	A5	V_{SS}	AC24
P014	D9	P066	D20	P118	P23	P170	AB20	P222	AB11	P274	T4	V_{DD}	A8	V_{SS}	AD26
P015	A7	P067	B23	P119	R26	P171	AE23	P223	AD8	P275/K3	V2	V_{DD}	A10	V_{SS}	AE3
P016	D8	P068	E20	P120	P24	P172	AC20	P224	AC8	P276	T3	V_{DD}	A14	V_{SS}	AF6
P017	C8	P069	A24	P121	R27	P173	AD22	P225	AF7	P277/K2	U2	V_{DD}	A19	V_{SS}	AF8
P018	D10	P070	D21	P122	R25	P174	AB19	P226	AB10	P278	R4	V_{DD}	A23	V_{SS}	AF11
P019	B8	P071	C23	P123	T26	P175	AE22	P227	AE7	P279/K1	T2	V_{DD}	AB1	V_{SS}	AF12
P020	C10	P072	E21	P124	R24	P176	AC19	P228	AB8	P280	R5	V_{DD}	AB27	V_{SS}	AF16
P021	C9	P073	B24	P125	U26	P177	AD21	P229	AD7	P281/K0	R1	V_{DD}	AD11	V_{SS}	AF17
P022	D11	P074	E22	P126	R23	P178	AB18	P230	AB9	P282	P3	V_{DD}	AD12	V_{SS}	AF22
P023	B9	P075	C25	P127	V27	P179	AE21	P231	AE6	P283/GC7	P2	V_{DD}	AD15	V_{SS}	B25
P024	C11	P076	C24	P128	T25	P180	AC18	P232	AB7	P284	P4	V_{DD}	AF5	V_{SS}	C2
P025	A9	P077	D25	P129	V26	P181	AF21	P233	AD6	P285/GC6	N1	V_{DD}	AF9	RCE	C4
P026	E12	P078	E23	P130	T24	P182	AD18	P234	AC7	P286	N3	V_{DD}	AF13	V_{SS}	D4
P027	B10	P079	C26	P131	V25	P183	AD20	P235	AE5	P287/GC5	M2	V_{DD}	AF14	V_{SS}	D23
P028	D12	P080	F24	P132	T23	P184	AB17	P236	AC6	P288	P5	V_{DD}	AF18	V_{SS}	D24
P029	B11	P081	D26	P133	W26	P185	AE20	P237	AF4	P289/GC4	L2	V_{DD}	AF20	V_{SS}	E4
P030	C12	P082	G23	P134	U25	P186	AC17	P238	AB6	P290	N4	V_{DD}	AF23	V_{SS}	F1
P031	B12	P083	E25	P135	W25	P187	AD19	P239	AD5	P291GT7	K1	V_{DD}	B13	V_{SS}	F27
P032	E13	P084	G24	P136	U24	P188	AD17	P240	AC5	P292	M3	V_{DD}	B15	V_{SS}	H1
P033	A13	P085	D27	P137	X26	P189	AE19	P241	AE4	P293/GT6	K2	V_{DD}	C13	V_{SS}	L1
P034	D13	P086	H23	P138	V24	P190	AB16	P242	AD3	P294	L3	V_{DD}	E1	V_{SS}	L27
P035	B14	P087	E26	P139	X25	P191	AF19	P243	AD4	P295/GT5	K3	V_{DD}	E27	V_{SS}	M1
P036	C14	P088	H24	P140	W24	P192	AC16	P244	AB4	P296/CA0	N5	V_{DD}	F23	V_{SS}	M27
P037	A15	P089	F25	P141	Y27	P193	AE18	P245	AC3	P297/CA1	J2	V_{DD}	H27	V_{SS}	T1
P038	D14	P090	J23	P142	V23	P194	AD16	P246	AA4	P298/CA2	M5	V_{DD}	H4	V_{SS}	T27
P039	B16	P091	F26	P143	Y26	P195	AE17	P247	AD2	P299/CA3	J3	V_{DD}	J1	V_{SS}	U1
P040	C15	P092	J24	P144	Y24	P196	AC15	P248	Y5	P300/CA4	M4	V_{DD}	K27	V_{SS}	U27
P041	B17	P093	G25	P145	Y25	P197	AE16	P249	AC2	P301/CA5	H2	V_{DD}	N2	V_{SS}	X27
P042	D15	P094	K23	P146	X23	P198	AB15	P250	Y4	P302/CA6	L4	V_{DD}	N25	V_{DD}.X	F3

IQX320 [PBGA/416L] Package Pinout by Location

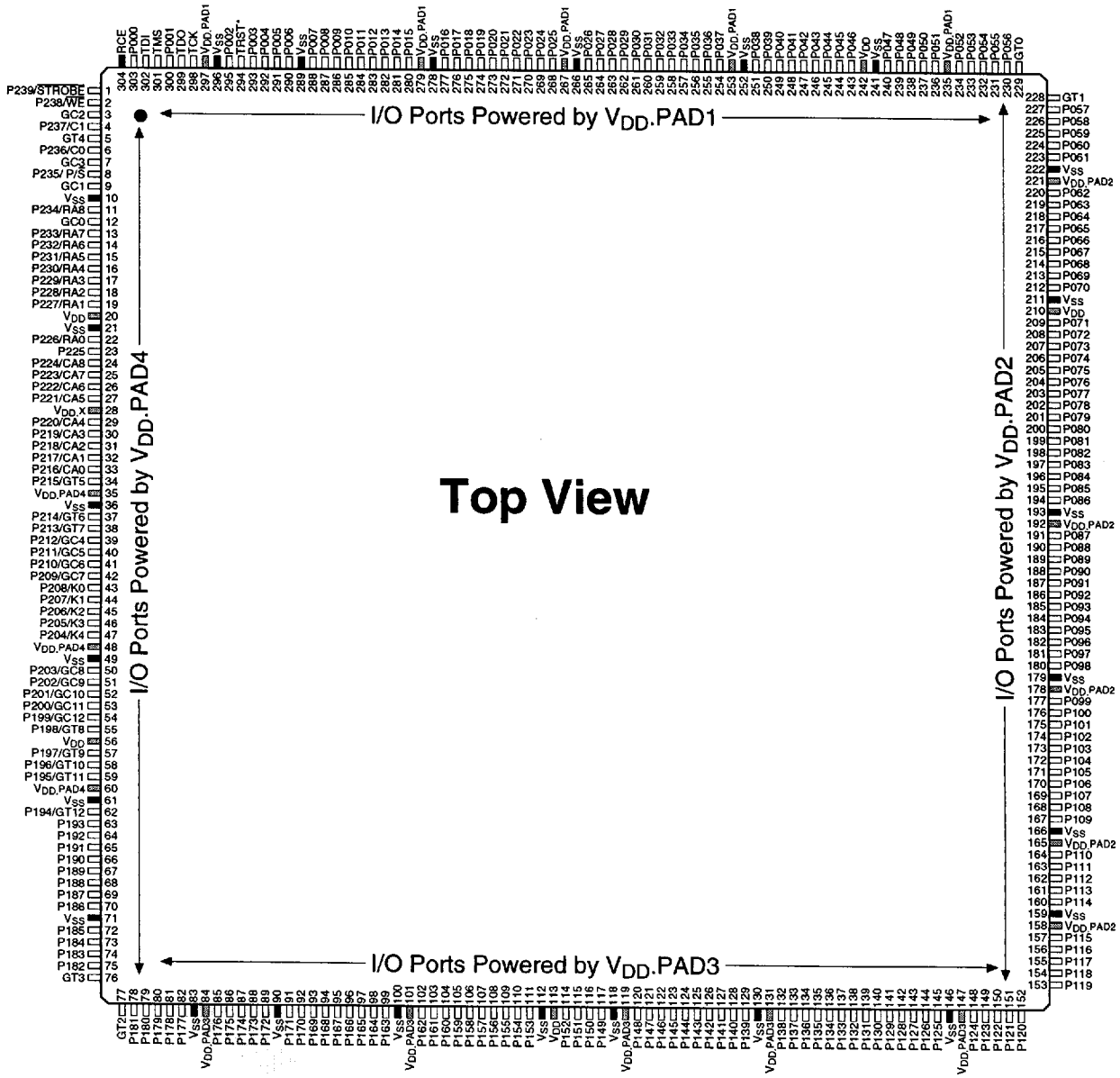
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
A4	TCK	C11	P024	E11	P003	J24	P092	P27	V_{DD}	X3	P267/GT8	AB26	V_{SS}	AD26	V_{SS}
A5	V_{DD}	C12	P030	E12	P026	J25	P103	R1	P281/K0	X4	P254	AB27	V_{DD}	AE3	V_{SS}
A6	V_{SS}	C13	V_{DD}	E13	P032	J26	P105	R2	V_{DD}	X5	P252	AC1	P253	AE4	P241
A7	P015	C14	P036	E14	P001	J27	P107	R3	V_{DD}	X23	P146	AC2	P249	AE5	P235
A8	V_{DD}	C15	P040	E15	P044	K1	P291/GT7	R4	P278	X24	V_{DD}	AC3	P245	AE6	P231
A9	P025	C16	P046	E16	P050	K2	P293/GT6	R5	P280	X25	P139	AC4	V_{SS}	AE7	P227
A10	V_{DD}	C17	P052	E17	P056	K3	P295/GT5	R23	P126	X26	P137	AC5	P240	AE8	P221
A11	V_{SS}	C18	P047	E18	P062	K4	P306/RA0	R24	P124	X27	V_{SS}	AC6	P236	AE9	P217
A12	V_{SS}	C19	P051	E19	P064	K5	P308/RA2	R25	P122	Y1	P265/GT9	AC7	P234	AE10	P213
A13	P033	C20	P055	E20	P068	K23	P094	R26	P119	Y2	P263/GT10	AC8	P224	AE11	P209
A14	V_{DD}	C21	P061	E21	P072	K24	P096	R27	P121	Y3	P261/GT11	AC9	P220	AE12	P207
A15	P037	C22	P065	E22	P074	K25	P098	T1	V_{SS}	Y4	P250	AC10	P218	AE13	P205
A16	V_{SS}	C23	P071	E23	P078	K26	P109	T2	P279/K1	Y5	P248	AC11	P216	AE14	P203
A17	V_{SS}	C24	P076	E24	GT1	K27	V_{DD}	T3	P276	Y23	P150	AC12	P212	AE15	P201
A18	P043	C25	P075	E25	P083	L1	V_{SS}	T4	P274	Y24	P144	AC13	P208	AE16	P197
A19	V_{DD}	C26	P079	E26	P087	L2	P289/GC4	T5	P272/GC8	Y25	P145	AC14	P204	AE17	P195
A20	V_{SS}	D1	GC1	E27	V_{DD}	L3	P294	T23	P132	Y26	P143	AC15	P196	AE18	P193
A21	P057	D2	GT4	F1	V_{SS}	L4	P302/CA6	T24	P130	Y27	P141	AC16	P192	AE19	P189
A22	V_{SS}	D3	P319/$\overline{STROBE}$	F2	P311/RA5	L5	P304/CA8	T25	P128	AA1	V_{SS}	AC17	P186	AE20	P185
A23	V_{DD}	D4	V_{SS}	F3	V_{DD}.X	L23	P100	T26	P123	AA2	P259	AC18	P180	AE21	P179
A24	P069	D5	P000	F4	P316/C0	L24	P102	T27	V_{SS}	AA3	P257	AC19	P176	AE22	P175
B3	TDI	D6	P004	F5	P317/C1	L25	P104	U1	V_{SS}	AA4	P246	AC20	P172	AE23	P171
B4	TMS	D7	P010	F23	V_{DD}	L26	P111	U2	P277/K2	AA5	GT3	AC21	P168	AE24	P165
B5	TRST*	D8	P016	F24	P080	L27	V_{SS}	U3	P270/GC10	AA23	P156	AC22	P166	AE25	P163
B6	P009	D9	P014	F25	P089	M1	V_{SS}	U4	P268/GC12	AA24	P154	AC23	P162	AF4	P237
B7	P013	D10	P018	F26	P091	M2	P287/GC5	U5	P266	AA25	P149	AC24	V_{SS}	AF5	V_{DD}
B8	P019	D11	P022	F27	V_{SS}	M3	P292	U23	P152	AA26	P147	AC25	P159	AF6	V_{SS}
B9	P023	D12	P028	G1	P305	M4	P300/CA4	U24	P136	AA27	V_{SS}	AC26	P155	AF7	P225
B10	P027	D13	P034	G2	P307/RA1	M5	P298/CA2	U25	P134	AB1	V_{DD}	AC27	P151	AF8	V_{SS}
B11	P029	D14	P038	G3	P309/RA3	M23	P108	U26	P125	AB2	P255	AD2	P247	AF9	V_{DD}
B12	P031	D15	P042	G4	P314/RA8	M24	P110	U27	V_{SS}	AB3	P251	AD3	P242	AF10	P211
B13	V_{DD}	D16	P048	G5	P315/ P/$\overline{S}$	M25	P106	V1	V_{DD}	AB4	P244	AD4	P243	AF11	V_{SS}
B14	P035	D17	P054	G23	P082	M26	P113	V2	P275/K3	AB5	GT2	AD5	P239	AF12	V_{SS}
B15	V_{DD}	D18	P058	G24	P084	M27	V_{SS}	V3	P264	AB6	P238	AD6	P233	AF13	V_{DD}
B16	P039	D19	P060	G25	P093	N1	P285/GC6	V4	P262	AB7	P232	AD7	P229	AF14	V_{DD}
B17	P041	D20	P066	G26	P095	N2	V_{DD}	V5	P260/GT12	AB8	P228	AD8	P223	AF15	P199
B18	P045	D21	P070	G27	P097	N3	P286	V23	P142	AB9	P230	AD9	P219	AF16	V_{SS}
B19	P049	D22	GT0	H1	V_{SS}	N4	P290	V24	P138	AB10	P226	AD10	P215	AF17	V_{SS}
B20	P053	D23	V_{SS}	H2	P301/CA5	N5	P296/CA0	V25	P131	AB11	P222	AD11	V_{DD}	AF18	V_{DD}
B21	P059	D24	V_{SS}	H3	P303/CA7	N23	P112	V26	P129	AB12	P214	AD12	V_{DD}	AF19	P191
B22	P063	D25	P077	H4	V_{DD}	N24	P114	V27	P127	AB13	P210	AD13	P206	AF20	V_{DD}
B23	P067	D26	P081	H5	P313/RA7	N25	V_{DD}	W1	P273/K4	AB14	P202	AD14	P200	AF21	P181
B24	P073	D27	P085	H23	P086	N26	P117	W2	V_{DD}	AB15	P198	AD15	V_{DD}	AF22	V_{SS}
B25	V_{SS}	E1	V_{DD}	H24	P088	N27	P115	W3	P271/GC9	AB16	P190	AD16	P194	AF23	V_{DD}
C2	V_{SS}	E2	GC0	H25	P099	P1	V_{DD}	W4	P258	AB17	P184	AD17	P188	AF24	P169
C3	GC2	E3	GC3	H26	P101	P2	P283/GC7	W5	P256	AB18	P178	AD18	P182		
C4	RCE	E4	V_{SS}	H27	V_{DD}	P3	P282	W23	P148	AB19	P174	AD19	P187		
C5	TDO	E5	P318/$\overline{WE}$	J1	V_{DD}	P4	P284	W24	P140	AB20	P170	AD20	P183		
C6	P007	E6	P002	J2	P297/CA1	P5	P288	W25	P135	AB21	P164	AD21	P177		
C7	P011	E7	P008	J3	P299/CA3	P23	P118	W26	P133	AB22	P160	AD22	P173		
C8	P017	E8	P006	J4	P310/RA4	P24	P120	W27	V_{DD}	AB23	P158	AD23	P167		
C9	P021	E9	P005	J5	P312/RA6	P25	P116	X1	V_{DD}	AB24	V_{SS}	AD24	P161		
C10	P020	E10	P012	J23	P090	P26	V_{DD}	X2	P269/GC11	AB25	P153	AD25	P157		

PAGE(S) INTENTIONALLY BLANK

IQX240B [MQUAD®/304L] Package Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	P239/ $\overline{\text{STROBE}}$	39	P212/GC4	77	GT2	115	P151	153	P119	191	P087	229	GT0	267	V_{DD}. PAD1
2	P238/ $\overline{\text{WE}}$	40	P211/GC5	78	P181	116	P150	154	P118	192	V_{DD}. PAD2	230	P056	268	P025
3	GC2	41	P210/GC6	79	P180	117	P149	155	P117	193	V_{SS}	231	P055	269	P024
4	P237/C1	42	P209/GC7	80	P179	118	V_{SS}	156	P116	194	P086	232	P054	270	P023
5	GT4	43	P208/K0	81	P178	119	V_{DD}.PAD3	157	P115	195	P085	233	P053	271	P022
6	P236/C0	44	P207/K1	82	P177	120	P148	158	V_{DD}. PAD2	196	P084	234	P052	272	P021
7	GC3	45	P206/K2	83	V_{SS}	121	P147	159	V_{SS}	197	P083	235	V_{DD}. PAD1	273	P020
8	P235/ P/$\overline{S}$	46	P205/K3	84	V_{DD}.PAD3	122	P146	160	P114	198	P082	236	P051	274	P019
9	GC1	47	P204/K4	85	P176	123	P145	161	P113	199	P081	237	P050	275	P018
10	V_{SS}	48	V_{DD}.PAD4	86	P175	124	P144	162	P112	200	P080	238	P049	276	P017
11	P234/RA8	49	V_{SS}	87	P174	125	P143	163	P111	201	P079	239	P048	277	P016
12	GC0	50	P203/GC8	88	P173	126	P142	164	P110	202	P078	240	P047	278	V_{SS}
13	P233/RA7	51	P202/GC9	89	P172	127	P141	165	V_{DD}. PAD2	203	P077	241	V_{SS}	279	V_{DD}. PAD1
14	P232/RA6	52	P201/GC10	90	V_{SS}	128	P140	166	V_{SS}	204	P076	242	V_{DD}	280	P015
15	P231/RA5	53	P200/GC11	91	P171	129	P139	167	P109	205	P075	243	P046	281	P014
16	P230/RA4	54	P199/GC12	92	P170	130	V_{SS}	168	P108	206	P074	244	P045	282	P013
17	P229/RA3	55	P198/GT8	93	P169	131	V_{DD}.PAD3	169	P107	207	P073	245	P044	283	P012
18	P228/RA2	56	V_{DD}	94	P168	132	P138	170	P106	208	P072	246	P043	284	P011
19	P227/RA1	57	P197/GT9	95	P167	133	P137	171	P105	209	P071	247	P042	285	P010
20	V_{DD}	58	P196/GT10	96	P166	134	P136	172	P104	210	V_{DD}	248	P041	286	P009
21	V_{SS}	59	P195/GT11	97	P165	135	P135	173	P103	211	V_{SS}	249	P040	287	P008
22	P226/RA0	60	V_{DD}.PAD4	98	P164	136	P134	174	P102	212	P070	250	P039	288	P007
23	P225	61	V_{SS}	99	P163	137	P133	175	P101	213	P069	251	P038	289	V_{SS}
24	P224/CA8	62	P194/GT12	100	V_{SS}	138	P132	176	P100	214	P068	252	V_{SS}	290	P006
25	P223/CA7	63	P193	101	V_{DD}.PAD3	139	P131	177	P099	215	P067	253	V_{DD}. PAD1	291	P005
26	P222/CA6	64	P192	102	P162	140	P130	178	V_{DD}. PAD2	216	P066	254	P037	292	P004
27	P221/CA5	65	P191	103	P161	141	P129	179	V_{SS}	217	P065	255	P036	293	P003
28	V_{DD}.X	66	P190	104	P160	142	P128	180	P098	218	P064	256	P035	294	TRST*
29	P220/CA4	67	P189	105	P159	143	P127	181	P097	219	P063	257	P034	295	P002
30	P219/CA3	68	P188	106	P158	144	P126	182	P096	220	P062	258	P033	296	V_{SS}
31	P218/CA2	69	P187	107	P157	145	P125	183	P095	221	V_{DD}. PAD2	259	P032	297	V_{DD}. PAD1
32	P217/CA1	70	P186	108	P156	146	V_{SS}	184	P094	222	V_{SS}	260	P031	298	TCK
33	P216/CA0	71	V_{SS}	109	P155	147	V_{DD}.PAD3	185	P093	223	P061	261	P030	299	TDO
34	P215/GT5	72	P185	110	P154	148	P124	186	P092	224	P060	262	P029	300	P001
35	V_{DD}.PAD4	73	P184	111	P153	149	P123	187	P091	225	P059	263	P028	301	TMS
36	V_{SS}	74	P183	112	V_{SS}	150	P122	188	P090	226	P058	264	P027	302	TDI
37	P214/GT6	75	P182	113	V_{DD}	151	P121	189	P089	227	P057	265	P026	303	P000
38	P213/GT7	76	GT3	114	P152	152	P120	190	P088	228	GT1	266	V_{SS}	304	RCE

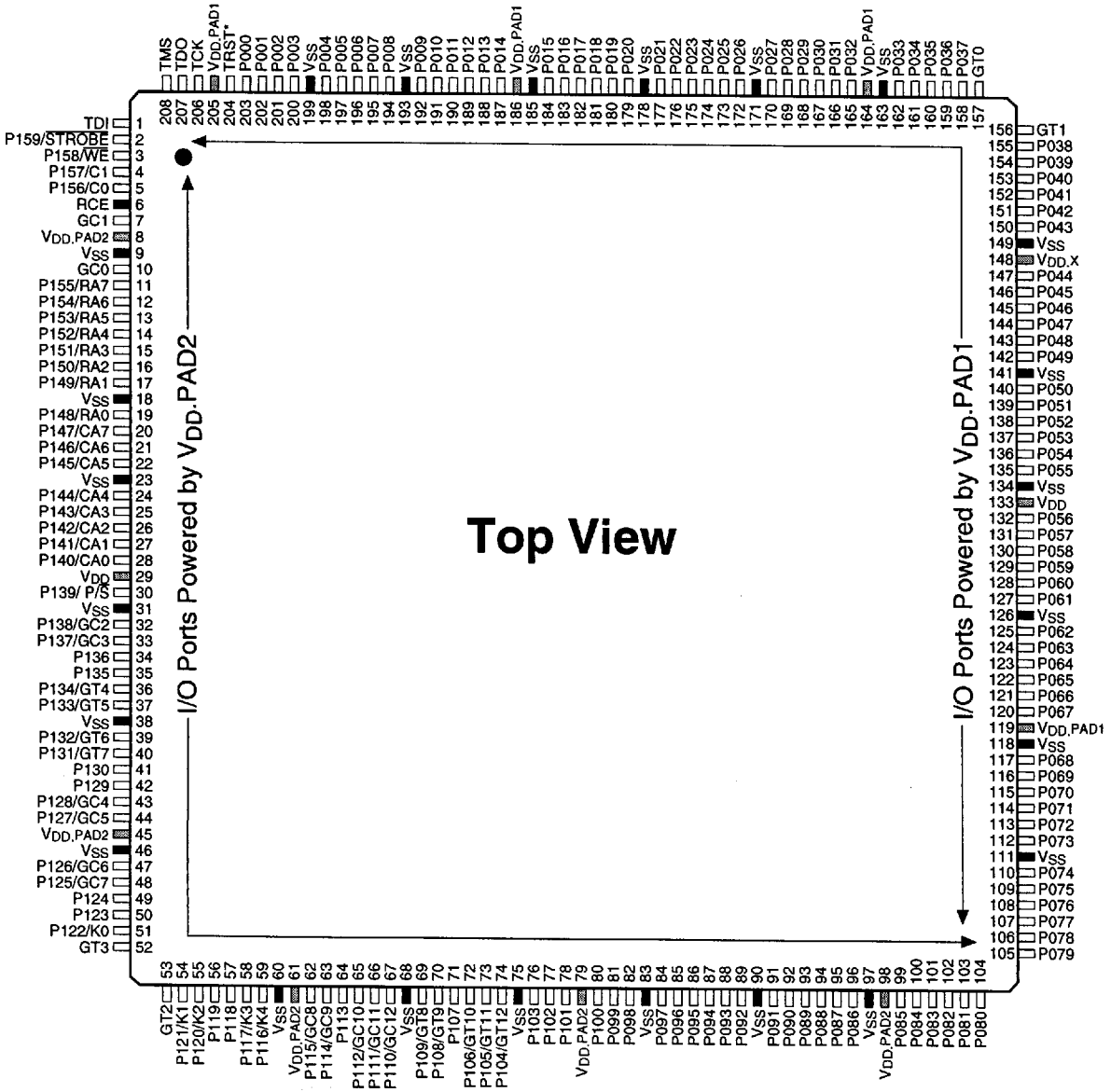
IQX240B [MQUAD®/304L] Package Pinout



IQX160 [MQUAD® and PQFP/208L] Package Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	TDI	53	GT2	105	P079	157	GT0
2	P159/STROBE	54	P121/K1	106	P078	158	P037
3	P158/WE	55	P120/K2	107	P077	159	P036
4	P157/C1	56	P119	108	P076	160	P035
5	P156/C0	57	P118	109	P075	161	P034
6	RCE	58	P117/K3	110	P074	162	P033
7	GC1	59	P116/K4	111	V_{SS}	163	V_{SS}
8	V_{DD}.PAD2	60	V_{SS}	112	P073	164	V_{DD}.PAD1
9	V_{SS}	61	V_{DD}.PAD2	113	P072	165	P032
10	GC0	62	P115/GC8	114	P071	166	P031
11	P155/RA7	63	P114/GC9	115	P070	167	P030
12	P154/RA6	64	P113	116	P069	168	P029
13	P153/RA5	65	P112/GC10	117	P068	169	P028
14	P152/RA4	66	P111/GC11	118	V_{SS}	170	P027
15	P151/RA3	67	P110/GC12	119	V_{DD}.PAD1	171	V_{SS}
16	P150/RA2	68	V_{SS}	120	P067	172	P026
17	P149/RA1	69	P109/GT8	121	P066	173	P025
18	V_{SS}	70	P108/GT9	122	P065	174	P024
19	P148/RA0	71	P107	123	P064	175	P023
20	P147/CA7	72	P106/GT10	124	P063	176	P022
21	P146/CA6	73	P105/GT11	125	P062	177	P021
22	P145/CA5	74	P104/GT12	126	V_{SS}	178	V_{SS}
23	V_{SS}	75	V_{SS}	127	P061	179	P020
24	P144/CA4	76	P103	128	P060	180	P019
25	P143/CA3	77	P102	129	P059	181	P018
26	P142/CA2	78	P101	130	P058	182	P017
27	P141/CA1	79	V_{DD}.PAD2	131	P057	183	P016
28	P140/CA0	80	P100	132	P056	184	P015
29	V_{DD}	81	P099	133	V_{DD}	185	V_{SS}
30	P139/ P/S	82	P098	134	V_{SS}	186	V_{DD}.PAD1
31	V_{SS}	83	V_{SS}	135	P055	187	P014
32	P138/GC2	84	P097	136	P054	188	P013
33	P137/GC3	85	P096	137	P053	189	P012
34	P136	86	P095	138	P052	190	P011
35	P135	87	P094	139	P051	191	P010
36	P134/GT4	88	P093	140	P050	192	P009
37	P133/GT5	89	P092	141	V_{SS}	193	V_{SS}
38	V_{SS}	90	V_{SS}	142	P049	194	P008
39	P132/GT6	91	P091	143	P048	195	P007
40	P131/GT7	92	P090	144	P047	196	P006
41	P130	93	P089	145	P046	197	P005
42	P129	94	P088	146	P045	198	P004
43	P128/GC4	95	P087	147	P044	199	V_{SS}
44	P127/GC5	96	P086	148	V_{DD}.X	200	P003
45	V_{DD}.PAD2	97	V_{SS}	149	V_{SS}	201	P002
46	V_{SS}	98	V_{DD}.PAD2	150	P043	202	P001
47	P126/GC6	99	P085	151	P042	203	P000
48	P125/GC7	100	P084	152	P041	204	TRST*
49	P124	101	P083	153	P040	205	V_{DD}.PAD1
50	P123	102	P082	154	P039	206	TCK
51	P122/K0	103	P081	155	P038	207	TDO
52	GT3	104	P080	156	GT1	208	TMS

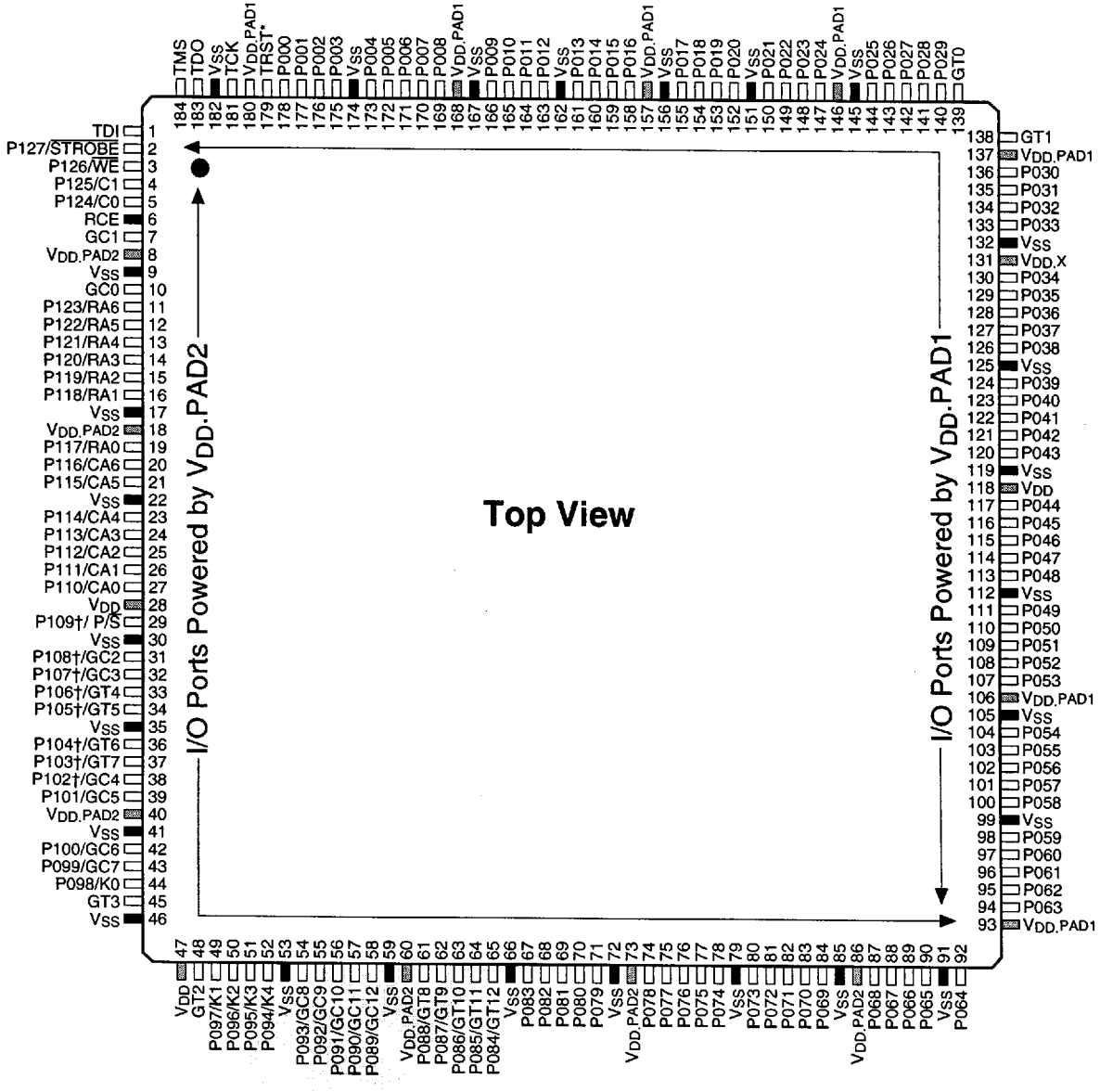
IQX160 [MQUAD® and PQFP/208L] Package Pinout



IQX128B [MQUAD® and PQFP/184L] Package Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	TDI	47	V_{DD}	93	V_{DD}.PAD1	139	GT0
2	P127/STROBE	48	GT2	94	P063	140	P029
3	P126/$\overline{WE}$	49	P097/K1	95	P062	141	P028
4	P125/C1	50	P096/K2	96	P061	142	P027
5	P124/C0	51	P095/K3	97	P060	143	P026
6	RCE	52	P094/K4	98	P059	144	P025
7	GC1	53	V_{SS}	99	V_{SS}	145	V_{SS}
8	V_{DD}.PAD2	54	P093/GC8	100	P058	146	V_{DD}.PAD1
9	V_{SS}	55	P092/GC9	101	P057	147	P024
10	GC0	56	P091/GC10	102	P056	148	P023
11	P123/RA6	57	P090/GC11	103	P055	149	P022
12	P122/RA5	58	P089/GC12	104	P054	150	P021
13	P121/RA4	59	V_{SS}	105	V_{SS}	151	V_{SS}
14	P120/RA3	60	V_{DD}.PAD2	106	V_{DD}.PAD1	152	P020
15	P119/RA2	61	P088/GT8	107	P053	153	P019
16	P118/RA1	62	P087/GT9	108	P052	154	P018
17	V_{SS}	63	P086/GT10	109	P051	155	P017
18	V_{DD}.PAD2	64	P085/GT11	110	P050	156	V_{SS}
19	P117/RA0	65	P084/GT12	111	P049	157	V_{DD}.PAD1
20	P116/CA6	66	V_{SS}	112	V_{SS}	158	P016
21	P115/CA5	67	P083	113	P048	159	P015
22	V_{SS}	68	P082	114	P047	160	P014
23	P114/CA4	69	P081	115	P046	161	P013
24	P113/CA3	70	P080	116	P045	162	V_{SS}
25	P112/CA2	71	P079	117	P044	163	P012
26	P111/CA1	72	V_{SS}	118	V_{DD}	164	P011
27	P110/CA0	73	V_{DD}.PAD2	119	V_{SS}	165	P010
28	V_{DD}	74	P078	120	P043	166	P009
29	P109†/ P/$\overline{S}$	75	P077	121	P042	167	V_{SS}
30	V_{SS}	76	P076	122	P041	168	V_{DD}.PAD1
31	P108†/GC2	77	P075	123	P040	169	P008
32	P107†/GC3	78	P074	124	P039	170	P007
33	P106†/GT4	79	V_{SS}	125	V_{SS}	171	P006
34	P105†/GT5	80	P073	126	P038	172	P005
35	V_{SS}	81	P072	127	P037	173	P004
36	P104†/GT6	82	P071	128	P036	174	V_{SS}
37	P103†/GT7	83	P070	129	P035	175	P003
38	P102†/GC4	84	P069	130	P034	176	P002
39	P101/GC5	85	V_{SS}	131	V_{DD}.X	177	P001
40	V_{DD}.PAD2	86	V_{DD}.PAD2	132	V_{SS}	178	P000
41	V_{SS}	87	P068	133	P033	179	TRST*
42	P100/GC6	88	P067	134	P032	180	V_{DD}.PAD1
43	P099/GC7	89	P066	135	P031	181	TCK
44	P098/K0	90	P065	136	P030	182	V_{SS}
45	GT3	91	V_{SS}	137	V_{DD}.PAD1	183	TDO
46	V_{SS}	92	P064	138	GT1	184	TMS

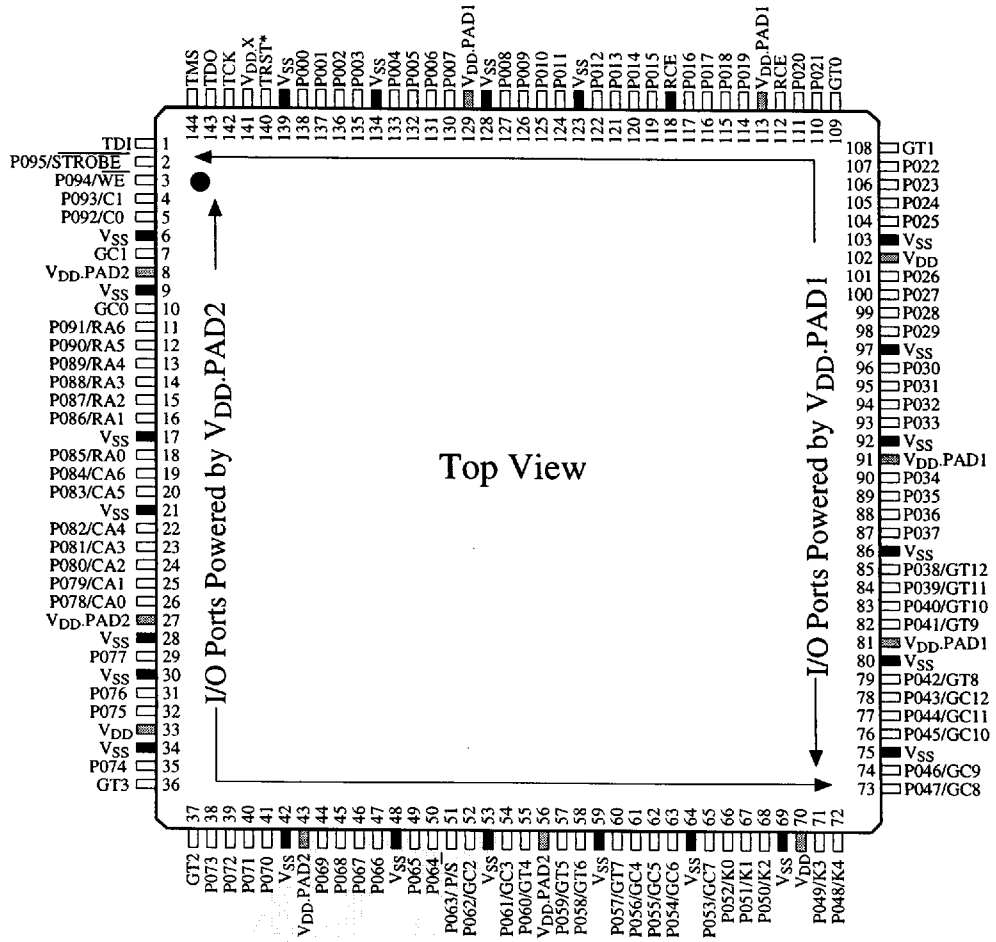
IQX128B [MQUAD® and PQFP/184L] Package Pinout



IQX96 [MQUAD®, TQFP and PQFP/144L] Package Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	TDI	37	GT2	73	P047/GC8	109	GT0
2	P095/STROBE	38	P073	74	P046/GC9	110	P021
3	P094/$\overline{WE}$	39	P072	75	V_{SS}	111	P020
4	P093/C1	40	P071	76	P045/GC10	112	RCE
5	P092/C0	41	P070	77	P044/GC11	113	V_{DD}.PAD1
6	Vss	42	V_{SS}	78	P043/GC12	114	P019
7	GC1	43	V_{DD}.PAD2	79	P042/GT8	115	P018
8	V_{DD}.PAD2	44	P069	80	Vss	116	P017
9	Vss	45	P068	81	V_{DD}.PAD1	117	P016
10	GC0	46	P067	82	P041/GT9	118	Vss
11	P091/RA6	47	P066	83	P040/GT10	119	P015
12	P090/RA5	48	Vss	84	P039/GT11	120	P014
13	P089/RA4	49	P065	85	P038/GT12	121	P013
14	P088/RA3	50	P064	86	Vss	122	P012
15	P087/RA2	51	P063/ P/$\overline{S}$	87	P037	123	Vss
16	P086/RA1	52	P062/GC2	88	P036	124	P011
17	Vss	53	Vss	89	P035	125	P010
18	P085/RA0	54	P061/GC3	90	P034	126	P009
19	P084/CA6	55	P060/GT4	91	V_{DD}.PAD1	127	P008
20	P083/CA5	56	V_{DD}.PAD2	92	Vss	128	Vss
21	Vss	57	P059/GT5	93	P033	129	V_{DD}.PAD1
22	P082/CA4	58	P058/GT6	94	P032	130	P007
23	P081/CA3	59	Vss	95	P031	131	P006
24	P080/CA2	60	P057/GT7	96	P030	132	P005
25	P079/CA1	61	P056/GC4	97	Vss	133	P004
26	P078/CA0	62	P055/GC5	98	P029	134	Vss
27	V_{DD}.PAD2	63	P054/GC6	99	P028	135	P003
28	V_{SS}	64	Vss	100	P027	136	P002
29	P077	65	P053/GC7	101	P026	137	P001
30	Vss	66	P052/K0	102	V_{DD}	138	P000
31	P076	67	P051/K1	103	Vss	139	Vss
32	P075	68	P050/K2	104	P025	140	TRST*
33	V_{DD}	69	Vss	105	P024	141	V_{DD}.X
34	Vss	70	V_{DD}	106	P023	142	TCK
35	P074	71	P049/K3	107	P022	143	TDO
36	GT3	72	P048/K4	108	GT1	144	TMS

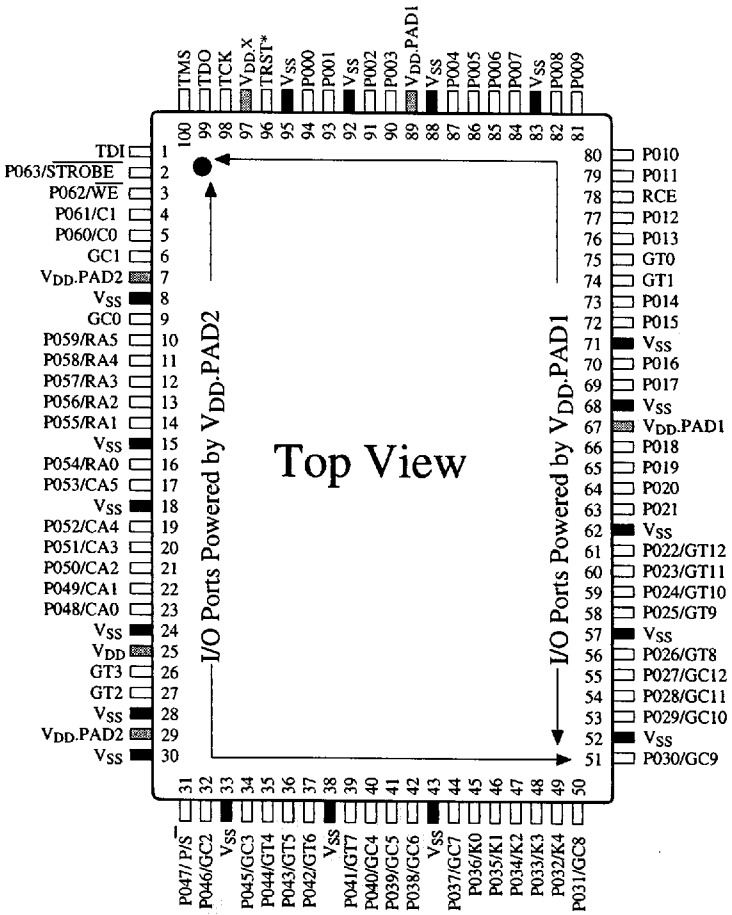
IQX96 [MQUAD®, PQFP and TQFP/144L Package] Pinout



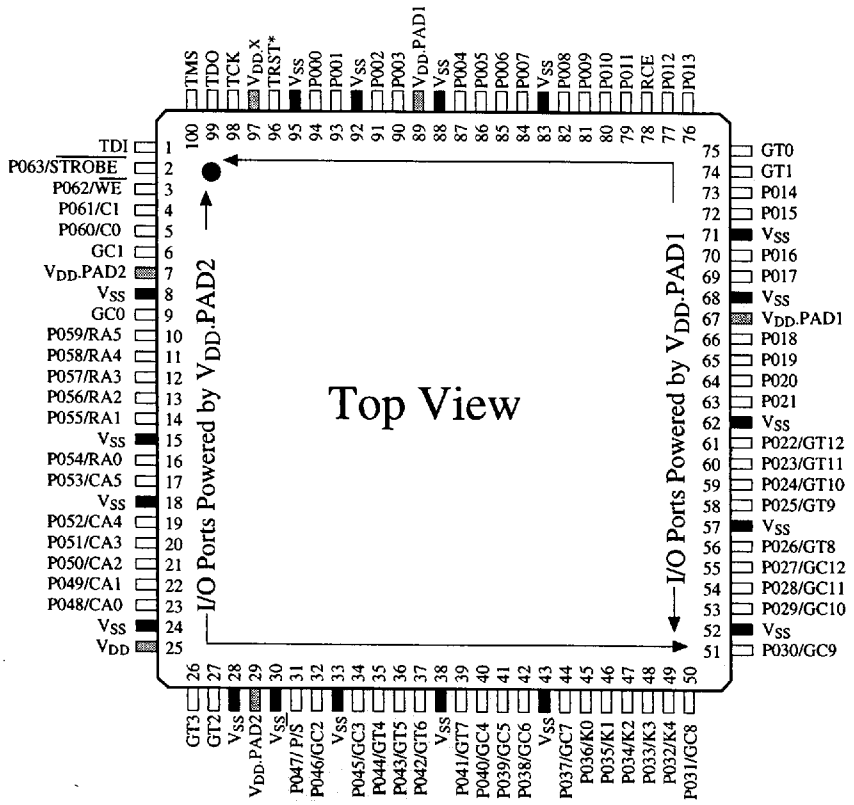
IQX64B [MQUAD®, PQFP and TQFP/100L] Package Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	TDI	26	GT3	51	P030/GC9	76	P013
2	P063/$\overline{\text{STROBE}}$	27	GT2	52	V_{SS}	77	P012
3	P062/$\overline{\text{WE}}$	28	V_{SS}	53	P029/GC10	78	RCE
4	P061/C1	29	V_{DD}.PAD2	54	P028/GC11	79	P011
5	P060/C0	30	Vss	55	P027/GC12	80	P010
6	GC1	31	P047/ P/$\overline{\text{S}}$	56	P026/GT8	81	P009
7	V_{DD}.PAD2	32	P046/GC2	57	Vss	82	P008
8	Vss	33	Vss	58	P025/GT9	83	Vss
9	GC0	34	P045/GC3	59	P024/GT10	84	P007
10	P059/RA5	35	P044/GT4	60	P023/GT11	85	P006
11	P058/RA4	36	P043/GT5	61	P022/GT12	86	P005
12	P057/RA3	37	P042/GT6	62	Vss	87	P004
13	P056/RA2	38	Vss	63	P021	88	Vss
14	P055/RA1	39	P041/GT7	64	P020	89	V_{DD}.PAD1
15	Vss	40	P040/GC4	65	P019	90	P003
16	P054/RA0	41	P039/GC5	66	P018	91	P002
17	P053/CA5	42	P038/GC6	67	V_{DD}.PAD1	92	Vss
18	Vss	43	Vss	68	Vss	93	P001
19	P052/CA4	44	P037/GC7	69	P017	94	P000
20	P051/CA3	45	P036/K0	70	P016	95	Vss
21	P050/CA2	46	P035/K1	71	Vss	96	TRST*
22	P049/CA1	47	P034/K2	72	P015	97	V_{DD}.X
23	P048/CA0	48	P033/K3	73	P014	98	TCK
24	V_{SS}	49	P032/K4	74	GT1	99	TDO
25	V_{DD}	50	P031/GC8	75	GT0	100	TMS

IQX64B [MQUAD® and PQFP/100L Package] Pinout

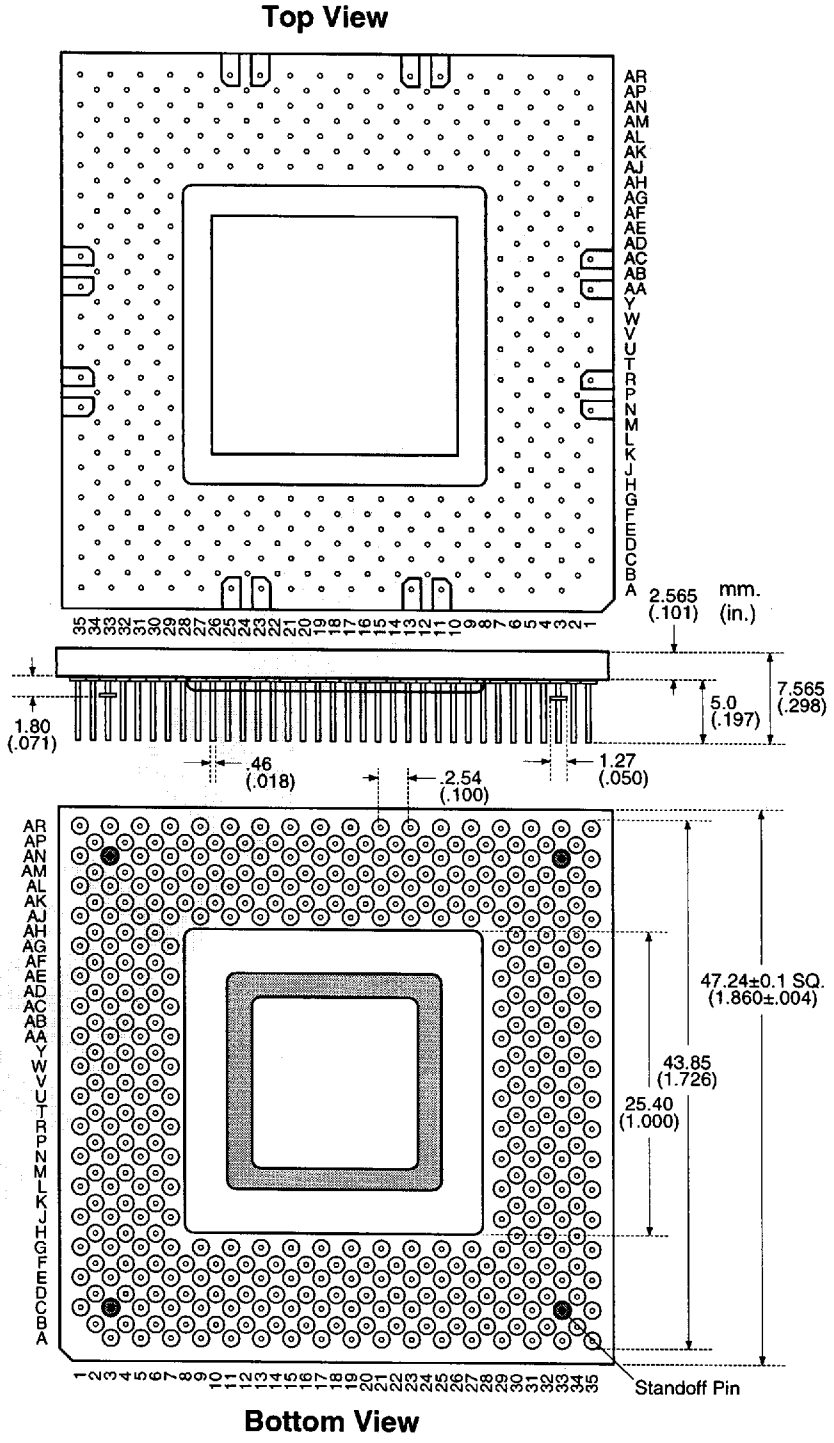


IQX64B [TQFP/100L Package] Pinout



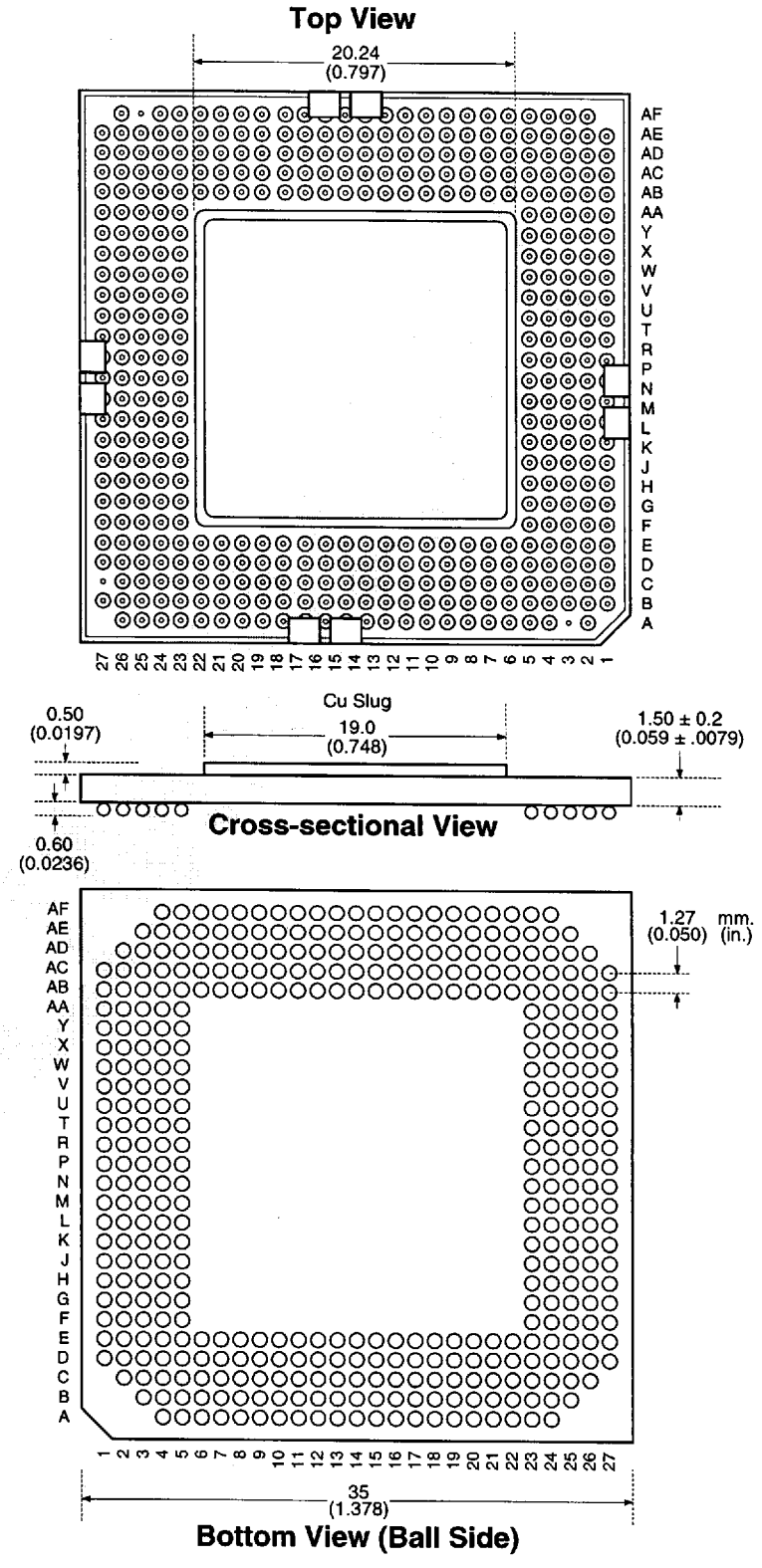
Mechanical Specification

IQX320 [PPGA/391L] Package Dimensions



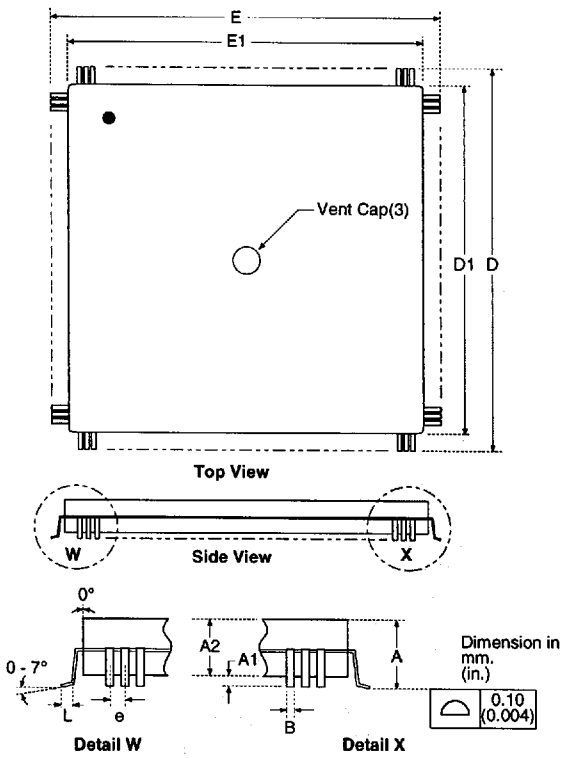
Note: Use "mm" as the controlling dimension.

IQX320 [PBGA/416L] Package Dimensions



Note: Use "mm" as the controlling dimension.

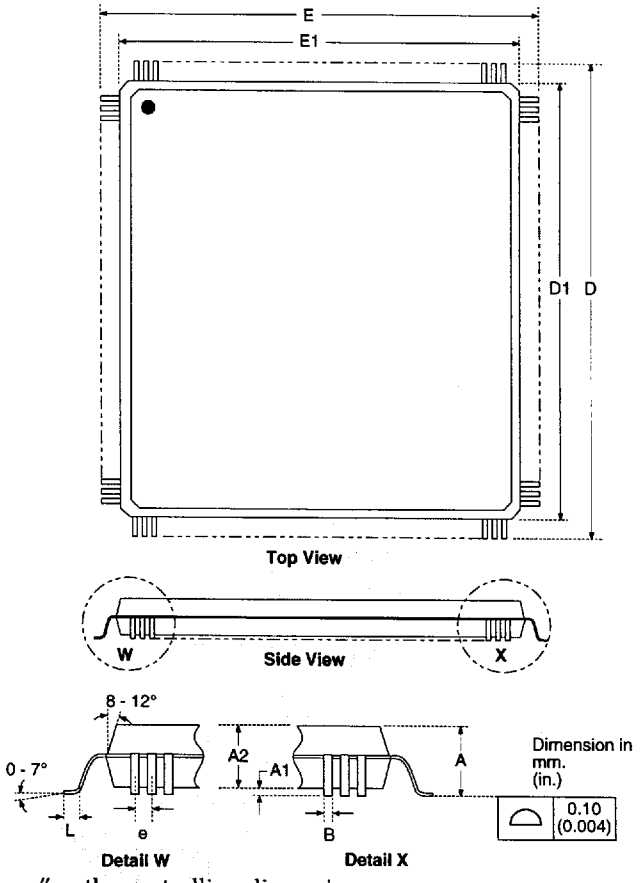
MQUAD Package Dimensions (1, 2)



Notes: (1) Use "mm" as the controlling dimension
(2) MQUAD - Metal Quad Flat Package

Package Dimension Table		MQUAD/304L		MQUAD/208L		MQUAD/184L		MQUAD/144L		MQUAD/100L	
		inch	mm	inch	mm	inch	mm	inch	mm	inch	mm
A	max	0.172	4.38	0.156	3.96	0.156	3.96	0.152	3.96	0.128	3.26
A1	min	0.010	0.25	0.014	0.35	0.014	0.35	0.014	0.35	0.011	0.28
	max	0.020	0.51	0.021	0.53	0.021	0.53	0.021	0.53	0.019	0.48
A2	min	0.144	3.66	0.125	3.18	0.125	3.17	0.125	3.17	0.099	2.51
	max	0.154	3.92	0.135	3.43	0.135	3.43	0.135	3.43	0.109	2.78
D	min	1.669	42.46	1.197	30.45	1.220	31.00	1.219	30.95	0.904	22.95
	max	1.685	42.87	1.213	30.86	1.236	31.40	1.238	31.45	0.923	23.45
D1	min	1.558	39.64	1.086	27.63	1.086	27.59	1.086	27.59	0.779	19.74
	max	1.566	39.84	1.094	27.83	1.094	27.79	1.094	27.79	0.781	19.84
E	min	1.669	42.46	1.197	30.45	1.22	31.00	1.219	30.95	0.667	16.95
	max	1.685	42.87	1.213	30.86	1.236	31.40	1.238	31.45	0.687	17.45
E1	min	1.558	39.64	1.086	27.63	1.086	27.59	1.086	27.59	0.541	13.74
	max	1.566	39.84	1.094	27.83	1.094	27.79	1.094	27.79	0.545	13.84
L	min	0.020	0.51	0.020	0.51	0.020	0.50	0.029	0.73	0.029	0.73
	max	0.030	0.76	0.030	0.76	0.030	0.75	0.041	1.03	0.041	1.03
B	min	0.007	0.18	0.006	0.15	0.006	0.16	0.009	0.22	0.009	0.22
	max	0.011	0.28	0.011	0.28	0.011	0.27	0.014	0.35	0.014	0.35
e	BSC.	0.0197	0.50	0.0197	0.50	0.0197	0.50	0.0256	0.65	0.0256	0.65

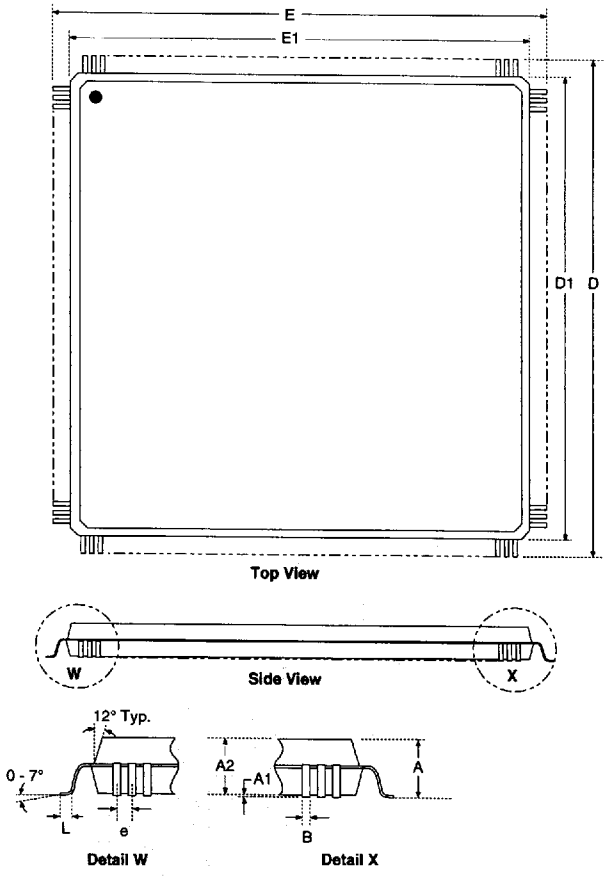
PQFP Package Dimensions (1, 2)



Notes: (1) Use "mm" as the controlling dimension

Package Dimension Table		PQFP/208L		PQFP/184L		PQFP/144L		PQFP/100L	
		inch	mm	inch	mm	inch	mm	inch	mm
A	max	0.157	3.99	0.157	3.99	0.157	3.99	0.130	3.30
A1	min	0.010	0.25	0.010	0.25	0.010	0.25	0.011	0.27
	max	0.017	0.43	0.017	0.43	0.017	0.43	0.017	0.43
A2	min	0.135	3.43	0.135	3.43	0.135	3.43	0.102	2.60
	max	0.140	3.56	0.140	3.56	0.140	3.56	0.110	2.80
D	min	1.195	30.40	1.219	31.01	1.219	31.01	0.903	22.95
	max	1.215	30.91	1.238	31.49	1.238	31.49	0.923	23.45
D1	min	1.098	27.93	1.098	27.93	1.098	27.93	0.783	19.90
	max	1.106	28.14	1.106	28.14	1.106	28.14	0.791	20.10
E	min	1.195	30.40	1.219	31.01	1.219	31.01	0.667	16.95
	max	1.215	30.91	1.238	31.49	1.238	31.49	0.687	17.45
E1	min	1.098	27.93	1.098	27.93	1.098	27.93	0.547	13.90
	max	1.106	28.14	1.106	28.14	1.106	28.14	0.555	14.10
L	min	0.018	0.46	0.029	0.74	0.029	0.74	0.023	0.60
	max	0.030	0.76	0.041	1.04	0.041	1.04	0.039	1.00
B	min	0.006	0.15	0.006	0.15	0.009	0.23	0.01	0.25
	max	0.011	0.28	0.011	0.28	0.014	0.36	0.014	0.35
e	BSC.	0.0197	0.50	0.0197	0.50	0.0256	0.65	0.0256	0.65

TQFP Package Dimensions (1, 2)



Notes: (1) Use "mm" as the controlling dimension

Package Dimension Table		TQFP/144L		TQFP/100L	
		inch	mm	inch	mm
A	max	0.063	1.60	0.063	1.60
A1	min	0.002	0.05	0.002	0.05
	max	0.006	0.15	0.006	0.15
A2	min	0.053	1.35	0.053	1.35
	max	0.057	1.45	0.057	1.45
D	min	0.858	21.80	0.622	15.80
	max	0.874	22.20	0.638	16.20
D1	min	0.783	19.90	0.547	13.90
	max	0.791	20.10	0.555	14.10
E	min	0.858	21.80	0.622	15.80
	max	0.874	22.20	0.638	16.20
E1	min	0.783	19.90	0.547	13.90
	max	0.791	20.10	0.555	14.10
L	min	0.018	0.45	0.012	0.30
	max	0.030	0.75	0.028	0.70
B	min	0.007	0.17	0.007	0.17
	max	0.011	0.2 7	0.111	0.27
e	BSC.	0.0197	0.50	0.0197	0.50

Package Thermal Characteristics

Pkg. Pins	100			144			184		208		304	391	416
Pkg. Type	PQFP	MQUAD	TQFP	PQFP	MQUAD	TQFP	PQFP	MQUAD	PQFP	MQUAD	MQUAD	PPGA	PBGA
Pkg. Code	PQ100	MQ100	TQ100	PQ144	MQ144	TQ144	PQ184	MQ184	PQ208	MQ208	MQ304	PP391	PB416
Θ_{JC}	7.0		10.4	6.8	6.3	8.5	6.6		6.6	3.0	2.0		
Θ_{JA}	40.3		38.1	38.8	25.2	29.7	37.4		36.6	14.7	11.1		
Θ_{JA}	31.5		33.6	29.8	23.5	25.2	28.3		27.4	11.9	8.7		
Θ_{JA}	25		32.1	24.6	19.7	23.8	24.2		24.0	10.7	7.9		
Θ_{JA}	22		30.9	21.8	17.1	22.7	21.7		21.4	9.7	7.0		

Table 14: Package Thermal Coefficients

Appendix A - Tables for Determining Die Pad to I/O Port Pin Mapping and Locations of Real SRAM Cell

The following tables help determine the locations of the real SRAM cells in the Switch Matrix. The SRAM cell controlling the connection between I/O Port "i" and I/O Port "j" is determined as follows:

Get the *Index* values corresponding to I/O Port numbers "i" and "j". If the index value for "i" is greater than index value for "j", then the SRAM cell has the row (word) address i* and column (bit) address j*, otherwise it has row address of j* and column address of i*. The numbers i* and j* represent the I/O Port locations on the die.

Example 1: On the IQX96, the SRAM cell controlling the connection between I/O Port 10 and I/O Port 50 is at location: Row address = 10, Column Address = 50

Example 2: On the IQX160, the SRAM cell controlling the connection between I/O Port 20 and I/O Port 100 is at location: Row address = 100, Column Address = 20

Example 3: On the IQX240B, the SRAM cell controlling the connection between I/O Port 80 and I/O Port 180 is at location: Row address = 241, Column Address = 110. Note that the IQX240B is a bondout version of IQX320 die, and the I/O Ports 80 and 180 on the device package are the I/O Ports 110 and 241 respectively.

Table A-1: IQX96 and IQX64B Table

Die PAD and IQX96 I/O Port	IQX64B I/O Port	Index	Die PAD and IQX96 I/O Port	IQX64B I/O Port	Index	Die PAD and IQX96 I/O Port	IQX64B I/O Port	Index	Die PAD and IQX96 I/O Port	IQX64B I/O Port	Index
0	0	2	24	-	0	48	32	95	72	-	93
1	1	6	25	-	4	49	33	91	73	-	89
2	-	10	26	-	8	50	34	87	74	-	85
3	-	14	27	16	12	51	35	83	75	-	81
4	2	18	28	-	16	52	36	79	76	-	77
5	3	22	29	17	20	53	37	75	77	-	73
6	-	26	30	-	24	54	38	71	78	48	69
7	-	30	31	-	28	55	39	67	79	49	65
8	-	34	32	-	32	56	40	63	80	50	61
9	-	38	33	-	36	57	41	59	81	51	57
10	-	42	34	18	40	58	42	55	82	52	53
11	-	46	35	19	44	59	43	51	83	53	49
12	4	50	36	20	48	60	44	47	84	-	45
13	5	54	37	21	52	61	45	43	85	54	41
14	6	58	38	22	56	62	46	39	86	55	37
15	7	62	39	23	60	63	47	35	87	56	33
16	8	66	40	24	64	64	-	31	88	57	29
17	9	70	41	25	68	65	-	27	89	58	25
18	10	74	42	26	72	66	-	23	90	59	21
19	11	78	43	27	76	67	-	19	91	-	17
20	12	82	44	28	80	68	-	15	92	60	13
21	13	86	45	29	84	69	-	11	93	61	9
22	14	90	46	30	88	70	-	7	94	62	5
23	15	94	47	31	92	71	-	3	95	63	1

Table A-2: IQX160 and IQX128B Table

Die PAD and IQX160 I/O Port	IQX128B I/O Port	Index	Die PAD and IQX160 I/O Port	IQX128B I/O Port	Index	Die PAD and IQX160 I/O Port	IQX128B I/O Port	Index	Die PAD and IQX160 I/O Port	IQX128B I/O Port	Index
0	0	2	40	-	0	80	64	159	120	96	157
1	1	6	41	-	4	81	65	155	121	97	153
2	2	10	42	32	8	82	66	151	122	98	149
3	3	14	43	33	12	83	-	147	123	-	145
4	4	18	44	34	16	84	67	143	124	-	141
5	5	22	45	35	20	85	68	139	125	99	137
6	6	26	46	36	24	86	69	135	126	100	133
7	7	30	47	-	28	87	70	131	127	101	129
8	8	34	48	37	32	88	71	127	128	102	125
9	9	38	49	38	36	89	-	123	129	-	121
10	10	42	50	39	40	90	72	119	130	-	117
11	-	46	51	40	44	91	73	115	131	103	113
12	-	50	52	-	48	92	74	111	132	104	109
13	11	54	53	41	52	93	75	107	133	105	105
14	12	58	54	42	56	94	76	103	134	106	101
15	13	62	55	43	60	95	-	99	135	-	97
16	14	66	56	44	64	96	77	95	136	-	93
17	-	70	57	45	68	97	78	91	137	107	89
18	-	74	58	46	72	98	79	87	138	108	85
19	15	78	59	-	76	99	80	83	139	109	81
20	16	82	60	47	80	100	81	79	140	110	77
21	17	86	61	48	84	101	-	75	141	111	73
22	18	90	62	49	88	102	82	71	142	112	69
23	-	94	63	50	92	103	83	67	143	113	65
24	-	98	64	51	96	104	84	63	144	114	61
25	19	102	65	-	100	105	85	59	145	115	57
26	20	106	66	52	104	106	86	55	146	116	53
27	21	110	67	53	108	107	-	51	147	-	49
28	22	114	68	54	112	108	87	47	148	117	45
29	-	118	69	55	116	109	88	43	149	118	41
30	-	122	70	56	120	110	89	39	150	119	37
31	23	126	71	-	124	111	90	35	151	120	33
32	24	130	72	57	128	112	91	31	152	121	29
33	25	134	73	58	132	113	-	27	153	122	25
34	26	138	74	59	136	114	92	23	154	123	21
35	27	142	75	60	140	115	93	19	155	-	17
36	28	146	76	61	144	116	94	15	156	124	13
37	29	150	77	62	148	117	95	11	157	125	9
38	30	154	78	63	152	118	-	7	158	126	5
39	31	158	79	-	156	119	-	3	159	127	1

Table A-3: IQX320 and IQX240B Table

Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index	Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index	Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index	Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index
0	-	2	40	30	162	80	-	0	120	90	160
1	0	6	41	31	166	81	60	4	121	91	164
2	-	10	42	32	170	82	-	8	122	92	168
3	1	14	43	33	174	83	61	12	123	93	172
4	-	18	44	34	178	84	-	16	124	94	176
5	2	22	45	35	182	85	62	20	125	95	180
6	-	26	46	36	186	86	-	24	126	96	184
7	3	30	47	37	190	87	63	28	127	97	188
8	-	34	48	38	194	88	-	32	128	98	192
9	4	38	49	39	198	89	64	36	129	99	196
10	-	42	50	40	202	90	-	40	130	100	200
11	5	46	51	41	206	91	65	44	131	101	204
12	-	50	52	42	210	92	-	48	132	102	208
13	6	54	53	43	214	93	66	52	133	103	212
14	-	58	54	44	218	94	67	56	134	104	216
15	7	62	55	45	222	95	68	60	135	105	220
16	8	66	56	-	226	96	-	64	136	106	224
17	9	70	57	46	230	97	69	68	137	107	228
18	10	74	58	-	234	98	-	72	138	108	232
19	11	78	59	47	238	99	70	76	139	109	236
20	12	82	60	-	242	100	-	80	140	-	240
21	13	86	61	48	246	101	71	84	141	110	244
22	14	90	62	-	250	102	72	88	142	-	248
23	15	94	63	49	254	103	73	92	143	111	252
24	-	98	64	-	258	104	74	96	144	-	256
25	16	102	65	50	262	105	75	100	145	112	260
26	17	106	66	-	266	106	76	104	146	-	264
27	18	110	67	51	270	107	77	108	147	113	268
28	19	114	68	-	274	108	78	112	148	-	272
29	20	118	69	52	278	109	79	116	149	114	276
30	21	122	70	-	282	110	80	120	150	-	280
31	22	126	71	53	286	111	81	124	151	115	284
32	23	130	72	-	290	112	82	128	152	-	288
33	24	134	73	54	294	113	83	132	153	116	292
34	-	138	74	-	298	114	84	136	154	-	296
35	25	142	75	55	302	115	85	140	155	117	300
36	26	146	76	56	306	116	86	144	156	-	304
37	27	150	77	57	310	117	87	148	157	118	308
38	28	154	78	58	314	118	88	152	158	-	312
39	29	158	79	59	318	119	89	156	159	119	316
160	-	319	200	149	159	240	-	317	280	-	157
161	120	315	201	150	155	241	180	313	281	208	153
162	-	311	202	151	151	242	181	309	282	-	149
163	121	307	203	152	147	243	182	305	283	209	145
164	-	303	204	153	143	244	-	301	284	-	141

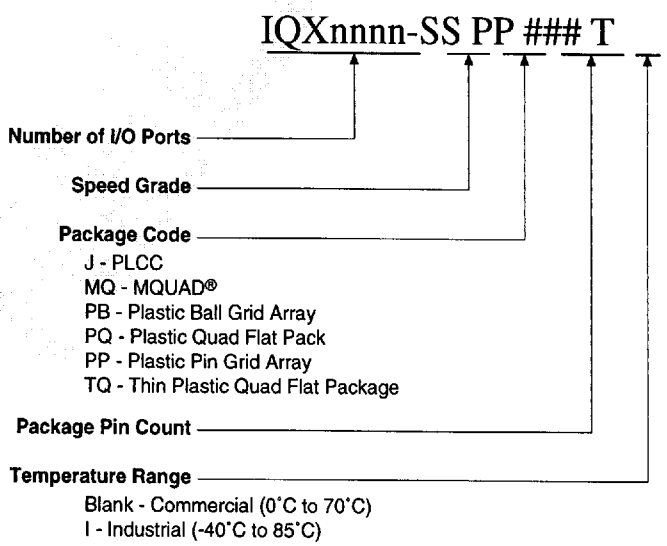
Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index	Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index	Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index	Die PAD and IQX320 I/O Port	IQX240 I/O Port	Index
165	122	299	205	154	139	245	183	297	285	210	137
166	-	295	206	155	135	246	-	293	286	-	133
167	123	291	207	156	131	247	184	289	287	211	129
168	-	287	208	157	127	248	-	285	288	-	125
169	124	283	209	158	123	249	185	281	289	212	121
170	-	279	210	159	119	250	-	277	290	-	117
171	125	275	211	160	115	251	186	273	291	213	113
172	-	271	212	161	111	252	-	269	292	-	109
173	126	267	213	162	107	253	187	265	293	214	105
174	-	263	214	163	103	254	188	261	294	-	101
175	127	259	215	164	99	255	189	257	295	215	97
176	-	255	216	165	95	256	190	253	296	216	93
177	128	251	217	166	91	257	191	249	297	217	89
178	-	247	218	167	87	258	192	245	298	218	85
179	129	243	219	168	83	259	193	241	299	219	81
180	-	239	220	169	79	260	194	237	300	220	77
181	130	235	221	170	75	261	195	233	301	221	73
182	131	231	222	-	71	262	-	229	302	222	69
183	132	227	223	171	67	263	196	225	303	223	65
184	133	223	224	-	63	264	-	221	304	224	61
185	134	219	225	172	59	265	197	217	305	225	57
186	135	215	226	-	55	266	-	213	306	226	53
187	136	211	227	173	51	267	198	209	307	227	49
188	137	207	228	-	47	268	199	205	308	228	45
189	138	203	229	174	43	269	200	201	309	229	41
190	139	199	230	-	39	270	201	197	310	230	37
191	140	195	231	175	35	271	202	193	311	231	33
192	141	191	232	-	31	272	203	189	312	232	29
193	142	187	233	176	27	273	204	185	313	233	25
194	143	183	234	-	23	274	-	181	314	234	21
195	144	179	235	177	19	275	205	177	315	235	17
196	145	175	236	-	15	276	-	173	316	236	13
197	146	171	237	178	11	277	206	169	317	237	9
198	147	167	238	-	7	278	-	165	318	238	5
199	148	163	239	179	3	279	207	161	319	239	1

Component Availability and Ordering Information

The following table lists the IQ devices and the different package options, speed grades and operating temperature ranges that will be available. Contact I-Cube Marketing for more up–to–date information on the current product availability.

Package	Pins	100			144			184		208		304	391	416
	Type	PQFP	MQUAD	TQFP	PQFP	MQUAD	TQFP	PQFP	MQUAD	PQFP	MQUAD	MQUAD	PPGA	PBGA
	Code	PQ100	MQ100	TQ100	PQ144	MQ144	TQ144	PQ184	MQ184	PQ208	MQ208	MQ304	PP391	PB416
IQX320	-15												C, I	C, I
	-12												C, I	C, I
	-10												C, I	C, I
	-7												C	C
IQX240B	-15											C, I		
	-12											C, I		
	-10											C, I		
	-7											C		
IQX160	-15									C, I	C, I			
	-12									C, I	C, I			
	-10									C, I	C, I			
	-7									C	C			
IQX128B	-15							C, I	C, I					
	-12							C, I	C, I					
	-10							C	C					
	-7							C	C					
IQX96B	-15				C, I	C, I	C, I							
	-12				C, I	C, I	C, I							
	-10				C, I	C, I	C, I							
	-7				C	C	C							
IQX64B	-15	C, I	C, I	C, I										
	-12	C, I	C, I	C, I										
	-10	C, I	C, I	C, I										
	-6	C	C	C										

Table 4: Component Availability



IQX Family At A Glance

Feature	IQX320	IQX240B	IQX160	IQX128B	IQX96	IQX64B
Number of Usable I/O Port Pins	320	240	160	128	96	64
Switch Matrix Size	320 lines	240 lines	160 lines	128 lines	96 lines	64 lines
Programmable I/O Port Attributes						
Signal Direction	IN, OUT, BIDIR	IN, OUT, BIDIR	IN, OUT, BIDIR	IN, OUT, BIDIR	IN, OUT, BIDIR	IN, OUT, BIDIR
Dataflow	Flow-through, Latched, Clocked	Flow-through, Latched, Clocked	Flow-through, Latched, Clocked	Flow-through, Latched, Clocked	Flow-through, Latched, Clocked	Flow-through, Latched, Clocked
Control Signals	Clock, Clock Enable, Input Tristate, Output Tristate	Clock, Clock Enable, Input Tristate, Output Tristate	Clock, Clock Enable, Input Tristate, Output Tristate	Clock, Clock Enable, Input Tristate, Output Tristate	Clock, Clock Enable, Input Tristate, Output Tristate	Clock, Clock Enable, Input Tristate, Output Tristate
Number of Clock Control Pins						
dedicated	4	4	2	2	2	2
shared with I/O Port Pins	9	9	11	11	11	11
Number of Tristate Control Pins						
dedicated	5	5	4	4	4	4
shared with I/O Port Pins	8	8	9	9	9	9
I/O Ports Used By RapidConfigure Interface	22	22	20	10	18	16
Pin-to-Pin Delay	7.5 ns	7.5 ns	7.5 ns	7.5 ns	6 ns	6 ns
NRZ Data Rate	180 Mbs	180 Mbs	200 Mbs	200 Mbs	250 Mbs	250 Mbs
Maximum Clock Frequency	133 MHz	133 MHz	133 MHz	133 MHz	150 MHz	150 MHz
I/O Current Drive	12 mA	12 mA	12 mA	12 mA	12 mA	12 mA
I/O Voltage	5V	3V or 5V	3V or 5V	3V or 5V	3V or 5V	3V or 5V
Process	0.6µ	0.6µ	0.6µ	0.6µ	0.6µ	0.6µ
Packages	391 PPGA 416 PBGA	304 MQUAD	208 PQFP 208 MQUAD	184 PQFP 184 MQUAD	144 PQFP 144 TQFP 144 MQUAD	100 PQFP 100 TQFP 100 MQUAD

I-Cube®, Inc.

2605 S. Winchester Blvd.
Campbell, CA 95008, USA

Phone: ++ (408) 341-1888
Fax: ++ (408) 341-1899
Email: marketing@icube.com
Internet: http://www.icube.com

IQX Family Data Sheet [v1.0]
[Preliminary]
July 1996
Document # D-11-014