HYM532210A E-Series

2M x 32-bit CMOS DRAM MODULE

DESCRIPTION

The HYM532210A is a 2M x 32-bit Fast Page mode CMOS DRAM module consisting of four HY5117800B in 28/28 pin SOJ or TSOPII on a 72 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitor is mounted for each DRAM.
The HYM532210AE/ASLE/ATE/ASLTE are Tin-Lead plated and HYM532210AEG/ASLEG/ATEG/ASLTEG are Gold plated socket type Single In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- **Low power dissipation**
  Max. self-refresh 6.6mW (SL-part)
  Max. battery back-up 8.8mW (SL-part)
  Max. CMOS standby 6.6mW (part)
  22.0mW
  Max. TTL standby 44.0mW
  Max. operating

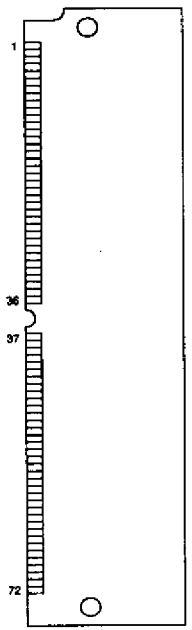
Speed	Power
60	2.64W
70	2.20W
80	1.98W

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

- **Fast Page mode operation**
- **CAS-before-RAS, RAS-only, Hidden refresh and Self-Refresh**
- **2048 refresh cycles / 256ms (SL-part)**
  2048 refresh cycles / 32ms

PIN CONNECTION



PIN DESCRIPTION

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$-$\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0-A10	Address Input
DQ0-DQ31	Data Input/Output
PD1-PD4	Presence Detect
Vcc	Power (+ 5V)
Vss	Ground

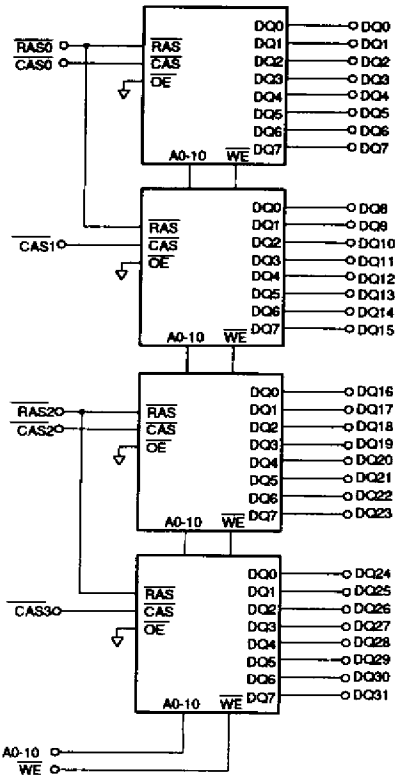
PIN NAME

#	NAME	#	NAME
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ17	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ18	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ19	45	NC
10	Vcc	46	NC
11	NC	47	$\overline{WE}$
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	NC	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	NC	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PRESENCE DETECT PIN

PIN	-60	-70	-80
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	Vss	NC
PD4	NC	NC	Vss

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	4.0	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	–1.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$+ 1.0, All other pins not under test= V_{SS}		-40	40	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	Vcc Supply Current, Operatin	t_{RC}= t_{RC} (min.)	60 70 80	- - -	480 400 360	mA	1,2,3
I_{CC2}	Vcc Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}		-	8	mA	
I_{CC3}	Vcc Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	480 400 360	mA	1,3
I_{CC4}	Vcc Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	60 70 80	- - -	480 400 360	mA	1,2,3
I_{CC5}	Vcc Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ Vcc–0.2V	 SL-part	- -	4 1.2	mA	 5
I_{CC6}	Vcc Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	480 400 360	mA	1,3
I_{CC7}	Vcc Supply Current, Battery Back Up (SL-part only)	t_{RC}= 125µs, $\overline{CAS}$= CBR cycling or 0.2V $\overline{WE}$= Vcc–0.2V A0-A10= Vcc–0.2V or 0.2V DQ0-DQ31= Vcc–0.2V, 0.2V, or open	$t_{RAS} \le$ 300ns $t_{RAS} \le$ 1µs	-	1.2 1.6	mA	1,4,5
I_{CC8}	Vcc Supply Current Self Refresh (SL-part only)	$\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V $\overline{OE}$ & $\overline{WE}$ & A0-A10= Vcc-0.2V or 0.2V DQ0-DQ31= Vcc - 0.2V, 0.2V or open			1.2	mA	5
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC8} depend on output loading. Specified values are obtained with the output open.
3. I_{CC} is specified as average current. For I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$= V_{IL}. For I_{CC4}, address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only t_{RAS}(max.)= 1µs is applied to refresh of battery backup but t_{RAS}(max.)= 10µs is applied to normal func tional operation..
5. ICC5(max.)= 1.2mA, ICC7 and ICC8 are applied to SL-part only (HYM532210ASLE/ASLTE/ASLEG/ASLTEG).

AC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS} = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532210A E-series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tRHCP	Time from CAS Precharge	40	-	40	-	50	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	8,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	8,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	8,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	40	ns	8,15
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	8
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	11
11	tT	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	6
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)		60	100K	70	100K	80	100K	ns
15	tRSH	RAS Hold Time	13	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	40	-	50	-	60	-	ns	
17	tCAS	CAS Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	CAS Precharge Time	7	-	10	-	10	-	ns	20
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	15
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	15
26	tAR	Column Address Hold Time from RAS	50	-	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	15
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	13,15
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	15
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	15
32	tWCR	Write Command Hold Time from RAS	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	15	-	ns	
35	tCWL	Write Command to CAS Lead Time	13	-	15	-	20	-	ns	22
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	15
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	15
38	tDHR	Data-In Hold Time Referenced to RAS	50	-	55	-	60	-	ns	
39	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	18
		SL-part	-	256	-	256	-	256		12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM532210A E-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	16,21
42	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15,24
43	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	20
44	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
45	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRASS	$\overline{RAS}$ Pulse (Self Refresh)	100	-	100	-	100	-	µs	
47	tRPS	$\overline{RAS}$ Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
48	tCHS	$\overline{CAS}$ Hold Time from $\overline{RAS}$ (Self Refresh)	-50	-	-50	-	-50	-	ns	

NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS}$= Vss during power-up, the HYM532210A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY5117800B data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.(V_{OH}= 2.0v,V_{OL}= 0.8V)
5. tOFF(max.)define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in late write or read-modify-write cycles.
8. twcs is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs≥ twcs(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. Measured with the specified current load and 100pF.
12. A burst of 2048 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 32ms after exiting self refresh (for SL-part).
13. If $t_{CWD} \geq t_{WCS(MIN.)}$, $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes bach to V_{IH}) is indeterminated.
14. In $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.
    In case of using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 2048 times during a 256ms after reset
    In case of using burst $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 2048 times during a 32ms after reset
    Incase of use $\overline{RAS}$ only refresh, refresh against all refresh address during a 32ms after reset
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

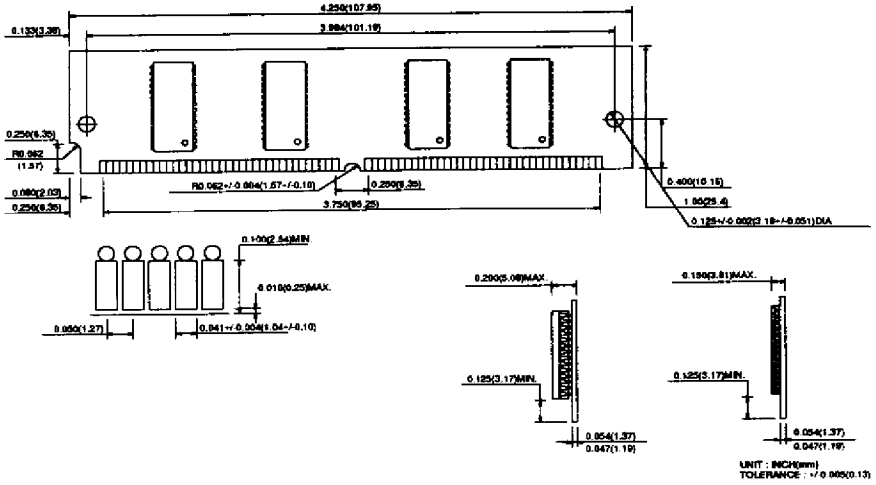
CAPACITANCE

(T_A= 25°C, V_{CC}= 5V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A10)	-	38	pF
C_{IN2}	Input Capacitance ($\overline{WE}$)	-	40	pF
C_{IN3}	Input Capacitance ($\overline{RAS0}$,$\overline{RAS2}$)	-	28	pF
C_{IN4}	Input Capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	-	18	pF
C_{DQ}	Data Input/output Capacitance (DQ0-DQ31)	-	17	pF

PACKAGE INFORMATION

72 pin Single In-line Memory (E ; Tin-Lead plated, EG ; Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM532210AE	60/70/80		SIMM	Tin-Lead
HYM532210ASLE	60/70/80	SL-part	SIMM	Tin-Lead
HYM532210ATE	60/70/80		SIMM	Tin-Lead
HYM532210ASLTE	60/70/80	SL-part	SIMM	Tin-Lead
HYM532210AEG	60/70/80		SIMM	Gold
HYM532210ASLEG	60/70/80	SL-part	SIMM	Gold
HYM532210ATEG	60/70/80		SIMM	Gold
HYM532210ASLTEG	60/70/80	SL-part	SIMM	Gold