

DS26LV31T

3V Enhanced CMOS Quad Differential Line Driver

General Description

The DS26LV31T is a high-speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV31T features low static I_{CC} of 100 μ A MAX which makes it ideal for battery powered and power conscious applications.

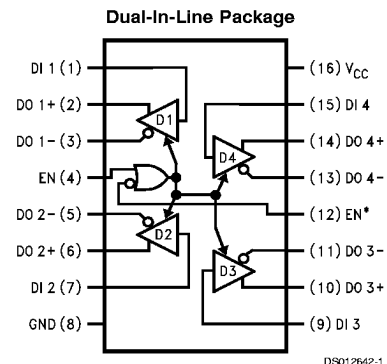
Differential outputs have the same V_{OD} guarantee ($\geq 2V$) as the 5V version.

The EN and EN* inputs allow active Low or active High control of the TRI-STATE® outputs. The enables are common to all four drivers. Protection diodes protect all the driver inputs against electrostatic discharge. Outputs have enhanced ESD protection providing greater than 7 kV tolerance. The driver and enable inputs (DI, EN, EN*) are compatible with low voltage LVTTTL and LVCMOS devices.

Features

- Industrial product meets TIA/EIA-422-B (RS-422) and ITU-T V.11 recommendation
- Military product conforms to TIA/EIA-422-B (RS-422)
- Interoperable with existing 5V RS-422 networks
- Industrial and Military temperature range
- Guaranteed V_{OD} of 2V min over operating conditions
- Balanced output crossover for low EMI (typical within 40 mV of 50% voltage level)
- Low power design (330 μ W 3.3V static)
- ESD ≥ 7 kV on cable I/O pins (HBM)
- Guaranteed AC parameter:
 - Maximum driver skew: 2 ns
 - Maximum transition time: 10 ns
- Pin compatible with DS26C31
- Available in SOIC and Cerpack packaging
- Standard Microcircuit Drawing (SMD) 5962-98584

Connection Diagram



DS012642-1

Top View

Order Number DS26LV31TM or DS26LV31W
See NS Package Number M16A or W16A

Truth Table

Enables		Input	Outputs	
EN	EN*	DI	DO+	DO-
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7V
Enable Input Voltage (EN, EN*)	-0.5V to $V_{CC} + 0.5V$
Driver Input Voltage (DI)	-0.5V to $V_{CC} + 0.5V$
Clamp Diode Current	± 20 mA
DC Output Current, per pin	± 150 mA
Driver Output Voltage (Power Off: DO+, DO-)	-0.5V to +7V
Maximum Package Power Dissipation +25°C	
M Package	1226 mW
W Package	1119 mW
Derate M Package 9.8 mW/°C above +25°C	
Derate W Package 7.5 mW/°C above +25°C	
Storage Temperature Range	-65°C to +150°C

Lead Temperature Range
Soldering

(4 sec.) +260°C

ESD Ratings (HBM, 1.5 k Ω , 100 pF)

Driver Outputs	≥ 7 kV
Other Pins	≥ 2.5 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature Range (T_A)				
DS26LV31T	-40	+25	+85	°C
DS26LV31W	-55	+25	+125	°C
Input Rise and Fall Time			500	ns

Electrical Characteristics (Note 2) (Note 3)

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Output Differential Voltage	$R_L = \infty$ (No Load)	DO+,		3.3	4	V
V_{OD2}	Output Differential Voltage	$R_L = 100\Omega$ (Figure 1)	DO-	2	2.6		V
ΔV_{OD2}	Change in Magnitude of Output Differential Voltage	$I_O \geq 20$ mA		-400	7	400	mV
V_{OD3}	Output Differential Voltage	$R_L = 3900\Omega$ (V.11) Figure 1 (Note 7)			3.2	3.6	V
V_{OC}	Common Mode Voltage	$R_L = 100\Omega$ (Figure 1)			1.5	2	V
ΔV_{OC}	Change in Magnitude of Common Mode Voltage			-400	6	400	mV
I_{OZ}	TRI-STATE Leakage Current	$V_{OUT} = V_{CC}$ or GND Drivers Disabled			± 0.5	± 20	μA
I_{SC}	Output Short Circuit Current	$V_{OUT} = 0V$ $V_{IN} = V_{CC}$ or GND (Note 4)		-40	-70	-150	mA
		$T_A = -40^\circ C$ to +85°C $T_A = -55^\circ C$ to +125°C (Note 10)		-30		-160	mA
I_{OFF}	Output Leakage Current	$V_{CC} = 0V$, $V_{OUT} = 3V$ or 6V			0.03	100	μA
		$V_{CC} = 0V$, $V_{OUT} = -0.25V$			-0.08	-100	μA
		$T_A = -40^\circ C$ to +85°C $T_A = -55^\circ C$ to +125°C				-200	μA
V_{IH}	High Level Input Voltage		DI,	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		EN,	GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	EN*			10	μA
I_{IL}	Low Level Input Current	$V_{IN} = GND$		-10			μA
V_{CL}	Input Clamp Voltage	$I_{IN} = -18$ mA				-1.5	V
I_{CC}	Power Supply Current	No Load, V_{IN} (all) = V_{CC} or GND	V_{CC}			100	μA
		$T_A = -40^\circ C$ to +85°C $T_A = -55^\circ C$ to +125°C				125	μA

Switching Characteristics - Industrial (Note 5) (Note 6)

Over supply voltage and -40°C to +85°C operating temperature range, unless otherwise specified

Sym	Parameter	Conditions	Min	Typ	Max	Units
t _{PHLD}	Differential Propagation Delay High to Low	R _L = 100Ω, C _L = 50 pF (Figures 2, 3)	6	10.5	16	ns
t _{PLHD}	Differential Propagation Delay Low to High		6	11	16	ns
t _{SKD}	Differential Skew (same channel) t _{PHLD} - t _{PLHD}			0.5	2.0	ns
t _{SK1}	Skew, Pin to Pin (same device)			1.0	2.0	ns
t _{SK2}	Skew, Part to Part (Note 8)			3.0	5.0	ns
t _{TLH}	Differential Transition Time Low to High (20% to 80%)			4.2	10	ns
t _{THL}	Differential Transition Time High to Low (80% to 20%)			4.7	10	ns
t _{PHZ}	Disable Time High to Z	(Figures 4, 5)		12	20	ns
t _{PLZ}	Disable Time Low to Z			9	20	ns
t _{PZH}	Enable Time Z to High			22	32	ns
t _{PZL}	Enable Time Z to Low			22	32	ns
f _{max}	Maximum Operating Frequency (Note 9)		32			MHz

Switching Characteristics - Military (Note 5) (Note 6)

Over supply voltage and -55°C to +125°C operating temperature range, unless otherwise specified

Sym	Parameter	Conditions	Min	Max	Units
t _{PHLD}	Differential Propagation Delay High to Low	R _L = 100Ω, C _L = 50 pF (Figures 2, 3)	5	25	ns
t _{PLHD}	Differential Propagation Delay Low to High		5	25	ns
t _{SKD}	Differential Skew (same channel) t _{PHLD} - t _{PLHD}			5.0	ns
t _{SK1}	Skew, Pin to Pin (same device)			5.0	ns
t _{PHZ}	Disable Time High to Z	(Figures 4, 5)		35	ns
t _{PLZ}	Disable Time Low to Z			35	ns
t _{PZH}	Enable Time Z to High			40	ns
t _{PZL}	Enable Time Z to Low			40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages V_{OD1}, V_{OD2}, V_{OD3}.

Note 3: All typicals are given for V_{CC} = +3.3V, T_A = +25°C.

Note 4: Only one output shorted at a time. The output (true or complement) is configured High.

Note 5: f = 1 MHz, t_r and t_f ≤ 6 ns, 10% to 90%.

Note 6: See TIA/EIA-422-B specifications for exact test conditions.

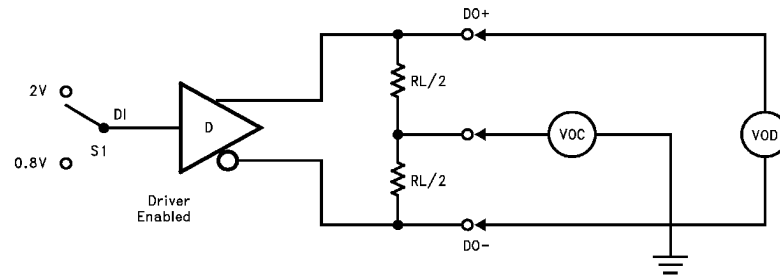
Note 7: This specification limit is for compliance with TIA/EIA-422-B and ITU-T V.11.

Note 8: Devices are at the same V_{CC} and within 5°C within the operating temperature range

Note 9: All channels switching, output duty cycle criteria is 40%/60% measured at 50%. This parameter is guaranteed by design and characterization.

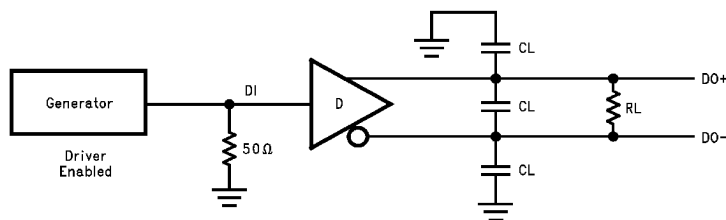
Note 10: This parameter does not meet the TIA/EIA-422-B specification.

Parameter Measurement Information



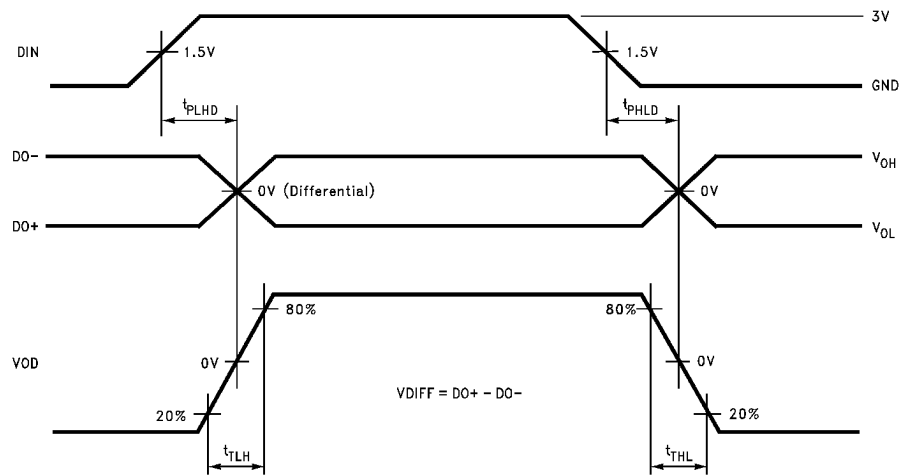
DS012642-2

FIGURE 1. Differential Driver DC Test Circuit



DS012642-3

FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit



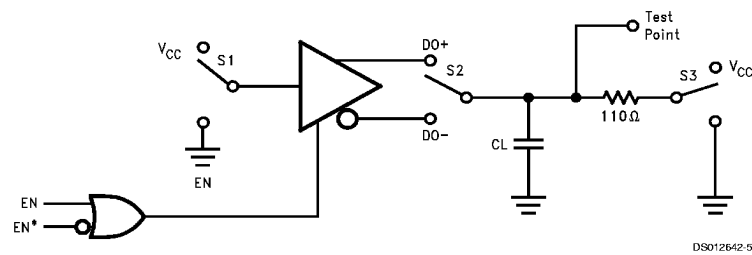
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FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

Note 11: Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}$, Duty Cycle = 50% $Z_o = 50\Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10$.

Note 12: C_L includes probe and fixture capacitance.

Parameter Measurement Information (Continued)



If EN is the input, then EN* = High
If EN* is the input, then EN = Low

FIGURE 4. Driver Single-Ended TRI-STATE Test Circuit

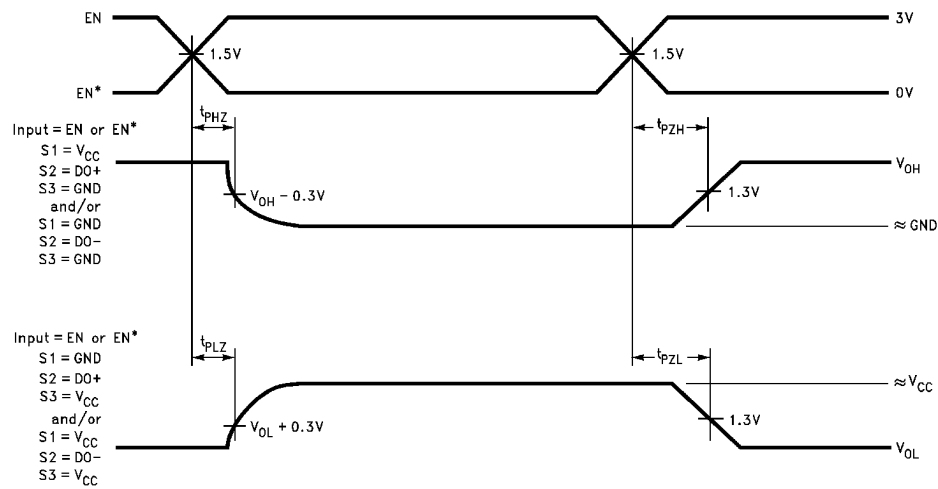


FIGURE 5. Driver Single-Ended TRI-STATE Waveforms

Typical Application Information

General application guidelines and hints for differential drivers and receivers may be found in the following application notes:

AN-214, AN-457, AN-805, AN-847, AN-903, AN-912, AN-916.

Power Decoupling Recommendations:

Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 μF in parallel with 0.01 μF at the power supply pin. A 10 μF or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

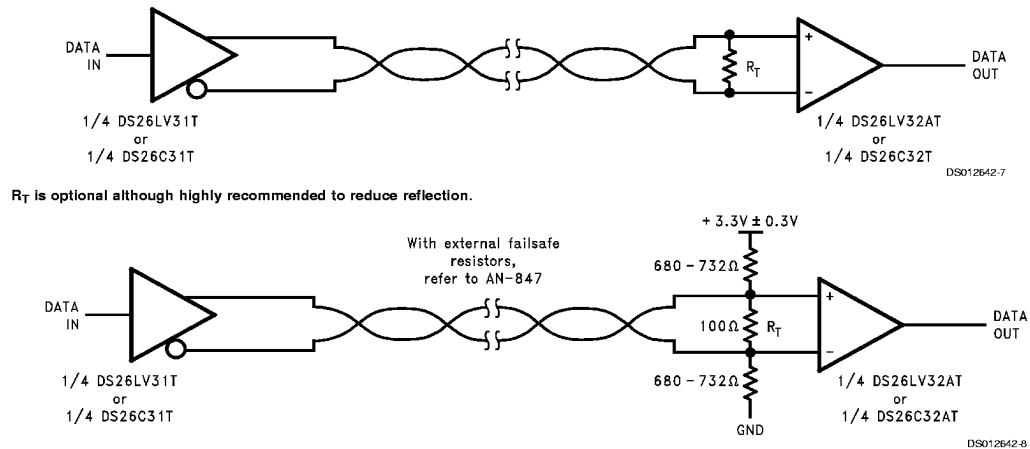


FIGURE 6. Typical Driver Connection

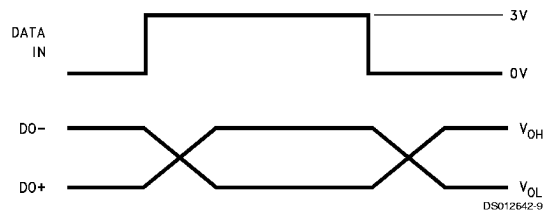
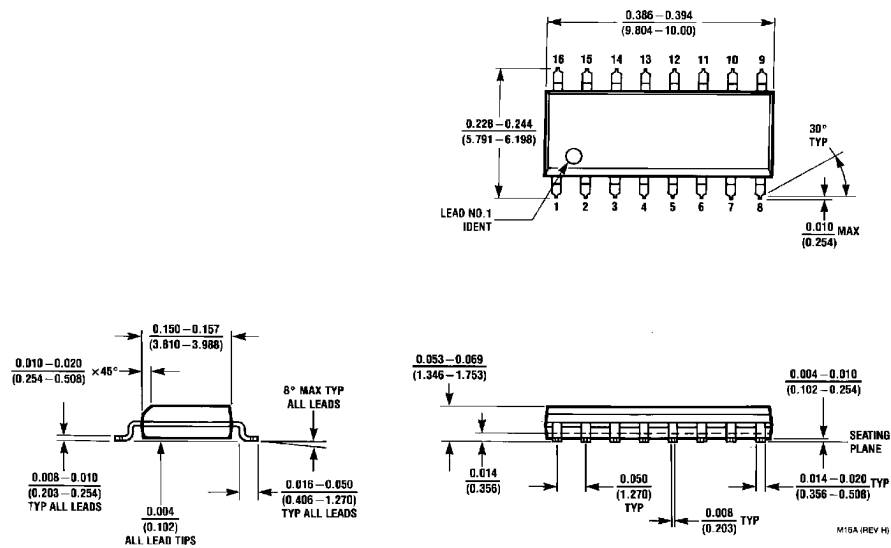


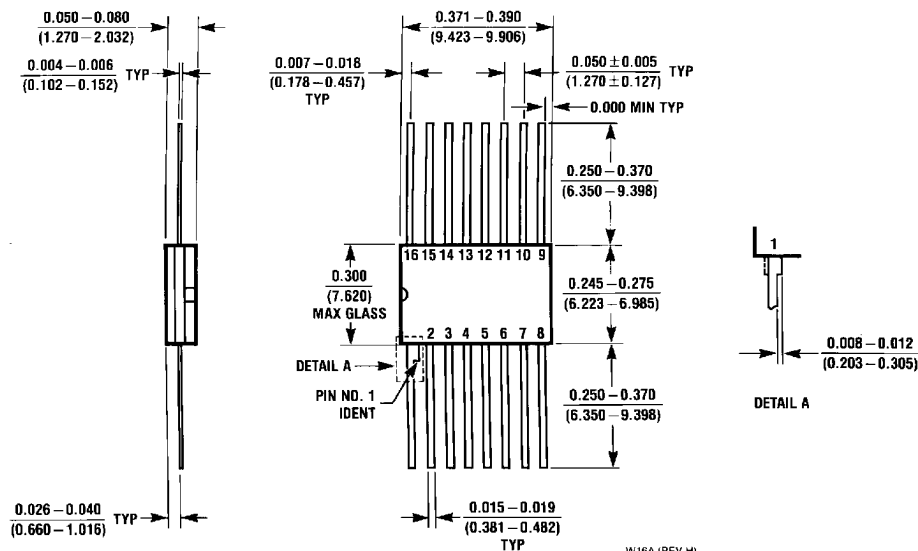
FIGURE 7. Typical Driver Output Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Molded Small Outline Package (M)
Order Number DS26LV31TM
NS Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flatpack (W)
Order Number DS26LV31W
NS Package Number W16A

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