



Ultralow-Drift Op Amp

ANALOG DEVICES INC

AD707

1.1 Scope.

This specification covers the detail requirements for a linear bipolar monolithic low-drift, low offset voltage operational amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD707S(X)/883B
-2	AD707T(X)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-8A	8-Pin Cerdip
H	H-08A	8-Pin TO-99 Metal Can

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

Supply Voltage	$\pm 22\text{V}$
Internal Power Dissipation ¹	500mW
Differential Input Voltage	$\pm V_S$
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	
AD707T, AD707S	-55°C to $+125^\circ\text{C}$
Lead Temperature Range (Soldering 60sec)	$+300^\circ\text{C}$

NOTE

¹Maximum package power dissipation vs. ambient temperature.

Package Type	MAXIMUM AMBIENT	DERATE ABOVE MAXIMUM
	Temperature for Rating	Ambient Temperature
Cerdip (Q)	75°C	$6.7\text{mW}/^\circ\text{C}$
TO-99 (H)	80°C	$7.1\text{mW}/^\circ\text{C}$

1.5 Thermal Characteristics.

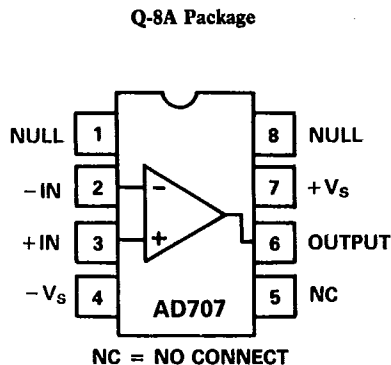
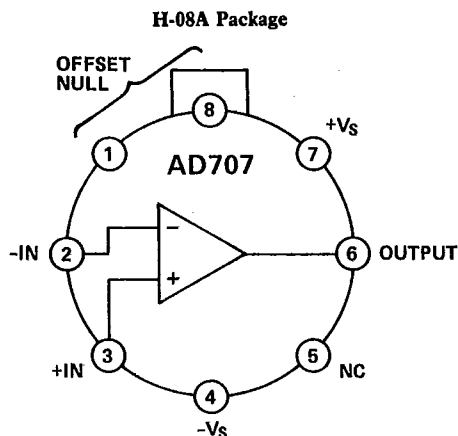
Thermal Resistance θ_{JC}	$= 65^\circ\text{C}/\text{W}$ for H-08A
θ_{JA}	$= 150^\circ\text{C}/\text{W}$ for H-08A
θ_{JC}	$= 22^\circ\text{C}/\text{W}$ for Q-8A
θ_{JA}	$= 110^\circ\text{C}/\text{W}$ for Q-8A

Table 1.

Test	Symbol	Device	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Gain Open Loop	A_{VS}	-1	5000	5000		$R_L \geq 2k\Omega, V_{OUT} = \pm 10V$	V/mV min
			5000			$R_L \geq 1k\Omega, V_{OUT} = \pm 10V$	
		-2	8000	8000		$R_L \geq 2k\Omega, V_{OUT} = \pm 10V$	
			8000			$R_L \geq 1k\Omega, V_{OUT} = \pm 10V$	
Output Voltage Swing	V_{OP}	-1, 2	13.5			$R_L \geq 10k\Omega$	$\pm V$ min
			12.5	12.0		$R_L = 2k\Omega$	
			12.0			$R_L = 1k\Omega$	
Input Offset Voltage	V_{IO}	-1	25	45			$\pm \mu V$ max
		-2	25	25	15		
Input Offset Drift	$\Delta V_{IO}/\Delta T$	-1		0.3			$\pm \mu V/^\circ C$ max
		-2		0.1			
Input Offset Current	I_{IO}	-1	1.5	2.0			$\pm nA$ max
		-2	1.5	1.5	1.0		
Input Bias Current	I_{IB}	-1	1.5	3.0			$\pm nA$ max
		-2	1.5	2.0	1.0		
Common-Mode Rejection Ratio	CMRR	-1, 2	130	130		$V_{CM} = \pm CMVR$	dB min
Common-Mode Voltage Range	CMVR	-1, 2	13	13			$\pm V$ min
Power Supply Current	I_Q	-1, 2	3				mA max
Power Consumption	P_D	-1, 2	90			No Load	mW max
Power Supply Rejection Ratio	PSRR	-1	115	115		$\pm 3 \leq V_S \leq \pm 18$	dB min
		-2	115	120	120		

NOTE

¹ $V_S = \pm 15$, unless otherwise noted.

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3.2.1 Functional Block Diagram and Terminal Assignments.

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

