

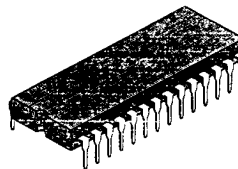
10 bit 30 MSPS D/A Converter

Description

CX20051A is 10 bit, 30 MSPS D/A Converter, designed for a video signal processing. The broadcasting application will require the fairly high resolution for D/A. CX20051A is suitable for the high definition TV application, too.

The external resistor can control the voltage output range of the D/A. The CX20051A requires $-5V$ single power supply, the ECL digital inputs, and the differential ECL clocks, to operate.

28 pin DIP (Plastic)



Features

- Maximum conversion frequency 30 MSPS
- High resolution 10 bit
- Low power consumption 550 mW
- $-5V$ single power supply
- Clock input and digital input are in ECL level

Structure

Bipolar silicon monolithic IC.

Block Diagram and Pin Connection

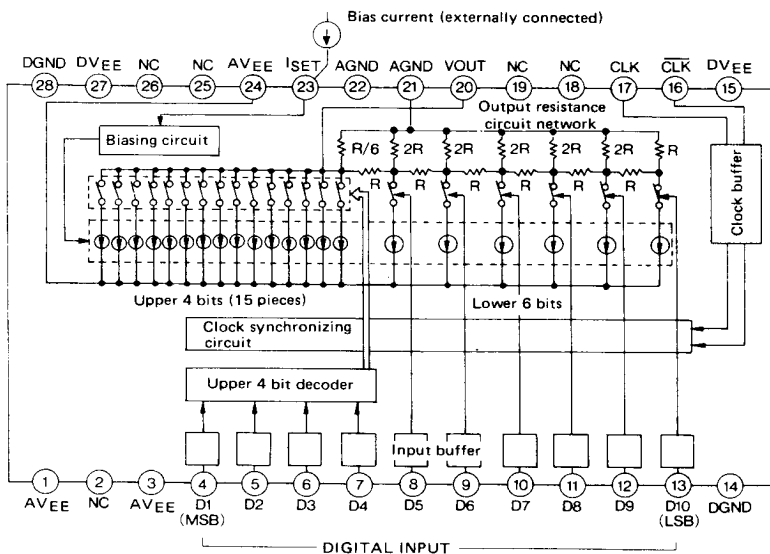


Fig. 1

Absolute Maximum Ratings (Ta=25°C)

• Supply voltage	V_{EE}	-12	V
• Digital input voltage	V_{IH}	V_{EE} to 0	V
• Operating temperature	T_{opr}	-10 to +70	°C
• Storage temperature	T_{stg}	-50 to +150	°C
• Allowable power dissipation		1.47	W

Recommended Operating Conditions

• Supply voltage	V_{EE}	-5.0 ± 0.25	V
• Digital input voltage	V_{IH}	-0.89 ± 0.15	V
	V_{IL}	-1.75 ± 0.15	V
• Dynamic range	V_o	-1.5 to -0.5	V
• Bias current	I_{SET}	1.0 ± 0.5	mA

Pin Description

No.	Symbol	Description	Equivalent circuit
1	D V_{EE}	Digital V_{EE} power supply (-5V)	
2	NC	Non-connection	
3	D V_{EE}	Digital V_{EE} power supply (-5V)	
4	NSB	10-bit digital input (MSB: Uppermost order) (LSB: Lower most order)	
5	BIT2		
6	BIT3		
7	BIT4		
8	BIT5		
9	BIT6		
10	BIT7		
11	BIT8		
12	BIT9		
13	LSB		
14	D GND	Digital GND	
15	D V_{EE}	Digital V_{EE} power supply (-5V)	

No.	Symbol	Description	Equivalent circuit
16	$\overline{\text{CLK}}$	Clock bar input	
17	CLK	Clock input	
18	NC	Non-connection	
19	NC		
20	OUT	D/A output	
21	A GND	Analog GND Directly connected to the output resistance circuit network (R_{OUT})	
22	A GND	Analog GND For analog circuit system other than the output resistance circuit network	
23	ISET	Dynamic range adjusting pin	
24	A VEE	Analog VEE power supply (-5V)	
25	NC	Non-connection	
26	NC		
27	D VEE	Digital VEE power supply (-5V)	
28	D GND	Digital GND	

Electrical Characteristics

(Ta=25°C AGND=DGND=0V, AV_{EE}=DV_{EE}=-5V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential linearity	D.L.	*1	-0.8	0	0.8	LSB
Maximum operating clock frequency	f _{MAX}	*2	30			MHz
Differential gain	D.G.	NTSC 40IRE mod. ramp f _{CLK} =14.3 MHz		0.7		%
Differential phase	D.P.			0.2		deg
Circuit current	I _{EE}		88	110	132	mA
Output impedance	R _{OUT}		52	62	72	Ω
Input current	I _{IH}	Measured in the high level input voltage of the individual pins 4 to 13	1	3	10	μA
Input current	I _{IL}	Measured in the low level input voltage of the individual pins 4 to 13	0	20	300	nA

Note) As for the test circuit, see Fig. 2a to 2d.

*1 Input signal is digital ramp with 1 MHz clock.

Glitches are not the subject of the measurement.

*2 The maximum operating clock frequency which shows no bit error. Input signal is digital ramp.

Glitches are not the subject of the measurement.

Electrical Characteristics Test Circuit

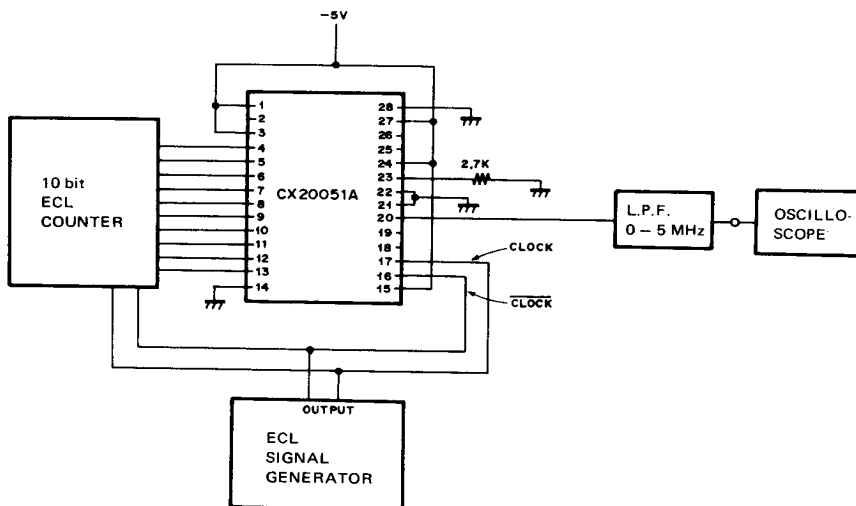


Fig. 2a Block diagram of differential linearity and maximum operating frequency test circuit

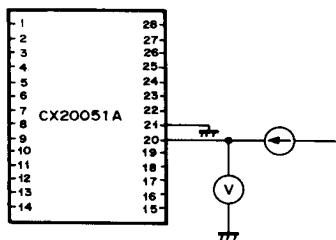


Fig. 2b Block diagram of output impedance test circuit

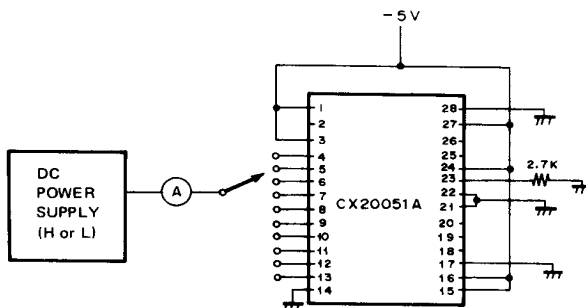


Fig. 2c Block diagram of input current test circuit

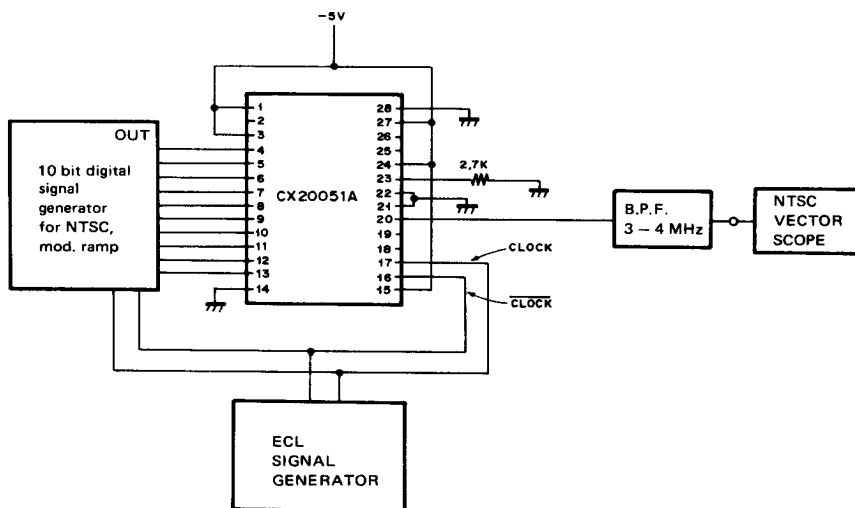


Fig. 2d Block diagram of DG and DP test circuit

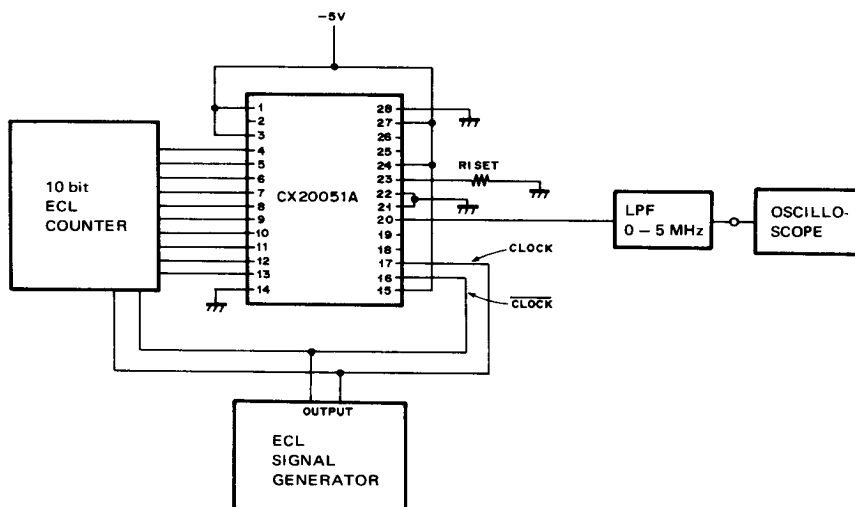


Fig. 2e Block diagram of dynamic range test circuit

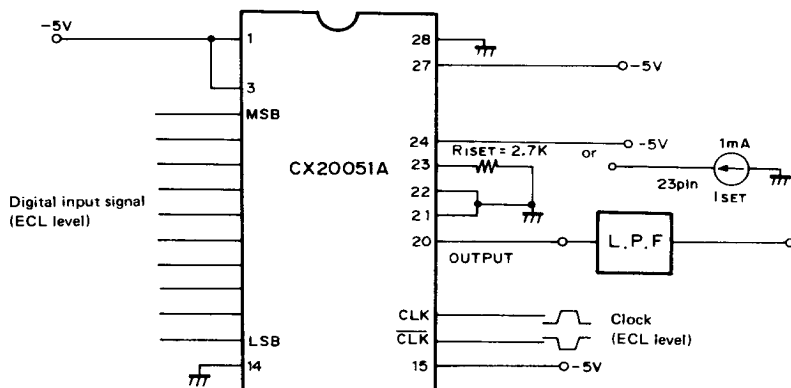


Fig. 3 Typical circuit connection

When changing the dynamic range of the output, change the value of R or the constant current supply value when a constant current supply is inserted in place of R. Both input and clock are in ECL level. Regarding the clock waveform, see the Note on Application.

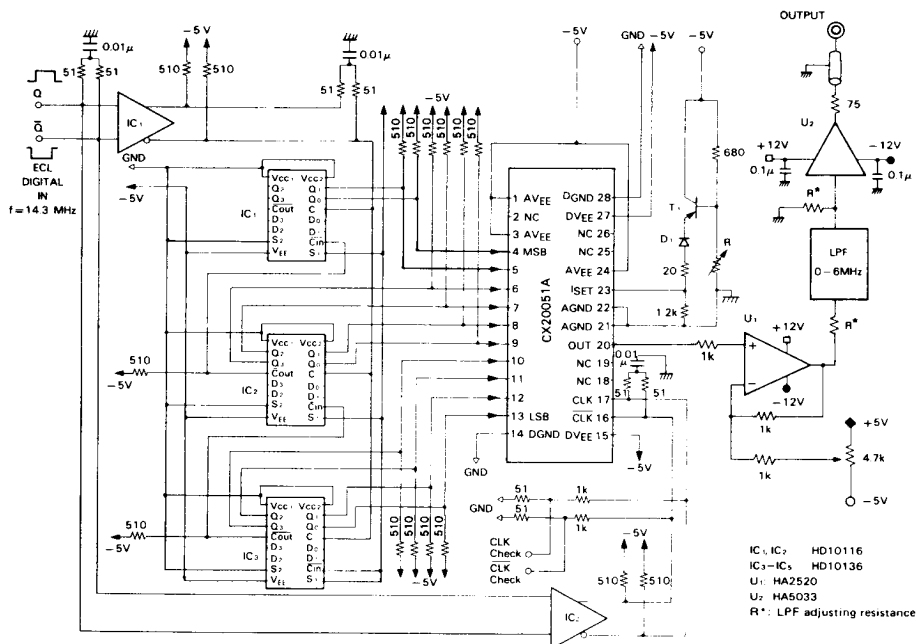


Fig. 4 Application circuit

Note on Application

(1) Applying clocks

- (a) To pins 16 and 17, clock signals denoted as $\overline{\text{CLOCK}}$ and CLOCK are to be fed respectively. Both of their levels are ECL compatible levels.

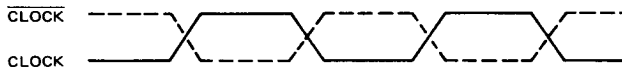


Fig. 5a CLOCK and $\overline{\text{CLOCK}}$ waveforms

- (b) Alternatively single-end method is usable to apply clock signal to the device. A clock signal of ECL level is to be fed to one of pin 16 or pin 17, with the other pin fixed to the ECL threshold level.

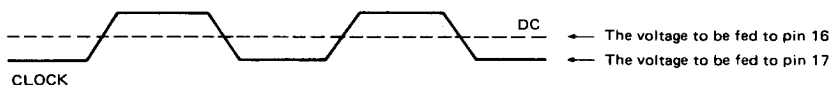
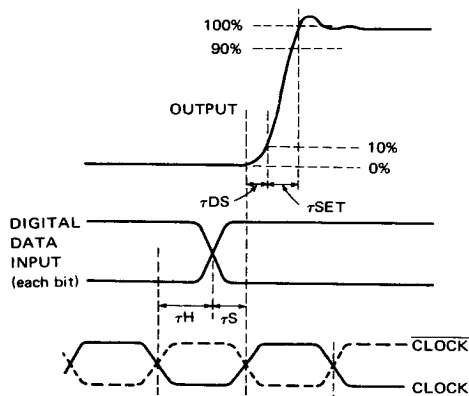


Fig. 5b Single-end method

(2) Timing chart

The timing between the CLOCK signal and 10 bit Digital Data Input signal is shown in the diagram below.



(Recommended operating condition)

$$\tau_H > 2 \text{ ns}$$

$$\tau_S > 10 \text{ ns}$$

The typical values of τ_{DS} and τ_{SET} under the above-mentioned condition are

$$\tau_{DS} \approx 7 \text{ ns}$$

$$\tau_{SET} \approx 4 \text{ ns}$$

for Z_L (load resistance) $> 10 \text{ k}\Omega$

Fig. 5c Timing chart

(3) Dynamic range (ISET pin, pin 23)

Dynamic range can be determined by connecting an external resistor (R_{SET}) between the ISET pin (pin 23) and the A GND pin (pin 22), or by applying a current source (ISET) to the ISET pin (pin 23). Typical values to obtain 1V of dynamic range are $2.7 \text{ k}\Omega$ and 1 mA , for R_{SET} and ISET respectively (for a load resistance $Z_L > 10 \text{ k}\Omega$). (See the Dynamic range vs. R_{SET} on page 193.)

(4) Input coding

STEPS	DIGITAL INPUT	ANALOG OUTPUT	
		CASE ①	CASE ②
0000	MSB1111111111LSB	-0.003V	-0.003V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
0511	1000000000	-0.4825V	-0.503V
0512	0111111111	-0.4835V	-0.504V
0513	0111111110	-0.4844V	-0.505V
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
1023	0000000000	-0.963V	-1.003V

CASE ① : $R_{SET}=2.7\text{ k}\Omega$

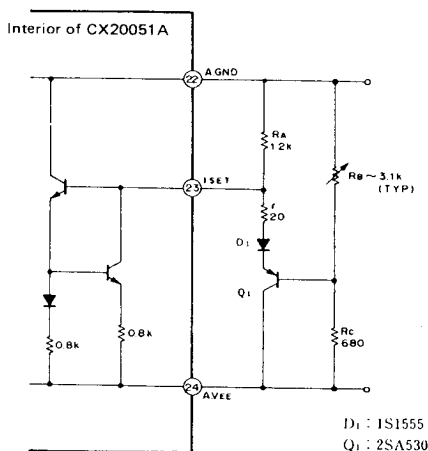
(Output voltage is typical value.)

CASE ② : R_{SET} is adjusted to obtain 1.000V full scale of analog output voltage.

(5) Temperature fluctuation compensation method of D/A output voltage dynamic range

When the temperature fluctuation of the output voltage dynamic range poses a problem, a simple temperature compensation can be performed by adding a simple circuit externally.

Connecting diagram of the external circuit for temperature compensation is shown below. In this way, the temperature fluctuation may be limited to within $\pm 150\text{ ppm}/^\circ\text{C}$.



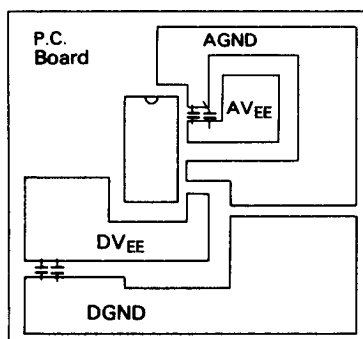
- (6) When the analog output level is at full scale 1 Vp-p, the 1LSB becomes approximately 1 mV. In order to obtain the predesignated characteristics, due care should be exercised in the designing of the CX20051A periphery circuit.

[Note on mounting onto the printed board]

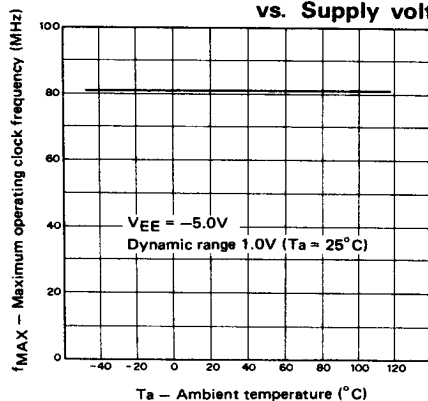
The external connection diagram of CX20051A is basically as shown in Fig. 3. In this regard, take note to the points mentioned below.

- (1) AGND and DGND as also AV_{EE} and DV_{EE} are not connected internally. It is also desired to separate the analog block and digital block externally.
- (2) Take as much space as possible of the ground surface on the printed board to reduce parasitic inductance and resistance.
- (3) Insert a 47 μ F tantalum capacitor and a 1000 pF ceramic capacitor in parallel between the V_{EE} surface and the ground surface most adjacent to it on the printed board and reduce the noise. In addition, it is also desired to insert a capacitor between the V_{EE} surface and the GND surface near the IC. (See Fig. below)

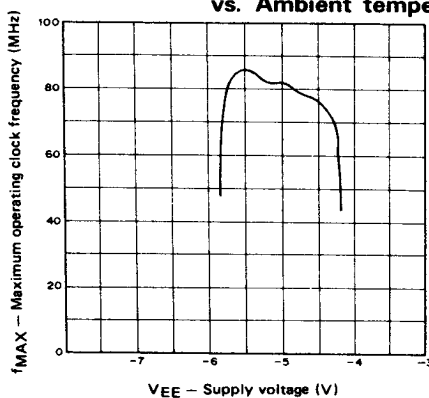
GND and V_{EE} pattern arrangement



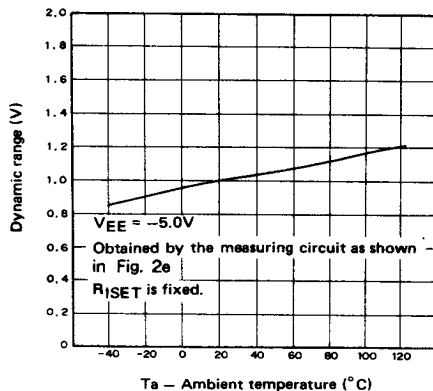
**Maximum operating clock frequency
vs. Supply voltage**



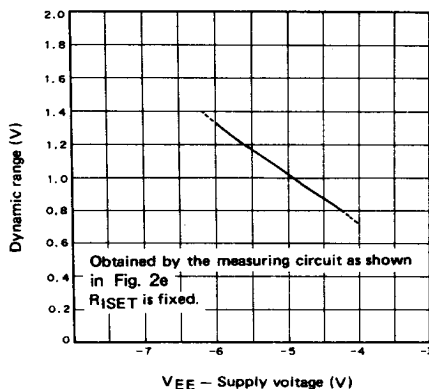
**Maximum operating clock frequency
vs. Ambient temperature**



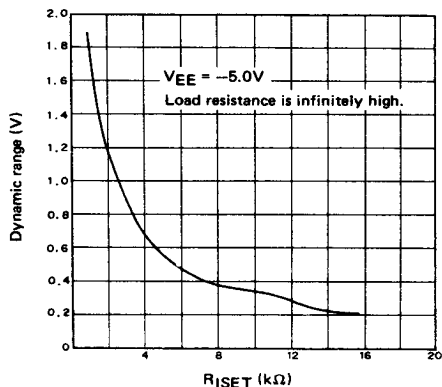
Dynamic range vs. Ambient temperature



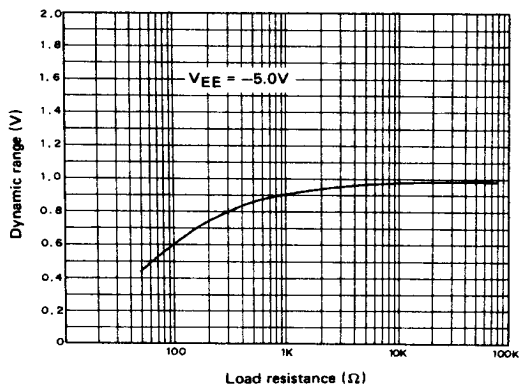
Dynamic range vs. Supply voltage

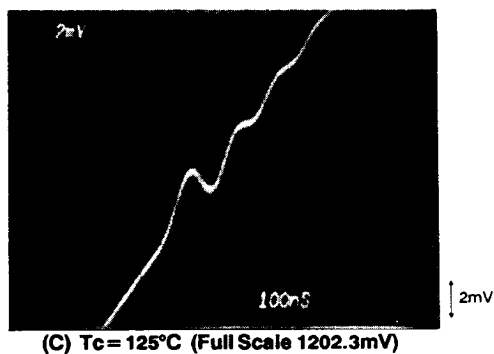
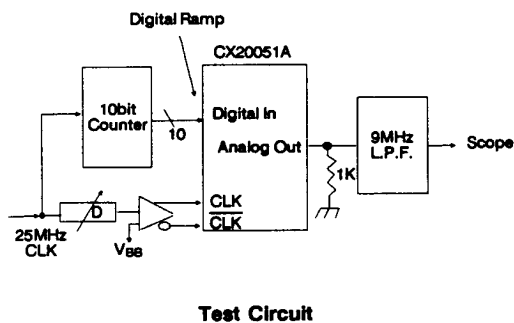
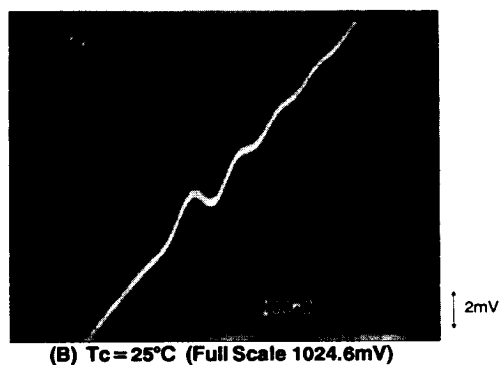
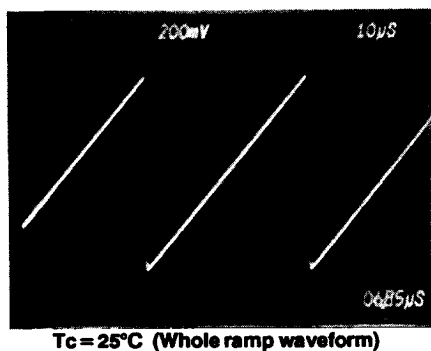
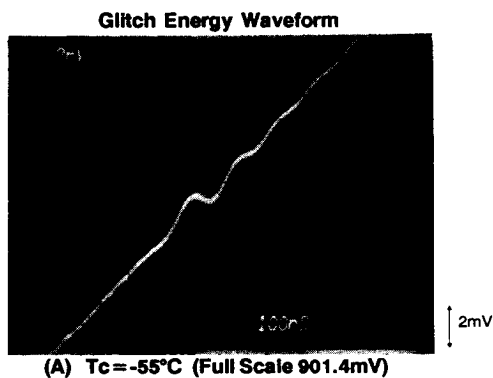
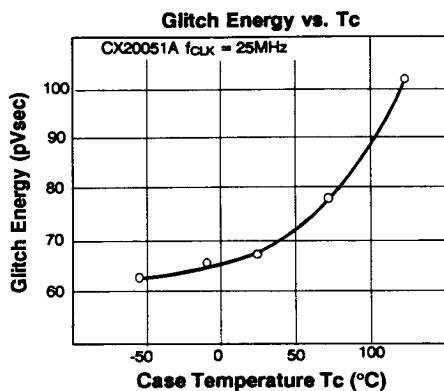


Dynamic range vs. R_{1SET}



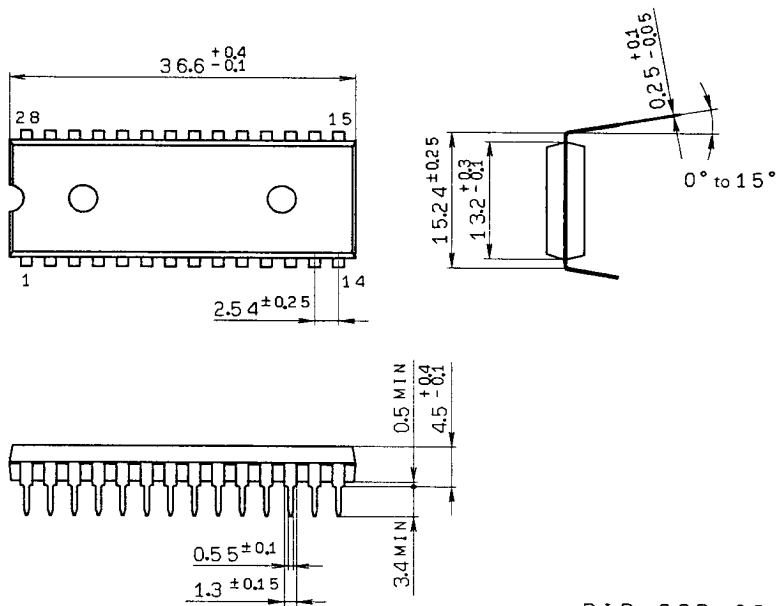
Dynamic range vs. Load resistance





Package Outline Unit : mm

CX20051A 28 pin DIP (Plastic) 600mil 4.0g



DIP-28P-02