

74ACT841

10-Bit Transparent Latch with TRI-STATE® Outputs

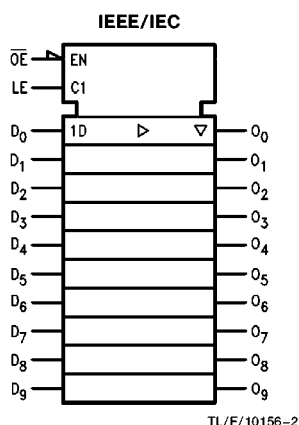
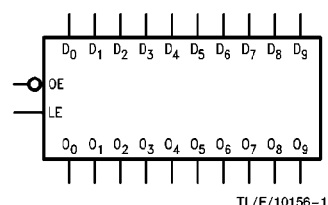
General Description

The 'ACT841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'ACT373.

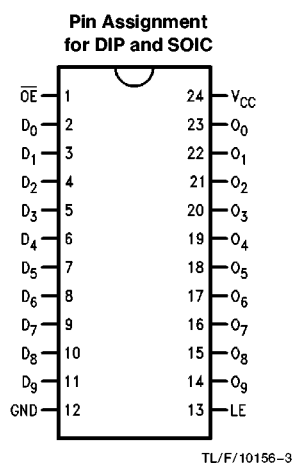
Features

- 'ACT841 has TTL-compatible inputs
- Outputs source/sink 24 mA
- Non-inverting TRI-STATE outputs

Logic Symbols



Connection Diagram



Pin Names	Description
D ₀ –D ₉	Data Inputs
O ₀ –O ₉	TRI-STATE Outputs
$\overline{OE}$	Output Enable
LE	Latch Enable

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Functional Description

The ACT841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

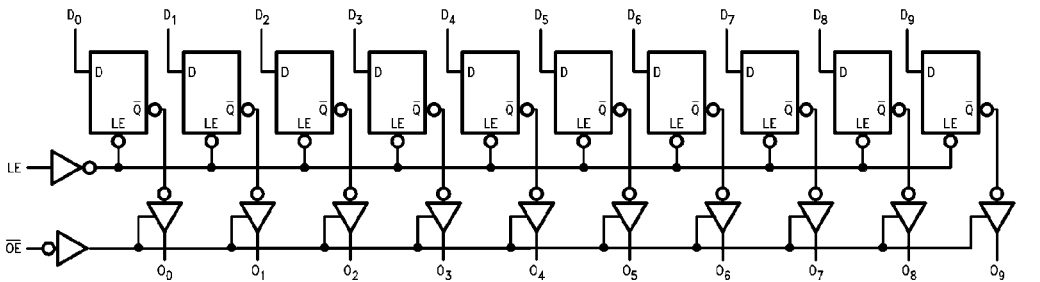
On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
X	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 NC = No Change

Logic Diagram



TL/F/10156-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
*ACT	
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT	−40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
*ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for *ACT Family Devices

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I _{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.76 4.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I _{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.44 0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V _I = V _{CC} , GND
I _{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.5	±5.0	μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	μA	V _I = V _{CC} − 2.1V

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT	Units	Conditions
			T _A = +25°C		T _A = −40°C to +85°C		
			Typ	Guaranteed Limits			
I _{OLD}	‡Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	V _{IN} = V _{CC} or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Units
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay D _n to O _n	5.0	2.0	5.5	9.5	2.0	10.0	ns
t _{PHL}	Propagation Delay D _n to O _n	5.0	2.0	5.5	9.5	2.0	10.0	ns
t _{PLH}	Propagation Delay LE to O _n	5.0	2.0	5.5	9.0	2.0	10.0	ns
t _{PHL}	Propagation Delay LE to O _n	5.0	2.0	5.5	9.0	2.0	10.0	ns
t _{PZH}	Output Enable Time OE to O _n	5.0	2.0	5.5	9.5	2.0	10.5	ns
t _{PZL}	Output Enable Time OE to O _n	5.0	2.0	5.5	9.5	2.0	10.5	ns
t _{PHZ}	Output Disable Time OE to O _n	5.0	2.0	6.0	10.5	2.0	11.0	ns
t _{PLZ}	Output Disable Time OE to O _n	5.0	2.0	6.0	10.5	2.0	11.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT	Units
			T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	−0.5	0.5	1.0	ns
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	0.5	2.0	2.0	ns
t _w	LE Pulse Width, HIGH	5.0	2.0	3.5	3.5	ns

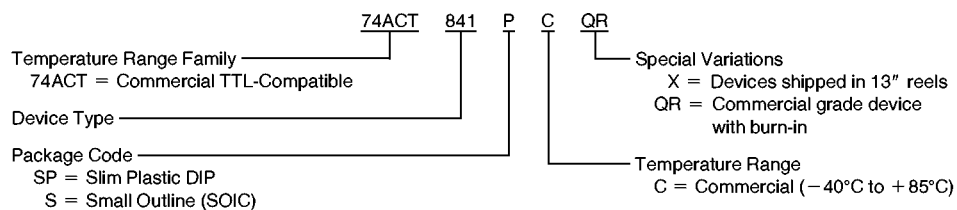
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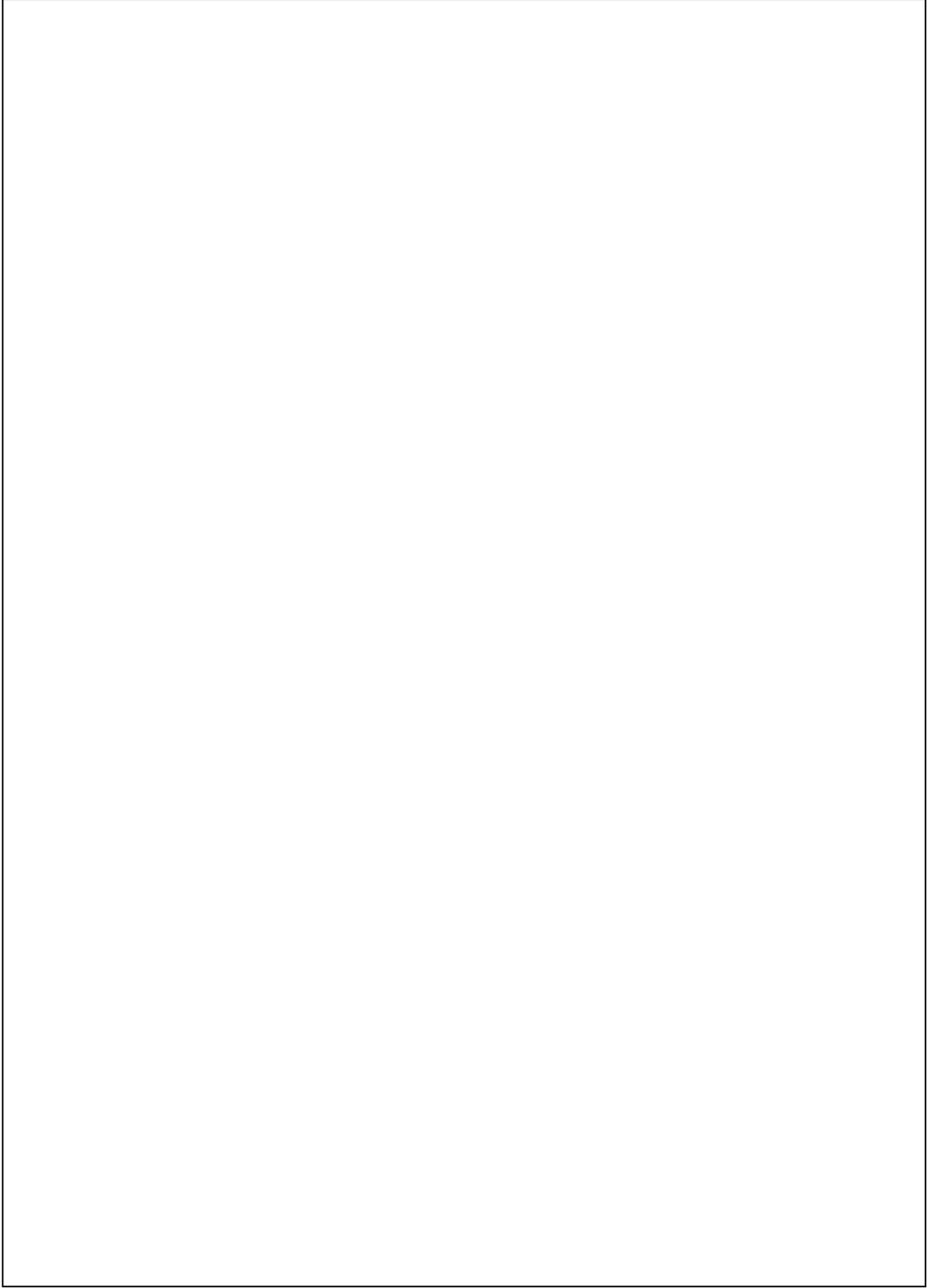
Capacitance

Symbol	Parameter	AC/ACT	Units	Conditions
		Typ		
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	44	pF	V _{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:





Top View Dimensions:

- Pin 1 Identification: 0.1043, 0.0926, 2.65, 2.35
- Pin 1 to Pin 12: 0.014, 0.35
- Pin 12 to Pin 24: 0.0118, 0.3, 0.1
- Pin 24 to Pin 1: 0.6141, 0.5985, 15.60, 15.20
- Pin 1 to Pin 2: 0.050, 1.27
- Pin 12 to Pin 13: 0.0200, 0.0138, 0.508, 0.350
- Pin 13 to Pin 24: 0.2992, 0.2914, 7.6, 7.4
- Pin 13 to Pin 1: 0.4190, 0.3940, 10.65, 10.00

Side View Dimensions:

- Seating Plane to Pin 1: 0.014, 0.35
- Seating Plane to Pin 12: 0.0118, 0.3, 0.1

Detail View Dimensions:

- Lead Tip: 0.004, 0.1
- Lead Width: 0.029, 0.010, 0.75, 0.25
- Lead Angle: 45°
- Lead Spacing: 0.0125, 0.0091, 0.32, 0.23
- Lead Tip to Lead Base: 0.0500, 0.0160, 1.27, 0.40
- Lead Tip to Lead Base: 8° MAX TYP- ALL LEADS

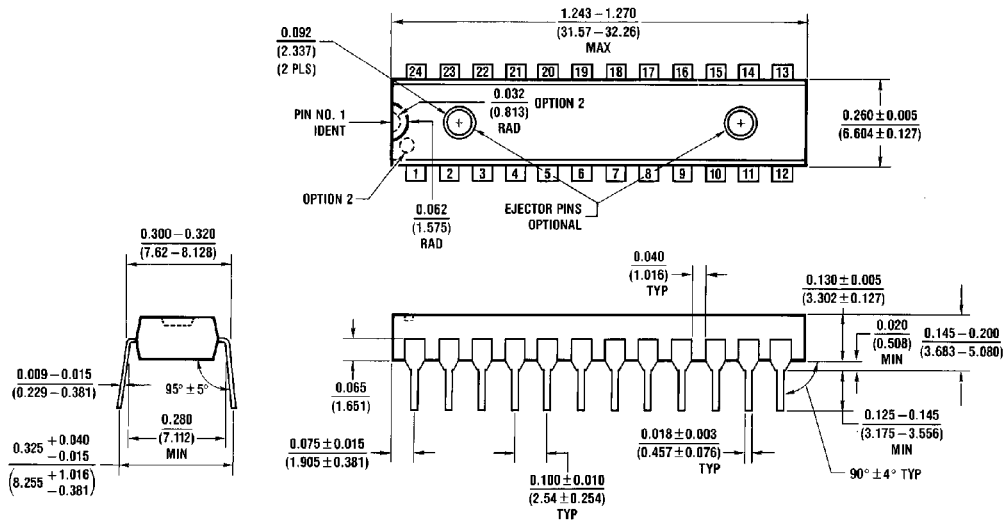
Marking:

- Pin 1 Identification: 1
- Pin 12 to Pin 13: TYP
- Pin 13 to Pin 24: M A C S B

M24B (REV F)

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114850



24 Lead Slim (0.300" Wide) Plastic Dual-In-Line Package (SP)
NS Package Number N24C

N24C (REV F)

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