

# 4.5V Drive Nch MOSFET

# RMW280N03

#### Structure

Silicon N-channel MOSFET

#### ● Features

- 1) High Power package(PSOP8).
- 2) High-speed switching, Low On-resistance.
- 3) Low voltage drive(4.5V drive).

#### Application

Switching

#### Packaging specifications

	Package	Taping	
Type	Code	TB	
	Basic ordering unit (pieces)	2500	
RMW280N	0		

# ● Absolute maximum ratings (Ta = 25°C)

Parame	Symbol	Limits	Unit	
Drain-source voltage		$V_{DSS}$	30	V
Gate-source voltage		$V_{GSS}$	±20	V
Drain current	Continuous	I <sub>D</sub>	±28	Α
	Pulsed	I <sub>DP</sub> *1	±112	Α
Source current	Continuous	I <sub>S</sub>	2.5	Α
(Body Diode)	Pulsed	I <sub>SP</sub> *1	112	Α
Power dissipation		P <sub>D</sub> *2	3.0	W
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	-55 to +150	°C

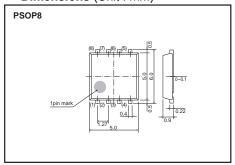
<sup>\*1</sup> Pw $\leq$ 10 $\mu$ s, Duty cycle $\leq$ 1%

#### Thermal resistance

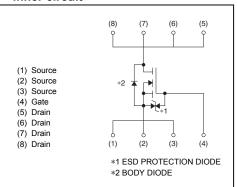
Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-a)*	41.7	°C / W

<sup>\*</sup> MOUNTED ON 40mm × 40mm Cu BOARD

#### • Dimensions (Unit : mm)



#### • Inner circuit



<sup>\*2</sup> MOUNTED ON 40mm × 40mm Cu BOARD

# ● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	1	-	±10	μA	$V_{GS}=\pm20V$ , $V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	1	-	<b>V</b>	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	1	1	1	μA	$V_{DS}$ =30V, $V_{GS}$ =0V
Gate threshold voltage	V <sub>GS (th)</sub>	1.0	1	2.5	<b>V</b>	$V_{DS}$ =10V, $I_{D}$ =1mA
Static drain-source on-state	R <sub>DS (on)</sub> *	1	2.0	2.8	mΩ	I <sub>D</sub> =28A, V <sub>GS</sub> =10V
resistance	US (on)	1	2.7	3.8		I <sub>D</sub> =28A, V <sub>GS</sub> =4.5V
Forward transfer admittance	IY <sub>fs</sub> I*	25	1	-	S	I <sub>D</sub> =28A, V <sub>DS</sub> =10V
Input capacitance	C <sub>iss</sub>	1	3130	-	pF	V <sub>DS</sub> =15V
Output capacitance	C <sub>oss</sub>	1	940	-	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	C <sub>rss</sub>	1	350	-	pF	f=1MHz
Turn-on delay time	t <sub>d(on)</sub> *	1	24	-	ns	I <sub>D</sub> =14A, V <sub>DD</sub> ≒15V
Rise time	t <sub>r</sub> *	1	81	-	ns	V <sub>GS</sub> =10V
Turn-off delay time	t <sub>d(off)</sub> *	ı	94	-	ns	$R_L$ =1.07 $\Omega$
Fall time	t <sub>f</sub> *	i	50	-	ns	$R_G$ =10 $\Omega$
Total gate charge	Q <sub>g</sub> *	-	53	_	nC	I <sub>D</sub> =28A, V <sub>DD</sub> ≒15V
Gate-source charge	Q <sub>gs</sub> *	-	10	-	nC	V <sub>GS</sub> =10V
Gate-drain charge	Q <sub>gd</sub> *	-	11	-	nC	

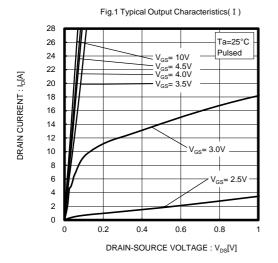
<sup>\*</sup>Pulsed

# ●Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward Voltage	V <sub>SD</sub> *	-	-	1.2	V	I <sub>s</sub> =2.5A, V <sub>GS</sub> =0V

<sup>\*</sup>Pulsed

#### ●Electrical characteristic curves (Ta=25°C)





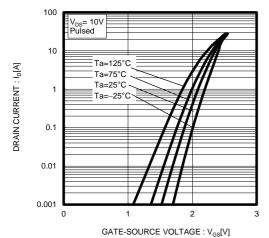


Fig.5 Static Drain-Source On-State

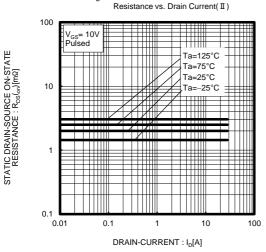


Fig.2 Typical Output Characteristics( II )

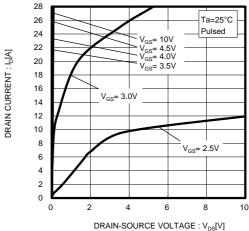


Fig.4 Static Drain-Source On-State

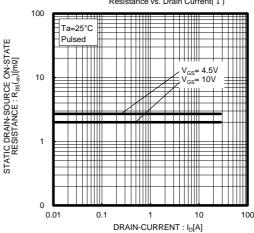
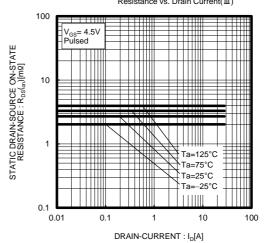


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)



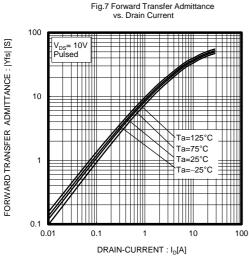


Fig.9 Static Drain-Source On-State
Resistance vs. Gate Source Voltage

15

Ta=25°C
Pulsed

I<sub>D</sub>= 14.0A

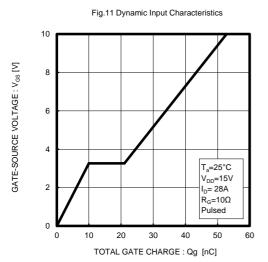
I<sub>D</sub>= 28.0A

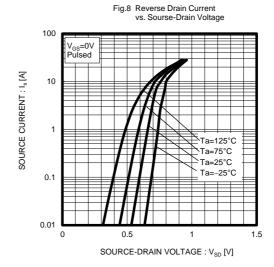
0

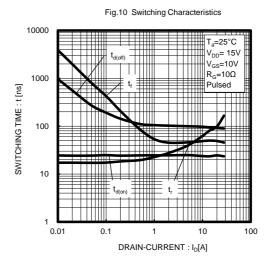
10

GATE-SOURCE VOLTAGE : V<sub>GS</sub>[V]

15







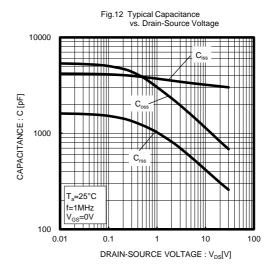


Fig.13 Maximum Safe Operating Aera 1000 Operation in this area is limited by R<sub>DS(ON</sub> (V<sub>GS</sub>=10V) 100 DRAIN CURRENT: I<sub>D</sub> (A) 10 P<sub>W</sub>=1ms 111111  $P_W = 10ms$ 0.1 DC operation T<sub>a</sub> = 25°C 0.01 Single Pulse Mounted on a COPPER board 0.001 10 0.1 100 DRAIN-SOURCE VOLTAGE :  $V_{DS}[V]$ 

NORMARIZED TRANSIENT THERMAL

Ta = 55°C
Single Pulse : 1 Unit
Rth(ch-a)(t) = r(t)×Rth(ch-a)
Rth(ch-a) = 41.7 °C/W

Mounted on a COPPER board>

Fig.14 Normalized Transient Thermal Resistance vs. Pulse Width

PULSE WIDTH: Pw(s)

#### Measurement circuits

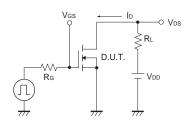


Fig.1-1 Switching Time Measurement Circuit

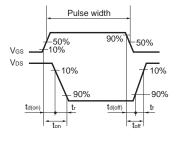


Fig.1-2 Switching Waveforms

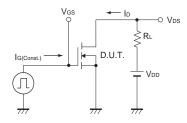


Fig.2-1 Gate Charge Measurement Circuit

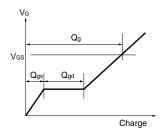


Fig.2-2 Gate Charge Waveform

#### Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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