

10 - 50 MHz Channel Link III Serializer and Deserializer with Embedded Bi-Directional Control Channel

General Description

The DS92LX2121/DS92LX2122 chipset offers a Channel Link III interface to deliver clock, high-speed data and a low-speed, bidirectional I²C control bus over a single twisted wire pair. This single serial stream simplifies transferring a wide data bus over PCB traces and cable by eliminating clock to data skew, while reducing cable width and connector size. The DS92LX2121/DS92LX2122 incorporates differential signaling on both the high-speed and bi-directional back channel control data paths.

The Serializer/ Deserializer pair is ideally suited for driving video data with up to 18-bit color depth (RGB666 + HS, VS, and DE) along with a bi-directional back channel control bus.

In addition, the Deserializer provides input equalization to compensate for loss from the media over longer distances. Internal DC balanced encoding/decoding is used to support AC-Coupled interconnects. Deserializer features such as output slew rate control, spread spectrum clock generation and staggered outputs can be enabled to lower EMI.

A sleep function provides a power-savings mode when the high speed forward channel and embedded bi-directional control channel are not needed.

The Serializer is offered in a 40-pin lead in LLP and Deserializer is offered in a 48-pin LLP packages.

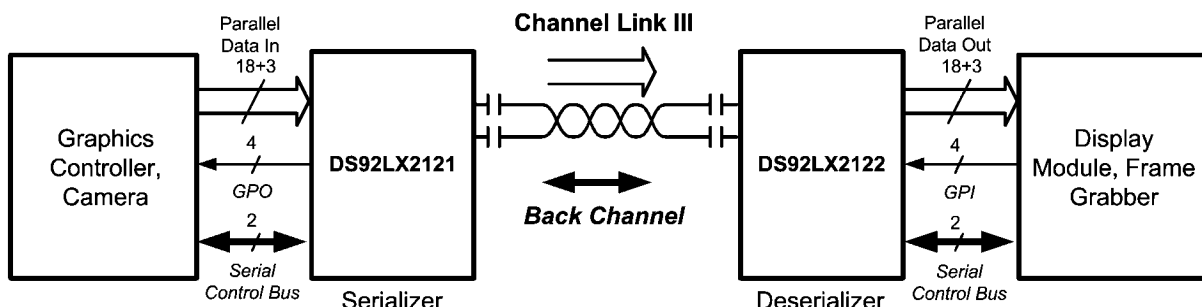
Features

- Up to 1050 Mbts/sec data throughput
- 10 MHz to 50 MHz input clock support
- Supports 18-bit color depth (RGB666 + HS, VS, DE)
- Embedded clock with DC Balanced coding to support AC-coupled interconnects
- Capable to drive up to 10 meters shielded twisted-pair
- Bi-directional control interface channel with I²C support
- I²C interface for device configuration. Single-pin ID addressing
- Up to 4 GPI on DES and GPO on SER
- AT-SPEED BIST diagnosis feature to validate link integrity
- Individual power-down controls for both SER and DES
- User-selectable clock edge for parallel data on both SER and DES
- Integrated termination resistors
- 1.8V- or 3.3V-compatible parallel bus interface
- Single power supply at 1.8V
- IEC 61000-4-2 ESD compliant
- Temperature range -40°C to +85°C
- No reference clock required on Deserializer
- Programmable Receive Equalization
- LOCK output reporting pin to ensure
- EMI/EMC Mitigation
 - DES Programmable Spread Spectrum (SSCG) outputs
 - DES Receiver Output clock and data slew rate select
 - DES Receiver staggered outputs

Applications

- Industrial Displays, Touch Screens
- Medical Imaging

Typical Application Diagram



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Block Diagrams

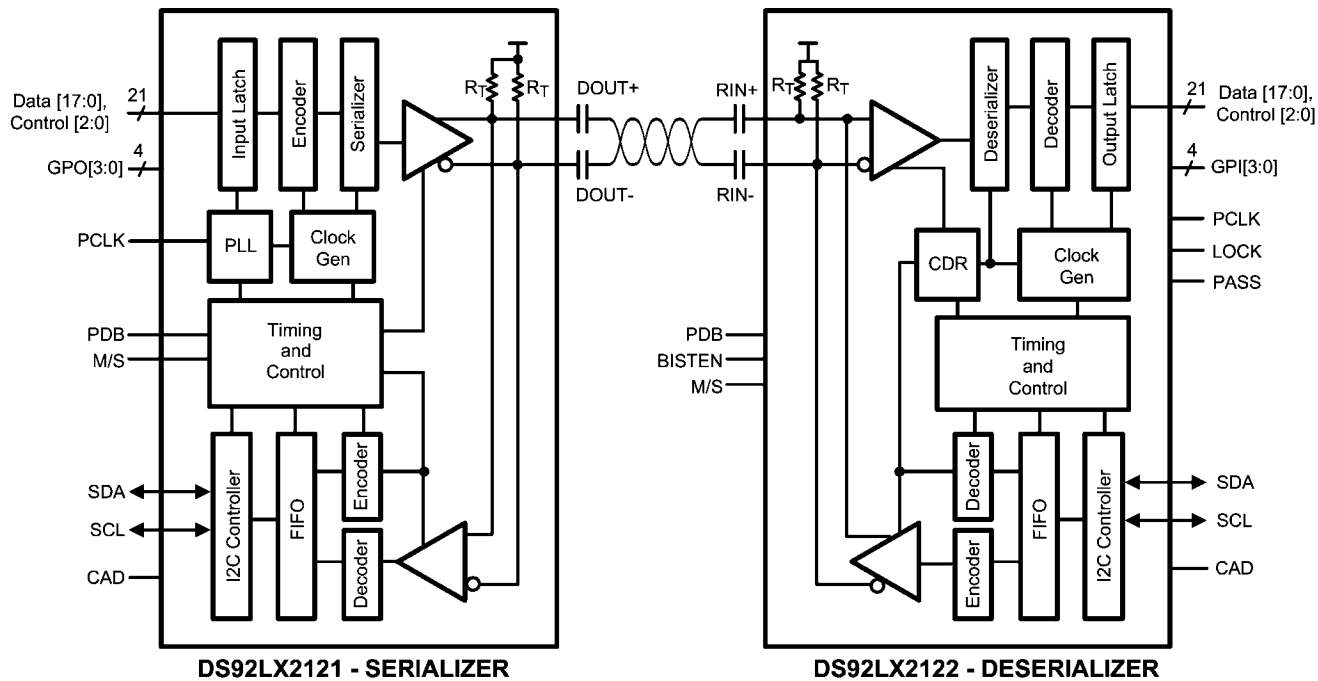


FIGURE 1. Block Diagram

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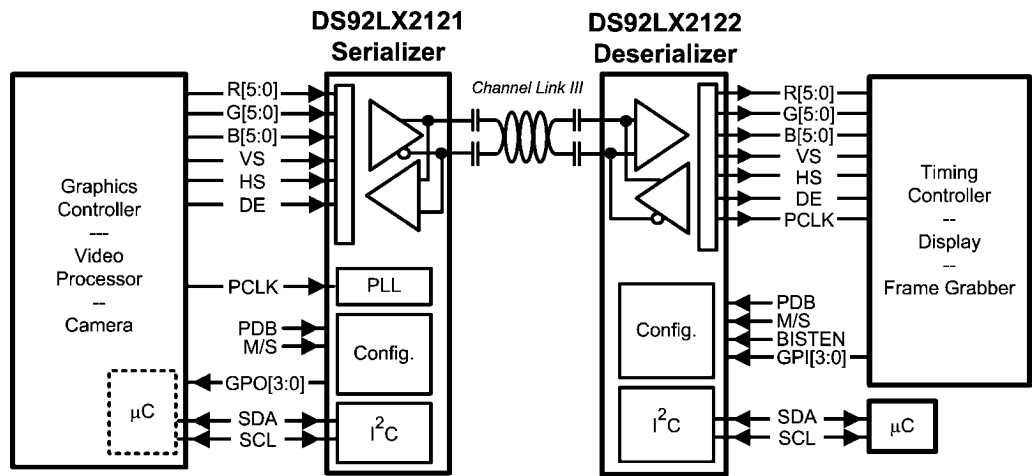
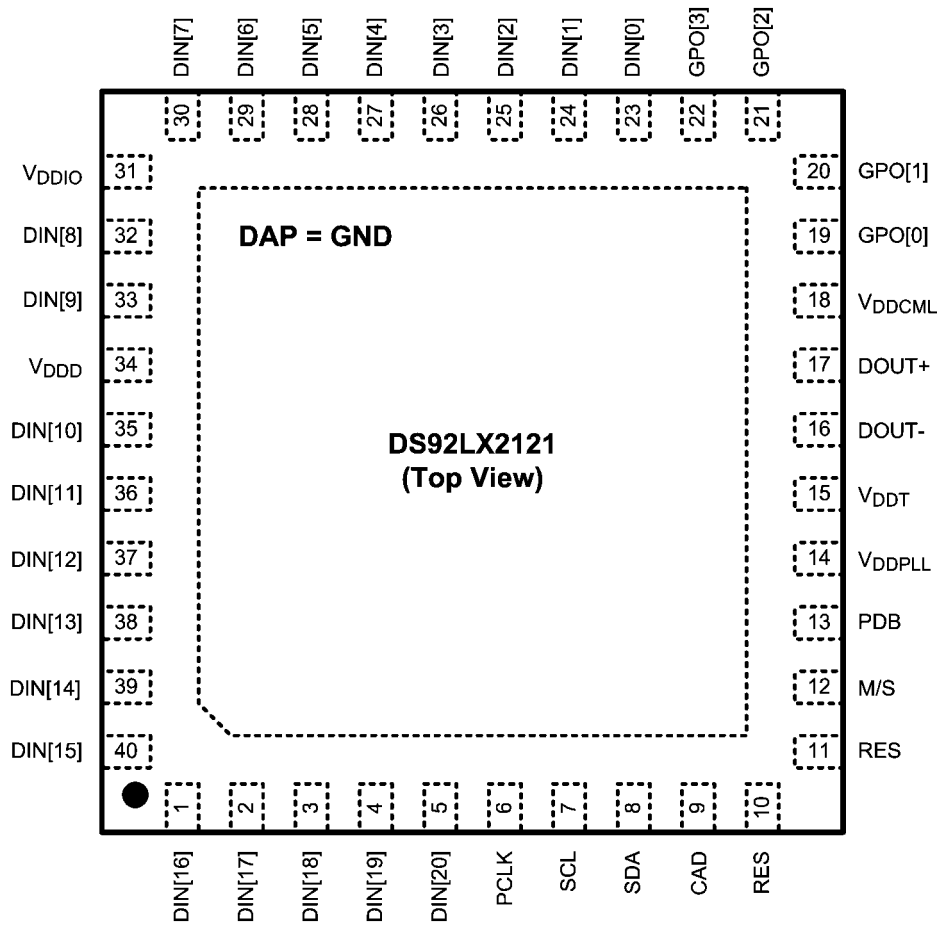


FIGURE 2. Application Block Diagram

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DS92LX2121 Pin Diagram



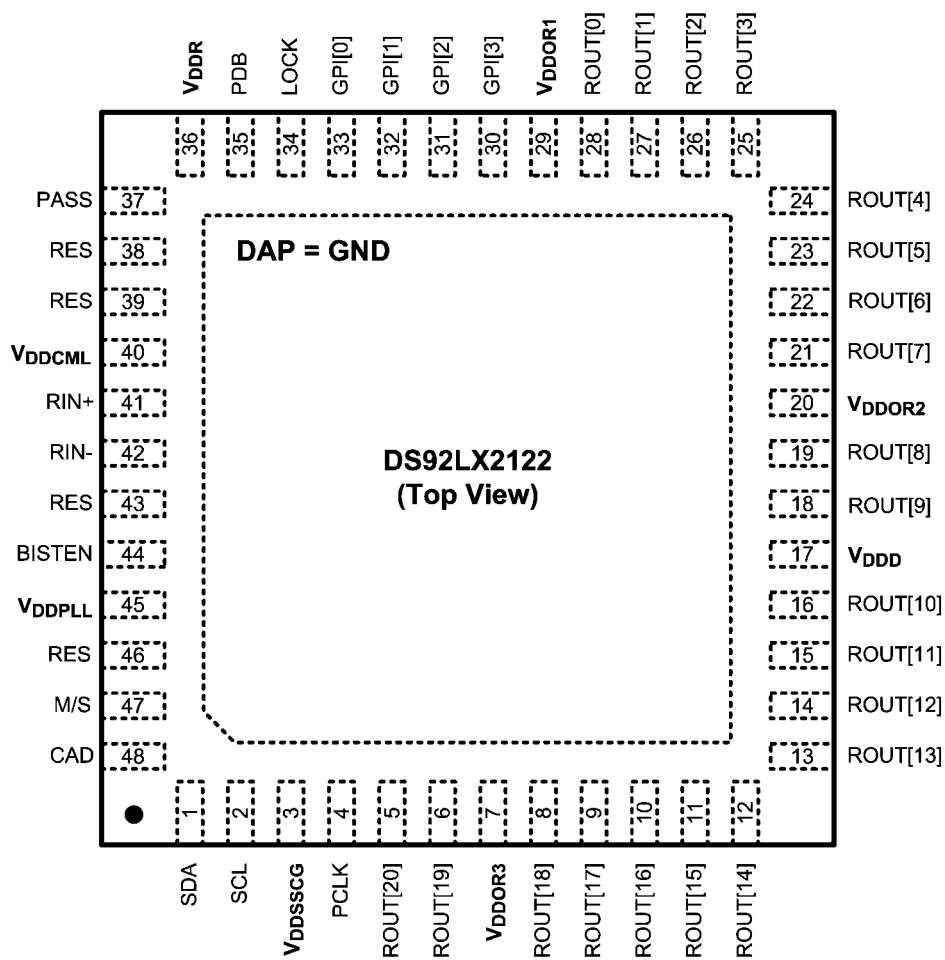
Serializer - DS92LX2121 — Top View

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DS92LX2121 Serializer Pin Descriptions

Pin Name	Number of Pins	I/O, Type	Description
LVC MOS PARALLEL INTERFACE			
DIN[20:0]	21	Inputs, LVCMOS w/ pull down	Parallel data inputs.
PCLK	1	Input, LVCMOS w/ pull down	Pixel Clock Input Pin. Strobe edge set by TRFB configuration.
GENERAL PURPOSE OUTPUT (GPO)			
GPO[3:0]	4	Output, Digital	General-purpose pins individually configured as outputs; which are used to control and respond to various commands.
SERIAL CONTROL BUS - I²C COMPATIBLE			
SCL	1	Input/Output, Open Drain	Clock line for the serial control bus communication SCL requires an external pull-up resistor to V _{DDIO} .
SDA	1	Input/Output, Open Drain	Data line for the serial control bus communication SDA requires an external pull-up resistor to V _{DDIO} .
M/S	1	Input, LVCMOS w/ pull down	I ² C Master / Slave select M/S = L, Master (default); device generates and drives the SCL clock line M/S = H, Slave; device accepts SCL clock input
CAD	1	Input, analog	Continuous Address Decoder Input pin to select the Slave Device Address. Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection).
CONTROL AND CONFIGURATION			
PDB	1	Input, LVCMOS w/ pull down	Power down Mode Input Pin. PDB = H, Transmitter is enabled and is ON. PDB = L, Transmitter is in Sleep (Power Down). When the transmitter is in the SLEEP state, the PLL is shutdown, and IDD is minimized.
RES	2	Input, LVCMOS w/ pull down	Reserved. This pin MUST be tied LOW.
Channel Link III INTERFACE			
DOUT+	1	Input/Output, CML	Non-inverting differential output, back-channel input.
DOUT-	1	Input/Output, CML	Inverting differential output, back-channel input.
Power and Ground			
VDDPLL	1	Power, Analog	PLL Power, 1.8V ±5%
VDDT	1	Power, Analog	Tx Analog Power, 1.8V ±5%
VDDCML	1	Power, Analog	LVDS & BC Dr Power, 1.8V ±5%
VDDD	1	Power, Digital	Digital Power, 1.8V ±5%
VDDIO	1	Power, Digital	Power for input stage, The single-ended inputs are powered from V _{DDIO} .
VSS	-	Ground, DAP	All VSS pads are down bonded to DAP. DAP must be grounded.

DS92LX2122 Pin Diagram



Deserializer - DS92LX2122 — Top View

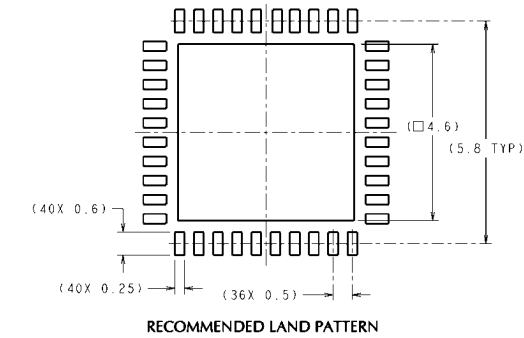
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DS92LX2122 Deserializer Pin Descriptions

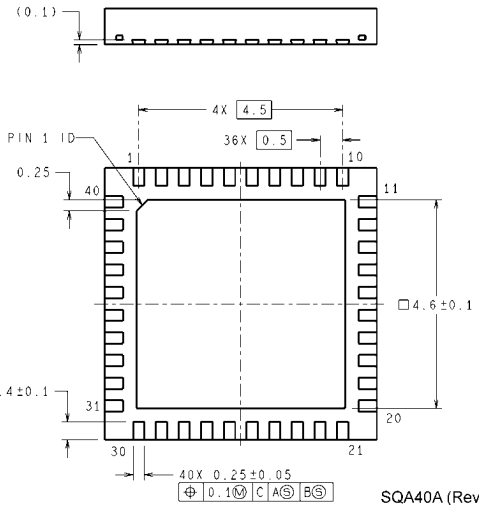
Pin Name	Number of Pins	I/O, Type	Description
LVC MOS PARALLEL INTERFACE			
ROUT[20:0]	21	Outputs, LVC MOS	Parallel data outputs.
PCLK	1	Output, LVC MOS	Pixel Clock Output Pin. Strobe edge set by RFB configuration. In SLEEP, outputs are controlled by the OSS_SEL.
General Purpose Input (GPI)			
GPI[3:0]	4	Input/Output, Digital	General-purpose pins individually configured as inputs; which are used to control and respond to various commands.
SERIAL CONTROL BUS - I²C COMPATIBLE			
SCL	1	Input/Output, Open Drain	Clock line for the serial control bus communication SCL requires an external pull-up resistor to V _{DDIO} .
SDA	1	Input/Output, Open Drain	Data line for serial control bus communication SDA requires an external pull-up resistor to V _{DDIO} .
M/S	1	Input, LVC MOS w/ pull up	I ² C Master / Slave select M/S = L, Master; device generates and drives the SCL clock line M/S = H, Slave (default); device accepts SCL clock input
CAD	1	Input, analog	Continuous Address Decoder Input pin to select the Slave Device Address. Input is connect to external resistor divider to programmable Device ID address (see Serial Control Bus Connection)
CONTROL AND CONFIGURATION			
PDB	1	Input, LVC MOS w/ pull down	Power down Mode Input Pin. PDB = H, Receiver is enabled and is ON. PDB = L, Receiver is in Sleep (Power down mode). When the Receiver is in the SLEEP state, the LVC MOS Outputs are in TRI-STATE, the PLL is shutdown and IDD is minimized.
LOCK	1	Output, LVC MOS	LOCK Status Output Pin. LOCK = H, PLL is Locked, outputs are active LOCK = L, PLL is unlocked, ROUT and PCLK output states are controlled by OSS_SEL. May be used as Link Status.
RES	4	-	Reserved. Pin 46: This pin MUST be tied LOW. Pins 38, 39, 43: Leave pin open.
BIST MODE			
BISTEN	1	Input, LVC MOS w/ pull down	BIST Enable Pin. BISTEN = H, BIST Mode is enabled. BISTEN = L, BIST Mode is disabled.
PASS	1	Output, LVC MOS	PASS Output Pin for BIST mode. PASS = H, ERROR FREE Transmission PASS = L, one or more errors were detected in the received payload. Leave Open if unused. Route to test point (pad) recommended.
Channel Link III INTERFACE			
RIN+	1	Input/Output, CML	Noninverting differential input, back channel output.
RIN-	1	Input/Output, CML	Inverting differential input, back channel output.

Pin Name	Number of Pins	I/O, Type	Description
POWER AND GROUND			
VDDSSCG	1	Digital Power	SSCG Power, 1.8V $\pm$ 5%
VDDOR1/2/3	3	Digital Power	TTL Output Buffer Power, The single-ended outputs and control input are powered from V _{DDIO} . V _{DDIO} can be connected to a 1.8V $\pm$ 5% or 3.3V $\pm$ 10%
VDDD	1	Digital Power	Digital Core Power, 1.8V $\pm$ 5%
VDDR	1	Analog Power	Rx Analog Power, 1.8V $\pm$ 5%
VDDCML	1	Analog Power	BC Driver Power, 1.8V $\pm$ 5%
VDDPLL	1	Analog Power	PLL Power, 1.8V $\pm$ 5%
VSS	-	Ground	All VSS pads are down bonded to DAP. DAP must be grounded.

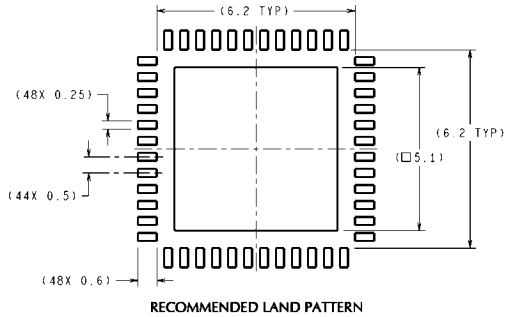
Physical Dimensions inches (millimeters) unless otherwise noted



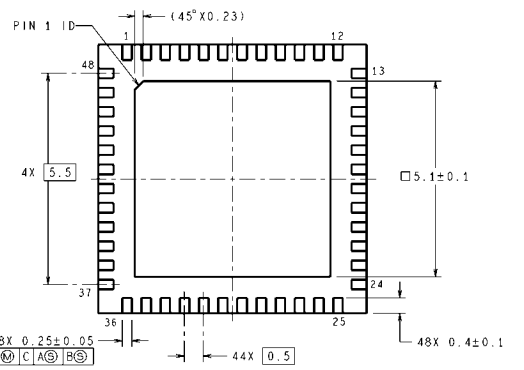
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DS92LX2121 Serializer
NS Package Number SQA40A



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DS92LX2122 Deserializer
NS Package Number SQA48A

Notes

Notes

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