3.3 V SDRAM Modules

HYS 64Vx00(2)0G(C)D(L)-8/-10

144 pin SO-DIMM SDRAM Modules
32MB, 64MB & 128MB density

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual-In-Line Synchronous DRAM Modules for PC notebook applications
- One bank 4M × 64, 8M × 64 and 16M × 64 non-parity module organization
- Two bank 16M × 64 organization
- Performance:

		-8	-10	Units
f_{CK}	Clock frequency (max.)	PC 100	PC 66	MHz
t_{AC}	Clock access time $\overline{CAS}$ latency = 2 & 3	6	8	ns

- Single + 3.3 V (± 0.3 V) power supply
- Programmable $\overline{CAS}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTL compatible
- Serial Presence Detect with E^2PROM
- 4096 refresh cycles every 64 ms
- Gold contact pad
- HYS 64V4000GCD, HYS 64V8000GCD and HYS 64V160(2)0GCD in COB techniques with 1" height only
- Low Power versions with reduced self refresh current also available

This Siemens module family are industry standard 144 pin 8-byte Synchronous DRAM (SDRAM) Small Outline Dual In-line Memory Modules (SO-DIMM) which are organized as x64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs use SDRAMs in TSOPII packages. Decoupling capacitors are mounted on the board.

The DIMMs use optional serial presence detects implemented via a serial E^2PROM using the two pin I^2C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All Siemens 144-pin SO-DIMMs provide a high performance, flexible 8-byte interface in a 67.5 mm long footprint. This module family is available in conventional and COB module assembly technique.

Product Spectrum

Organization	Partnumber	SDRAMs used	Row Addr.	Bank Select	Col. Addr.	Refresh	Period
4M × 64	HYS 64V4000GD(L)-8/-10	4 4M × 16	12	BA0, BA1	8	4k	64 ms
8M × 64	HYS 64V8000G(C)D(L)-8/-10	8 8M × 8	12	BA0, BA1	9	4k	64 ms
16M × 64	HYS 64V1600GCD(L)-8/-10	16 16M × 4	12	BA0, BA1	10	4k	64 ms
16M × 64	HYS 64V1620GCD(L)-8/-10	16 8M × 8	12	BA0, BA1	9	4k	64 ms

Card Dimensions

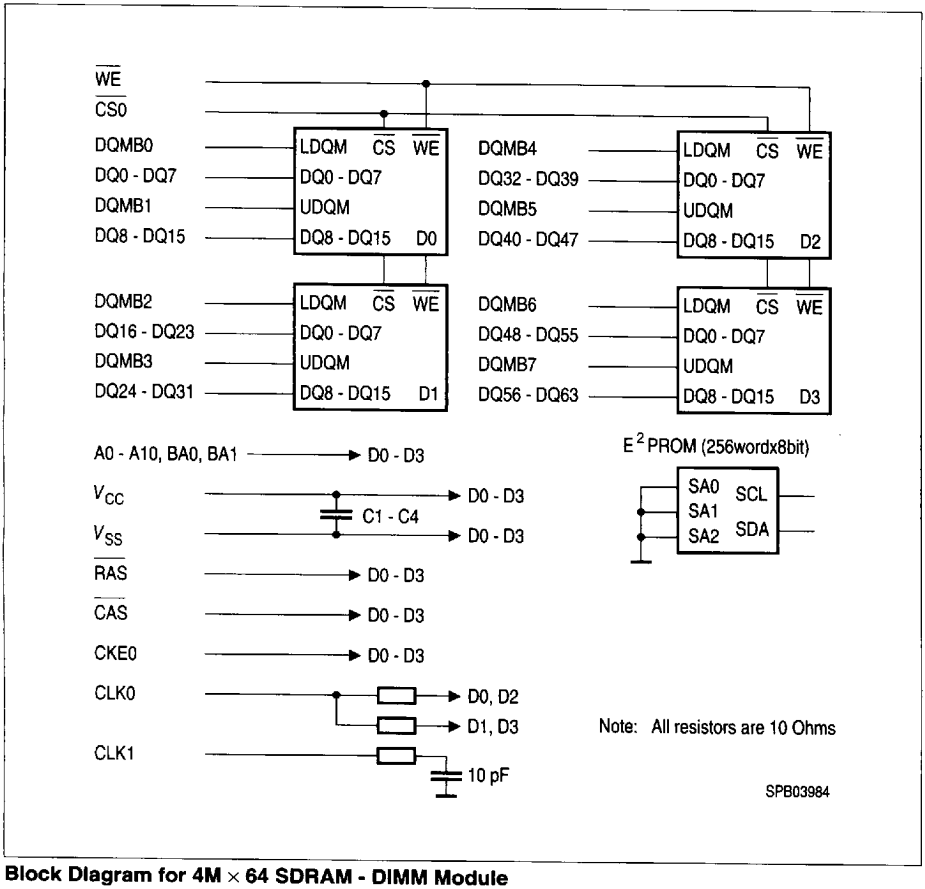
Organization	PCB-Board	L × H × T [mm]
4M × 64	L-DIM-144-7	67.60 × 25.40 × 3.80
8M × 64	L-DIM-144-8	67.60 × 31.75 × 3.80
8M × 64 COB	L-DIM-144-C6	67.60 × 25.40 × 3.80
16M × 64 COB	L-DIM-144-C7	67.60 × 25.40 × 3.80

Pin Names

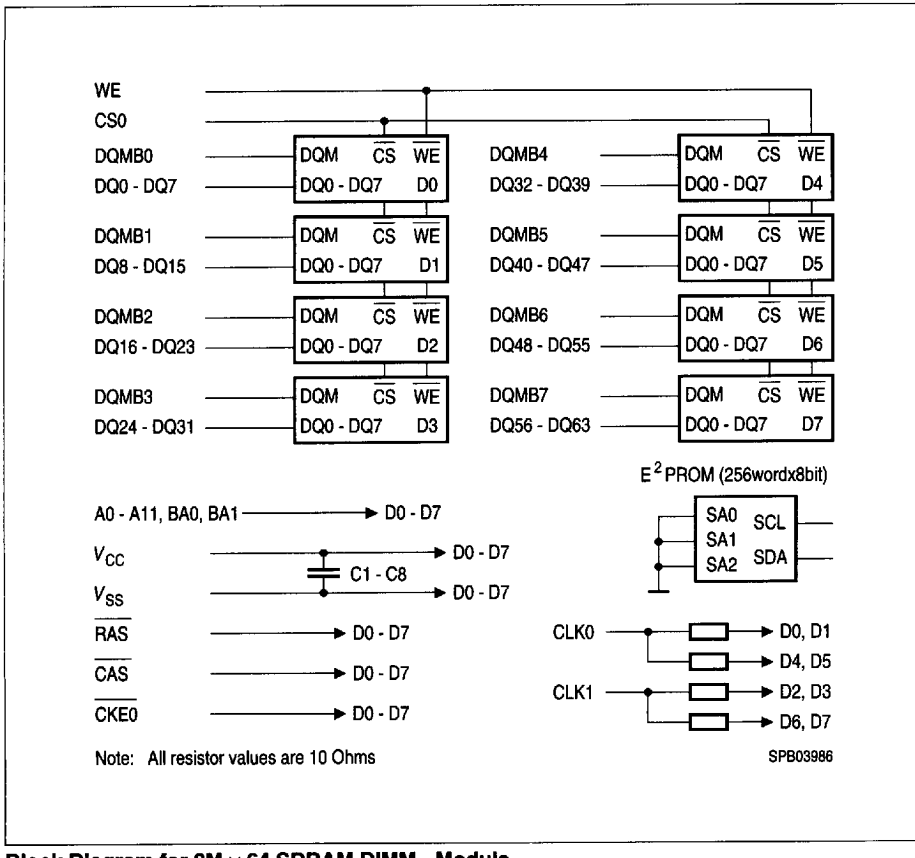
A0 - A11	Address Inputs for 4M × 64, 8M × 64 & 16M × 64 modules
BA0, BA1	Bank Selects for 4M × 64, 8M × 64& 16M × 64 modules
DQ0 - DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
$\overline{CKE0}$	Clock Enable
CLK0	Clock Input
DQMB0 - DQMB7	Data Mask
$\overline{CS0}$ - $\overline{CS3}$	Chip Select
V_{CC}	Power (+ 3.3 Volt)
V_{SS}	Ground
SCL	Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
N.C.	No Connection

Pin Configuration

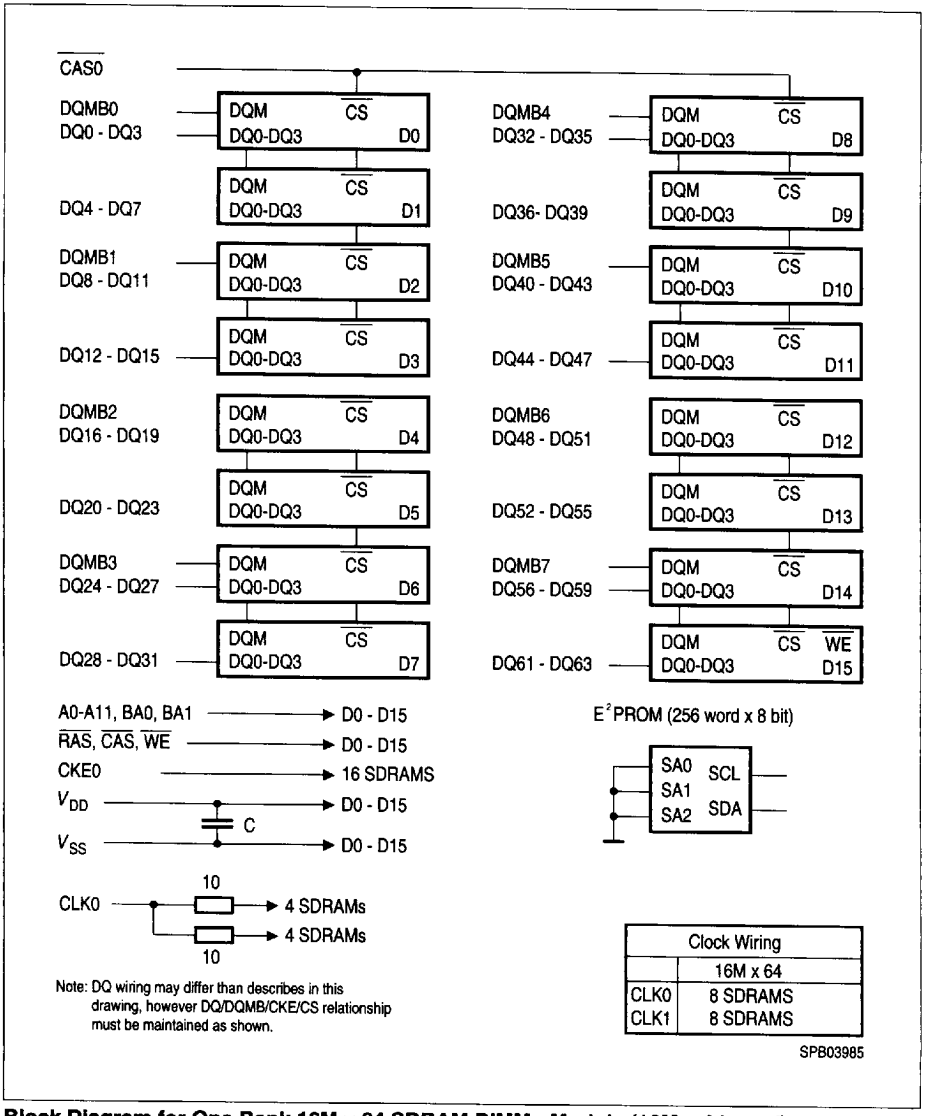
PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	V_{SS}	2	V_{SS}	73	NC	74	CLK1
3	DQ0	4	DQ32	75	V_{SS}	76	V_{SS}
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	V_{CC}	82	V_{CC}
11	V_{CC}	12	V_{CC}	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	V_{SS}	92	V_{SS}
21	V_{SS}	22	V_{SS}	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	V_{CC}	28	V_{CC}	99	DQ23	100	DQ55
29	A0	30	A3	101	V_{CC}	102	V_{CC}
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	V_{SS}	36	V_{SS}	107	V_{SS}	108	V_{SS}
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	V_{CC}	114	V_{CC}
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	V_{CC}	46	V_{CC}	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	V_{SS}	120	V_{SS}
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	V_{SS}	56	V_{SS}	127	DQ27	128	DQ59
57	NC	58	NC	129	V_{CC}	130	V_{CC}
59	NC	60	NC	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	V_{CC}	64	V_{CC}	135	DQ30	136	DQ62
65	$\overline{RAS}$	66	$\overline{CAS}$	137	DQ31	138	DQ63
67	$\overline{WE}$	68	$\overline{CKE1}$	139	V_{SS}	140	V_{SS}
69	$\overline{CS0}$	70	(A12)	141	SDA	142	SCL
71	NC ($\overline{CS1}$)	72	(A13)	143	V_{CC}	144	V_{CC}



Block Diagram for 4M × 64 SDRAM - DIMM Module

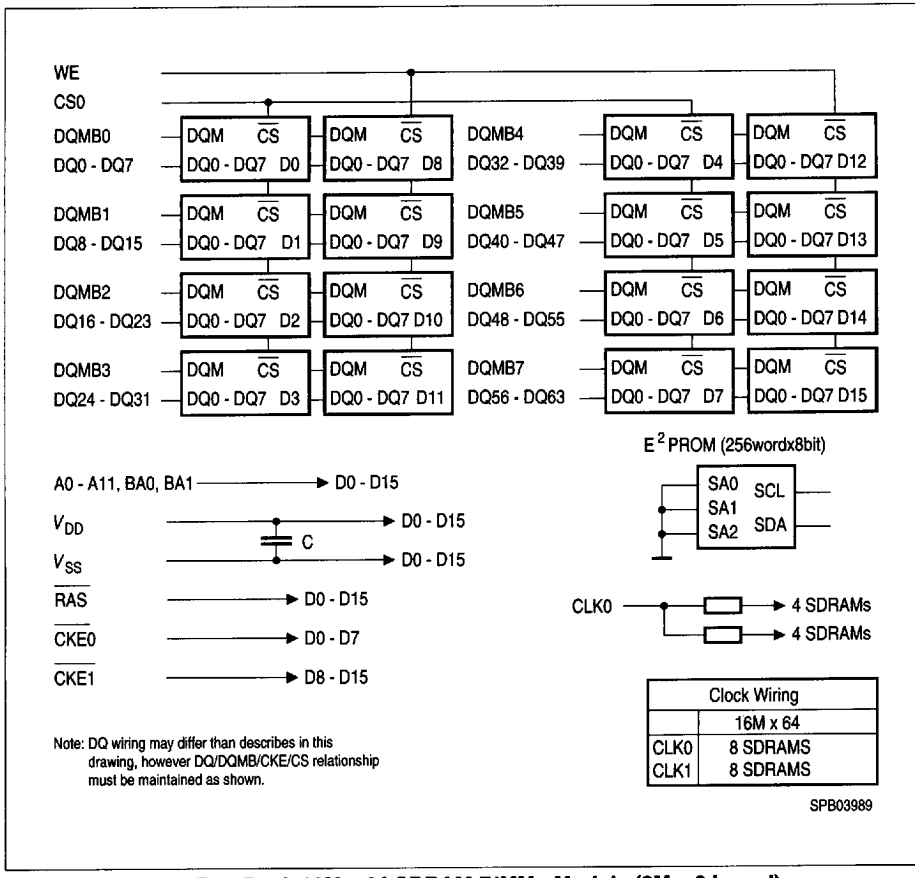


Block Diagram for 8M × 64 SDRAM DIMM - Module



Note: DQ wiring may differ than describes in this drawing, however DQ/DQMB/CKE/CS relationship must be maintained as shown.

Block Diagram for One Bank 16M × 64 SDRAM DIMM - Module (16M × 4 based)



Block Diagram for Two Bank 16M × 64 SDRAM DIMM - Module (8M × 8 based)

DC Characteristics

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input low voltage	V_{IH}	– 0.5	0.8	V
Output high voltage (I_{OUT} = – 2.0 mA)	V_{OH}	2.4	–	V
Output low voltage (I_{OUT} = 2.0 mA)	V_{OL}	–	0.4	V
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 20	20	µA
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 20	20	µA

Capacitance

T_A = 0 to 70 °C; V_{DD} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values				Unit
		4M × 64 max.	8M × 64 max.	16M × 64 max. one bank	16M × 64 max. two banks	
Input capacitance (A0 to A11, BA0, BA1)	C_{I1}	18	–	45	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0)	C_{I2}	18	–	50	65	pF
Input Capacitance (CLK0, CLK1)	C_{I3}	25	–	45	50	pF
Input capacitance (CS0)	C_{I4}	18	–	40	40	pF
Input capacitance (DQMB0 - DQMB7)	C_{I5}	7	–	10	13	pF
Input/Output capacitance (DQ0 - DQ63)	C_{IO}	8	–	9	15	pF
Input capacitance (SCL, SA0 - 2)	C_{SC}	8	–	8	8	pF
Input/Output capacitance	C_{SD}	10	–	10	10	pF

Operating Currents per SDRAM Component

T_A = 0 to 70 °C, V_{DD} = 3.3 V ± 0.3 V

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition		Symb.	-8	-10	Unit	Note
			max.			
Operating Current $t_{RC} = t_{RCMIN.}$, $t_{CK} = t_{CKMIN.}$ Ouputs open, Burst Length = 4, CL = 3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access		I_{CC1} x4 x8 x16	 100 110 130	 70 75 90	 mA mA mA	1
Precharge Standby Current in Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, CKE ≤ $V_{IL(MAX.)}$	t_{CK} = min.	I_{CC2P}	2	2	mA	1
	t_{CK} = Infinity	I_{CC2PS}	1	1	mA	1
Precharge Standby Current in Non-Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, CKE ≥ $V_{IH(MIN.)}$	t_{CK} = min.	I_{CC2N}	35	30	mA	1
	t_{CK} = Infinity	I_{CC2NS}	5	5	mA	1
No Operating Current t_{CK} = min., $\overline{CS} = V_{IH(MIN.)}$, active state (max. 4 banks)	CKE ≥ $V_{IH(MIN.)}$	I_{CC3N}	45	40	mA	1
	CKE ≤ $V_{IL(MAX.)}$	I_{CC3P}	8	8	mA	1
Burst Operating Current t_{CK} = min., Read command cycling		I_{CC4} x4 x8 x16	 60 70 100	 40 50 70	 mA mA mA	1, 2
Auto Refresh Current t_{CK} = min., Auto Refresh command cycling		I_{CC5}	130	90	mA	1
Self Refresh Current Self Refresh Mode, CKE = 0.2V	standard version	I_{CC6}	1	1	mA	1
	L-version		500	500	µA	1

Notes

1. These parameters depend on the cycle rate. These values are measured at 100 MHz for -8 and at 66 MHz for -10 parts. Input signals are changed once during t_{CK}, excepts for I_{CC6} and for standby currents when t_{CK} = infinity.
2. These parameters are measured with continuous data stream during read access and all DQ toggling. CL = 3 and BL = 4 is assumed and the V_{DDQ} current is excluded.

AC Characteristics [1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-8		-10			
		min.	max.	min.	max.		
Clock and Clock Enable							
Clock Cycle Time							
$\overline{CAS}$ Latency = 3	t_{CK}	10	–	10	–	ns	
$\overline{CAS}$ Latency = 2		10	–	15	–	ns	
Clock Frequency							
$\overline{CAS}$ Latency = 3	t_{CK}	–	100	–	100	MHz	
CAS Latency = 2		–	100	–	66	MHz	
Access Time from Clock							
$\overline{CAS}$ Latency = 3	t_{AC}	–	6	–	7	ns	2, 3
$\overline{CAS}$ Latency = 2		–	6	–	8	ns	
Clock High Pulse Width	t_{CH}	3	–	3	–	ns	
Clock Low Pulse Width	t_{CL}	3	–	3	–	ns	
Transition time	t_T	0.5	10	0.5	10	ns	
Setup and Hold Times							
Input Setup Time	t_{IS}	2	–	2.5	–	ns	4
Input Hold Time	t_{IH}	1	–	1	–	ns	4
CKE Setup Time	t_{CKS}	2	–	2.5	–	ns	4
CKE Hold Time	t_{CKH}	1	–	1	–	ns	4
Mode Register Setup time	t_{RSC}	16	–	20	–	ns	
Power Down Mode Entry Time	t_{SB}	0	8	0	10	ns	
Common Parameters							
Row to Column Delay Time	t_{RCD}	20	–	30	–	ns	5
Row Precharge Time	t_{RP}	20	–	30	–	ns	5
Row Active Time	t_{RAS}	50	100k	60	100k	ns	5
Row Cycle Time	t_{RC}	70	–	90	–	ns	5
Activate(a) to Activate(b) Command period	t_{RRD}	16	–	20	–	ns	5
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	–	1	–	CLK	

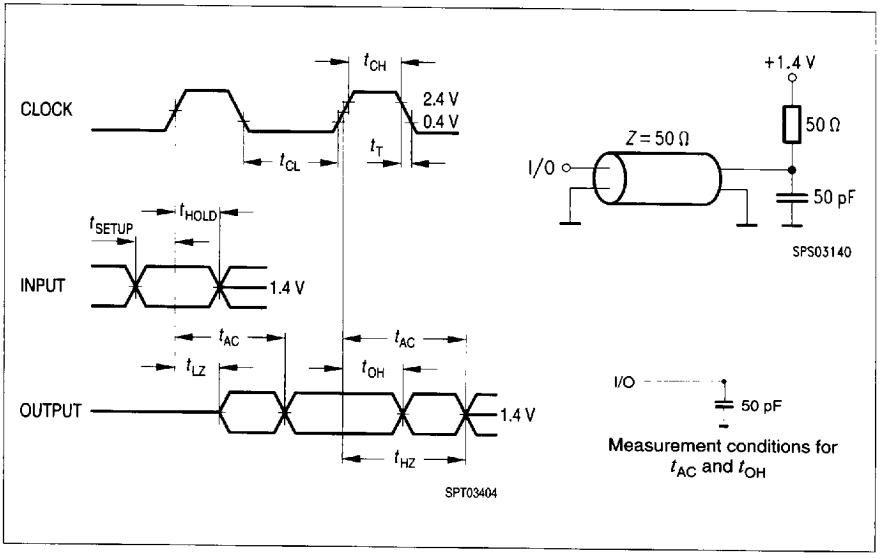
AC Characteristics (cont'd) [1, 2]

T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD} = 3.3 V ± 0.3 V, t_T = 1 ns

Parameter	Symbol	Limit Values				Unit	Note
		-8		-10			
		min.	max.	min.	max.		
Refresh Cycle							
Refresh Period (4096 cycles)	t_{REF}	–	64	–	64	ms	
Self Refresh Exit Time	t_{SREX}	10	–	10	–	ns	
Read Cycle							
Data Out Hold Time	t_{OH}	3	–	3	–	ns	[2]
Data Out to Low Impedance Time	t_{LZ}	0	–	0	–	ns	
Data Out to High Impedance Time	t_{HZ}	3	8	3	10	ns	
DQM Data Out Disable Latency	t_{DQZ}	–	2	–	2	CLK	
Write Cycle							
Data Input to Precharge (write recovery)	t_{WR}	2	–	2	–	CLK	
DQM Write Mask Latency	t_{DQW}	0	–	0	–	CLK	

Notes

1. An initial pause of 100 µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1ns with the AC output load circuit shown.



Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V/ns edge rate between 0.8V and 2.0 V.

3. If clock rising time is longer than 1ns, a time (t_T – 0.5) ns has to be added to this parameter.
4. If t_T is longer than 1ns, a time (t_T – 1) ns has to be added to this parameter.
5. Any time that the refresh Period has been exceeded, a minimum of two Auto (CRB) Refresh commands must be given to "wake-up" the device.
6. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
7. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.
8. t_{DAL} is equivalent to t_{DPL} + t_{RP}.
9. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.
10. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

Serial Presence Detects

A serial presence detect storage device - E^2PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E^2PROM device during module production using a serial presence detect protocol (I^2C synchronous 2-wire bus).

SPD-Table for -10 Modules

Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -10	8M × 64 -10	16M × 64 -10	16M × 64 -10
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS)	–	0C	0C	0C	0C
4	Number of Column Addresses	–	08	09	09	0A
5	Number of DIMM Banks	1	01	01	02	01
6	Module Data Width	64	40	40	40	40
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL = 3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL = 3	8.0 ns	80	80	80	80
11	DIMM Config (Error Det/Corr.)	none	00	00	00	00
12	Refresh Rate/Type	Self-Refresh, 15.6 µs	80	80	80	80
13	SDRAM width, Primary		10	08	08	04
14	Error Checking SDRAM data width	n/a/x8	00	00	00	00
15	Minimum clock delay for back-to-back random column address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	2	04	04	04	04

SPD-Table for -10 Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -10	8M × 64 -10	16M × 64 -10	16M × 64 -10
18	Supported $\overline{CAS}$ Latencies	2, & 3	06	06	06	06
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01	01	01	01
20	$\overline{WE}$ Latencies	$\overline{Write}$ latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes: General	V_{CC} tol ± 10%	06	06	06	06
23	SDRAM Cycle Time at CL = 2	15.0 ns	F0	F0	F0	F0
24	SDRAM Access Time from Clock at CL = 2	8.0 ns	80	80	80	80
25	SDRAM Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	SDRAM Access Time from Clock at CL = 1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	30 ns	1E	1E	1E	1E
28	Minimum Row Active to Row Active delay	20 ns	14	14	14	14
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay	30 ns	1E	1E	1E	1E
30	Minimum $\overline{RAS}$ pulse width	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	–	08	10	10	20
32	SDRAM input setup time	3 ns	25	25	25	25
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	3 ns	25	25	25	25
35	SDRAM data input hold time	1 ns	10	10	10	10
36 - 61	Superset information	–	FF	FF	FF	FF

SPD-Table for -10 Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -10	8M × 64 -10	16M × 64 -10	16M × 64 -10
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62	–	89	8A	8B	97
64 - 125	Manufactures's information (optional)	–	FF	FF	FF	FF
126	Frequency Specification	PC66	66	66	66	66
127	Details	–	87	C7	C7	C7
128+	Unused storage locations	–	FF	FF	FF	FF

SPD-Table for -8 Modules

Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -10	8M × 64 -10	16M × 64 -10	16M × 64 -10
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS)	–	0C	0C	0C	0C
4	Number of Column Addresses	–	08	09	09	0A
5	Number of DIMM Banks	1	01	01	02	01
6	Module Data Width	64	40	40	40	40
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL = 3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL = 3	6.0 ns	60	60	60	60
11	DIMM Config (Error Det/Corr.)	none	00	00	00	00
12	Refresh Rate/Type	Self-Refresh, 15.6 µs	80	80	80	80
13	SDRAM width, Primary	–	10	08	08	04
14	Error Checking SDRAM data width	n/a/x8	00	00	00	00
15	Minimum clock delay for back-to-back random column address	t_{CCD} = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4, 8 & full page	8F	8F	8F	8F
17	Number of SDRAM banks	2	04	04	04	04
18	Supported $\overline{CAS}$ Latencies	2, & 3	06	06	06	06
19	$\overline{CS}$ Latencies	$\overline{CS}$ latency = 0	01	01	01	01
20	$\overline{WE}$ Latencies	$\overline{Write}$ latency = 0	01	01	01	01

SPD-Table for -8 Modules (cont'd)

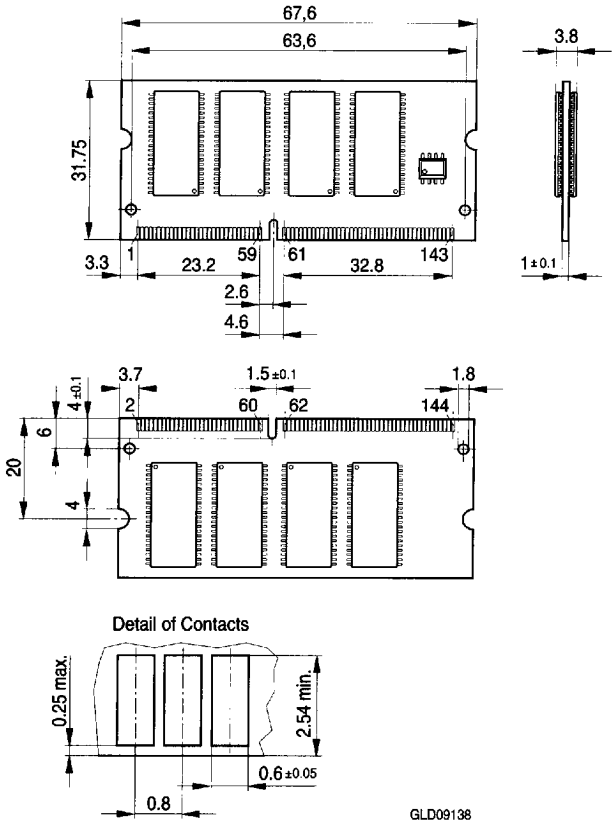
Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -10	8M × 64 -10	16M × 64 -10	16M × 64 -10
21	SDRAM DIMM module attributes	non buffered/ non reg.	00	00	00	00
22	SDRAM Device Attributes: General	V_{CC} tol ± 10%	0E	0E	0E	0E
23	SDRAM Cycle Time at CL = 2	10.0 ns	A0	A0	A0	A0
24	SDRAM Access Time from Clock at CL = 2	6.0 ns	60	60	60	60
25	SDRAM Cycle Time at CL = 1	not supported	FF	FF	FF	FF
26	SDRAM Access Time from Clock at CL = 1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20 ns	14	14	14	14
28	Minimum Row Active to Row Active delay	160 ns	10	10	10	10
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay	20 ns	14	14	14	14
30	Minimum $\overline{RAS}$ pulse width	45 ns	2D	2D	2D	2D
31	Module Bank Density (per bank)	–	08	10	10	20
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10
36 - 61	Superset information	–	FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62	–		00	01	0D

SPD-Table for -8 Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex			
			4M × 64 -10	8M × 64 -10	16M × 64 -10	16M × 64 -10
64 - 125	Manufactures's information (optional)	–	FF	FF	FF	FF
126	Frequency Specification	PC66	64	64	64	64
127	Details	–	87	C7	C7	C7
128+	Unused storage locations	–	FF	FF	FF	FF

Package Outlines

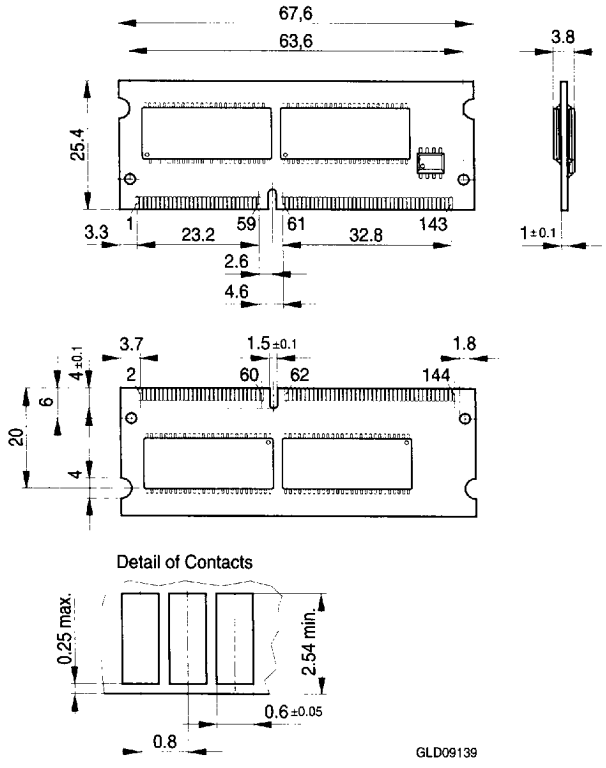
L-DIM-144-6
16 MByte SO-DIMM Module Package
(144 pin, dual read-out, single in-line memory module)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

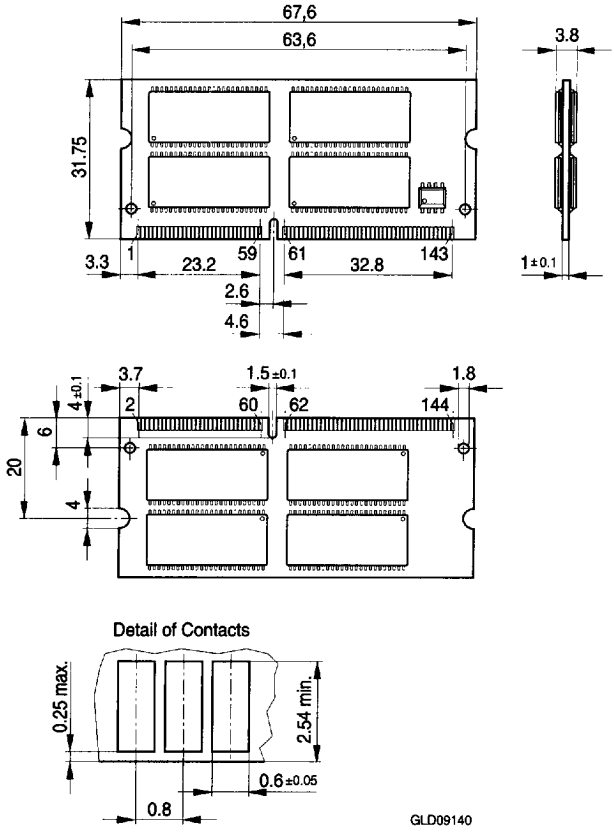
L-DIM-144-7
32 MByte SO-DIMM Module Package
(144 pin, dual read-out, single in-line memory module)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

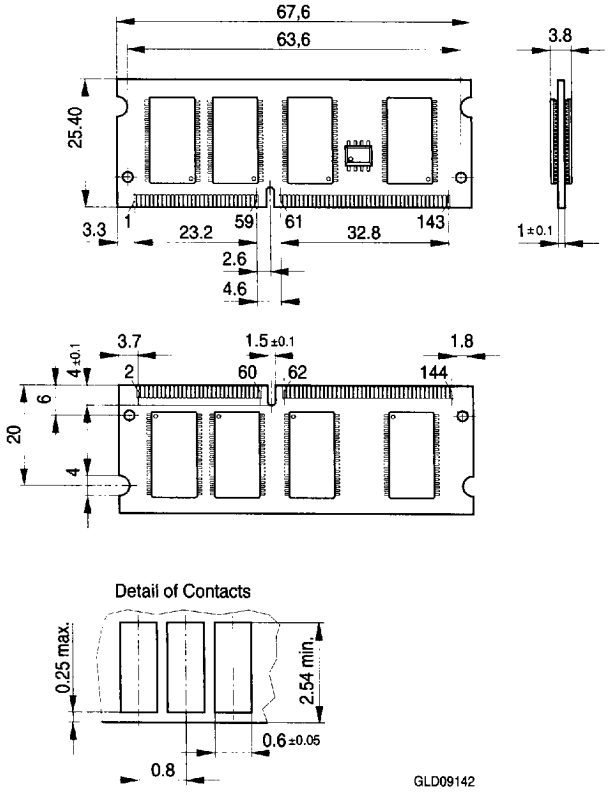
L-DIM-144-8
64 MByte SO-DIMM Module Package
(144 pin, dual read-out, single in-line memory module)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

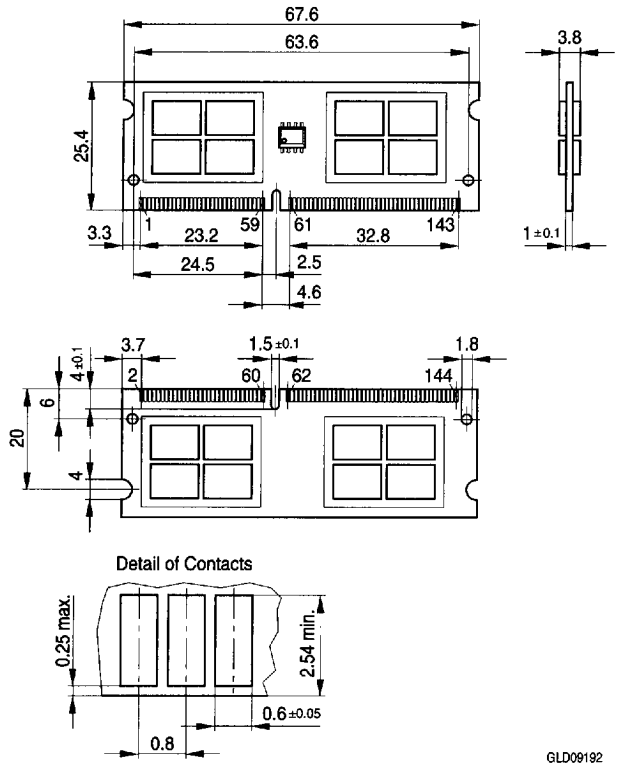
L-DIM-144-C6
64 MByte COB SO-DIMM Module Package
(144 pin, dual read-out, single in-line memory module)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm

L-DIM-144-C7
128 MByte COB SO-DIMM Module Package
(144 pin, dual read-out, single in-line memory module)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm