
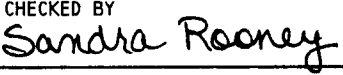



REVISIONS

LTR	DESCRIPTION										DATE (YR-MO-DA)				APPROVED								
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PMIC N/A					PREPARED BY 					DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444													
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A					CHECKED BY 					MICROCIRCUIT, LINEAR, DIGITAL TO ANALOG CONVERTER, 12 BIT, HIGH SPEED, MONOLITHIC SILICON													
					APPROVED BY 																		
					DRAWING APPROVAL DATE					92-07-15					SIZE		CAGE CODE		5962-89808				
					REVISION LEVEL										A		67268						
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DESC FORM 193

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5962-E487

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89808	01	J	X
_____	_____	_____	_____
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AD568SQ	12-bit high speed D/A converter
02	AD568SE	12-bit high speed D/A converter

1.2.2 Case outline. The case outline shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-Line
3	CQCC1-N28	28	Square leadless chip carrier

1.3 Absolute maximum ratings.

V_{CC} to reference common range	0 V dc to +18 V dc
V_{EE} to reference common range	0 V dc to -18 V dc
Reference common to ladder common range	+100 mV to -10 V dc
Analog common to ladder common	±100 mV
Threshold common to ladder common	±500 mV
10 V span resistor to ladder common	±12 V
Bipolar offset to ladder common	±5 V
I_{OUT} to ladder common	-5 V dc to threshold control
Digital inputs to threshold common range	-500 mV to +7.0 V dc
Voltage across span resistor	12 V dc
Threshold control to threshold common range	-0.7 V dc to +1.4 V dc
Logic threshold control input current	5 mA
Power dissipation (P_D):	
Case J	1000 mW
Case 3	600 mW
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	200°C
Thermal resistance junction-to-case (Θ_{JC}):	
Case J	25°C/W
Case 3	42°C/W
Thermal resistance junction-to-ambient (Θ_{JA}):	
Case J	75°C/W
Case 3	125°C/W

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55°C to +125°C
V_{CC} to reference common range	+13.5 V dc to +16.5 V dc
V_{EE} to reference common range	-13.5 V dc to -16.5 V dc

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C V _{CC} = +15 V, V _{EE} = -15 V unless otherwise specified	Device type	Group A subgroups	Limits ^{1/}		Unit
					Min	Max	
Relative accuracy	RA	I _{OUT} mode	ALL	1	-0.5	+0.5	LSB
			01	2, 3	-0.75	+0.75	
			02	2, 3	-1	+1	
Differential nonlinearity	DNL	I _{OUT} mode	ALL	1, 2, 3	-1	+1	
Gain error	A _E	All bits on, I _{OUT} mode	ALL	1	-1	+1	% of FSR
Gain drift temperature coefficient	TCA _E	All bits on, V _{OUT} mode	01	2, 3	-50	+50	ppm of FSR/°C
			02	2, 3	-60	+60	
		All bits on, I _{OUT} mode	ALL	2, 3	-150	+150	
Unipolar offset	U _{OS}	All bits off, I _{OUT} mode	ALL	1	-0.2	+0.2	% of FSR
Unipolar offset temperature coefficient	TCU _{OS}	All bits off, V _{OUT} mode	ALL	2, 3	-5	+5	ppm of FSR/°C
Bipolar offset	B _{POS}	I _{OUT} mode All bits off bipolar	ALL	1	-1.0	+1.0	% of FSR
Bipolar offset temperature coefficient	TCB _{POS}	V _{OUT} mode All bits off bipolar	01	2, 3	-30	+30	ppm of FSR/°C
			02	2, 3	-40	+40	
Bipolar zero	B _{PZE}	I _{OUT} mode, MSB on, all other bits off bipolar	ALL	1	-0.2	+0.2	% of FSR
Bipolar zero temperature coefficient	TCB _{PZE}	V _{OUT} mode, MSB on, all other bits off bipolar	ALL	2, 3	-15	+15	ppm of FSR/°C
High input voltage	V _{IH}		ALL	1, 2, 3	2.0	7.0	V
Low input voltage	V _{IL}		ALL	1, 2, 3	0.0	0.8	
High input current	I _{IH}	V _{IH} = 7 V	ALL	1, 2, 3	-10.0	+10.0	μA
Low input current	I _{IL}	V _{IL} = 0.0 V	ALL	1	-100	-0.5	
				2, 3	-200	-0.5	
Output current	I _O	Unipolar, all bits on	ALL	1	10.137	10.343	mA
				2, 3	9.985	10.50	
		Bipolar, all bits on		1	5.017	5.223	
				2, 3	4.942	5.300	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C V _{CC} = +15 V, V _{EE} = -15 V unless otherwise specified	Device type	Group A subgroups	Limits ^{1/}		Unit
					Min	Max	
Output voltage	V _O	Unipolar, all bits on	ALL	1	1.014	1.034	V
				2, 3	1.008	1.040	
		Bipolar, all bits on		1	.507	.517	
				2, 3	.504	.520	
Compliance voltage	V _C	≥/	ALL	1, 2, 3	-2	+1.2	
Output resistance exclusive of R _L	R _{OE}	≥/	ALL	1, 2, 3	160	240	Ω
Output resistance inclusive of R _L	R _{OI}	≥/	ALL	1, 2, 3	99	101	
Settling time	t _{SL}	Current to ±0.025 % of FSR ≥/	ALL	9		120	ns
				10, 11		165	
		Current to ±0.1 % of FSR ≥/		9		125	
				10, 11		130	
Rise time	t _R	From 10 % to 90 %, V _{OUT} ^{≥/} mode	ALL	9,10,11		20	
Fall time	t _F	From 90 % to 10 %, V _{OUT} ^{≥/} mode	ALL	9,10,11		20	
Power supply current	I _{CC}	V _{CC} = 16.5 V V _{EE} = -16.5 V V _{OUT} = 5 V	ALL	1, 2, 3		32	mA
	I _{EE}	V _{CC} = 16.5 V V _{EE} = -16.5 V V _{OUT} = 5 V			-8		
Power supply rejection ratio	+PSRR	13.5 V ≤ V _{CC} ≤ 16.5 V V _{EE} = -15 V	ALL	1		0.05	% of FSR/V
				2, 3		0.06	
	-PSRR	-13.5 V ≤ V _{EE} ≤ -16.5 V V _{CC} = 15 V	ALL	1		0.05	
				2, 3		0.06	

^{1/} The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.

^{2/} Guaranteed, if not tested.

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Device types	01	02
Case outlines	J	3
Terminal number	Terminal symbols	Terminal symbols
1	Bit 1 (MSB)	NC
2	Bit 2	Bit 1 (MSB)
3	Bit 3	Bit 2
4	Bit 4	Bit 3
5	Bit 5	Bit 4
6	Bit 6	Bit 5
7	Bit 7	Bit 6
8	Bit 8	NC
9	Bit 9	Bit 7
10	Bit 10	Bit 8
11	Bit 11	Bit 9
12	Bit 12 (LSB)	Bit 10
13	Threshold control (V_{TH})	Bit 11
14	Threshold common (THCOM)	Bit 12 (LSB)
15	10 V span resistor	NC
16	10 V span resistor	Threshold control (V_{TH})
17	Ladder common (LCOM)	Threshold common (THCOM)
18	Analog common (ACOM)	10 V span resistor
19	Load resistor (RL)	10 V span resistor
20	I_{OUT}	Ladder common (LCOM)
21	Bipolar offset (I_{BPO})	Analog common (ACOM)
22	V_{EE}	NC
23	Reference common (REFCOM)	Load resistor (RL)
24	V_{CC}	I_{OUT}
25		Bipolar offset (I_{BPO})
26		V_{EE}
27		Reference common (REFCOM)
28		V_{CC}

FIGURE 1. Terminal connections.

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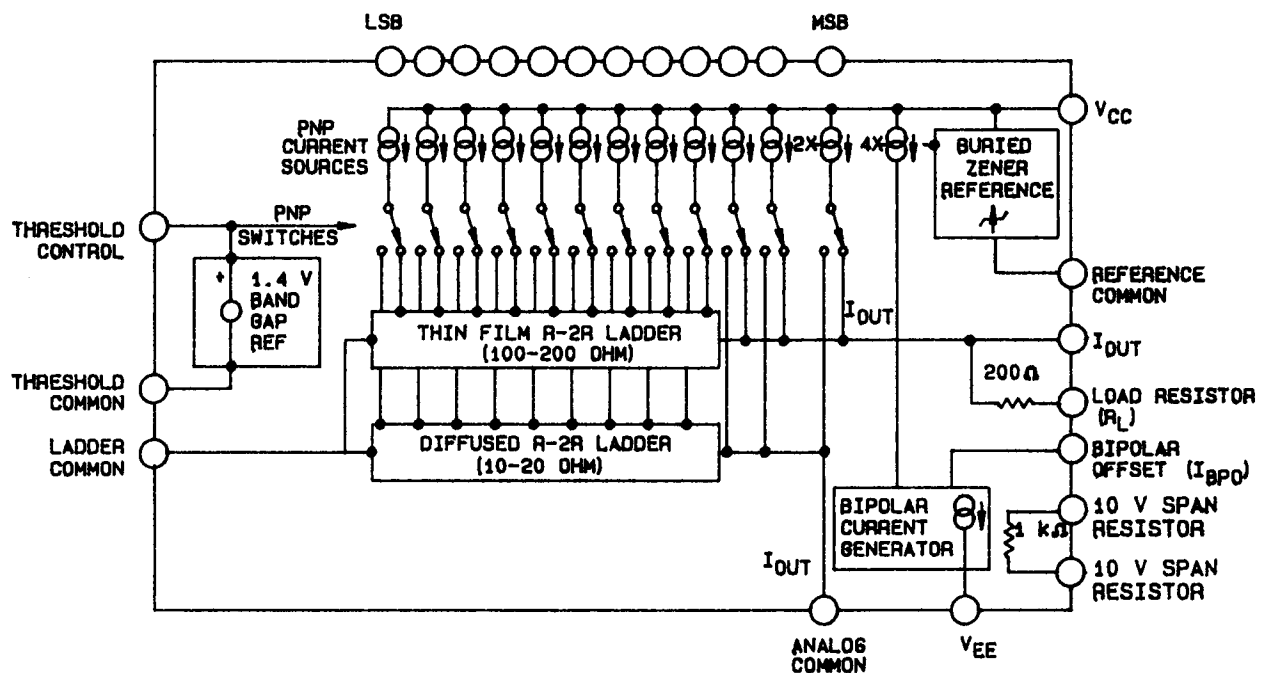


FIGURE 2. Functional block diagram.

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3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 9, 10, and 11 shall be guaranteed, if not tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) $T_A = +125^{\circ}\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3
Group A test requirements (method 5005)	1,2,3,9**, 10**,11**
Groups C and D end-point electrical parameters (method 5005)	1

* PDA applies to subgroup 1.

** Subgroups 9, 10, and 11 shall be guaranteed, if not tested.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6021.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

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