



STB80NF55-06

N-CHANNEL 55V - 0.005Ω - 80A D²PAK

STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STB80NF55-06	55 V	<0.0065Ω	80 A

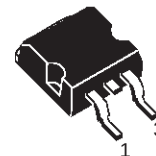
- TYPICAL R_{DS(on)} = 0.005Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION
- ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

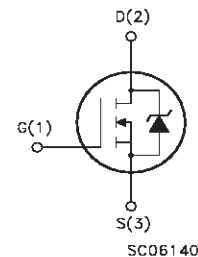
APPLICATIONS

- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- DC-DC CONVERTERS
- AUTOMOTIVE ENVIRONMENT



D²PAK
(TO-263)

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	55	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	55	V
V _{GS}	Gate- source Voltage	±20	V
I _{D(1)}	Drain Current (continuous) at T _C = 25°C	80	A
I _D	Drain Current (continuous) at T _C = 100°C	80	A
I _{DM} (●)	Drain Current (pulsed)	320	A
P _{TOT}	Total Dissipation at T _C = 25°C	300	W
	Derating Factor	2	W/°C
dv/dt(2)	Peak Diode Recovery voltage slope	7	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) Current Limited by Package

(2) I_{SD} ≤ 80A, di/dt ≤ 300 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	80	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	650	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)**OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	55			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250µA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 40 A		0.005	0.0065	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 40 A		50		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		7300		pF
C _{oss}	Output Capacitance			980		pF
C _{rss}	Reverse Transfer Capacitance			250		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 27V, I_D = 40A$		40		ns
t_r	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		240		ns
Q_g	Total Gate Charge	$V_{DD} = 44V, I_D = 80A,$ $V_{GS} = 10V$		190	256	nC
Q_{gs}	Gate-Source Charge			38		nC
Q_{gd}	Gate-Drain Charge			66		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 27V, I_D = 40A,$ $R_G = 4.7\Omega, V_{GS} = 4.5V$ (see test circuit, Figure 3)		260		ns
t_f	Fall Time			75		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 44V, I_D = 80A$ $R_G = 4.7\Omega, V_{GS} = 10V$		70		ns
$T_{r(Voff)}$	Off Voltage Rise time	(see test circuit, Figure 5)		185		ns
t_f	Fall Time			240		ns
t_c	Cross-over Time			110		ns

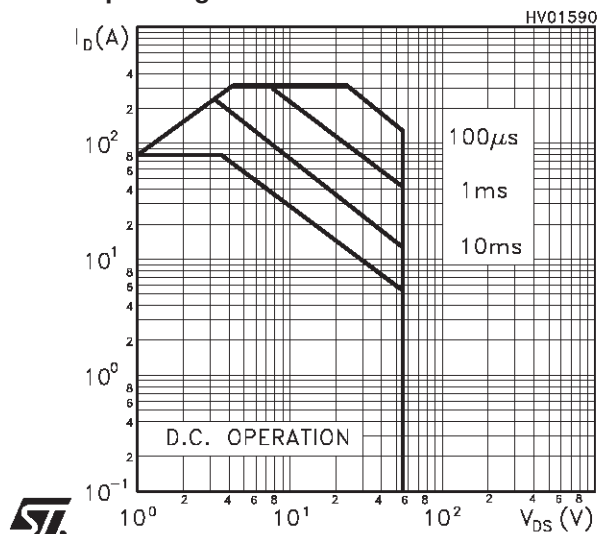
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				80	A
$I_{SDM(1)}$	Source-drain Current (pulsed)				320	A
$V_{SD(2)}$	Forward On Voltage	$I_{SD} = 80A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 80A, di/dt = 100A/\mu s,$ $V_{DD} = 20V, T_J = 150^\circ C$ (see test circuit, Figure 5)		80		ns
Q_{rr}	Reverse Recovery Charge			0.24		μC
I_{RRM}	Reverse Recovery Current			6		A

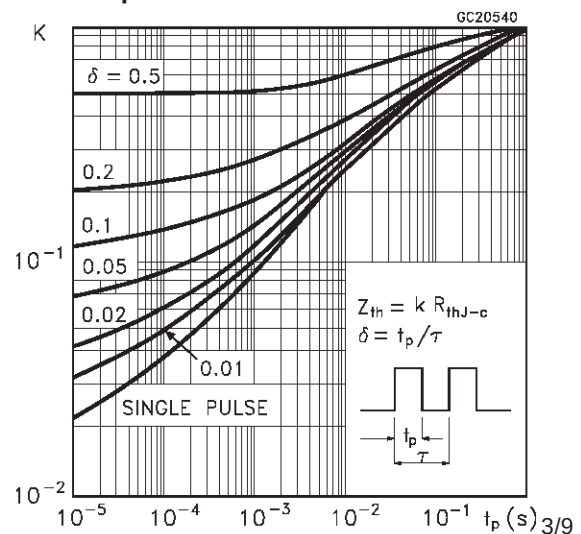
Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

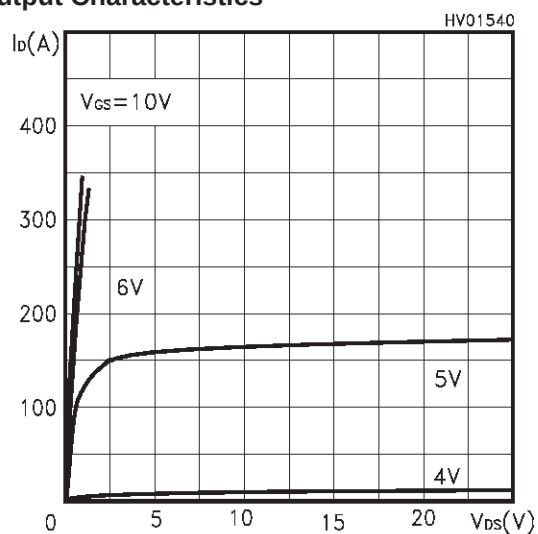
Safe Operating Area



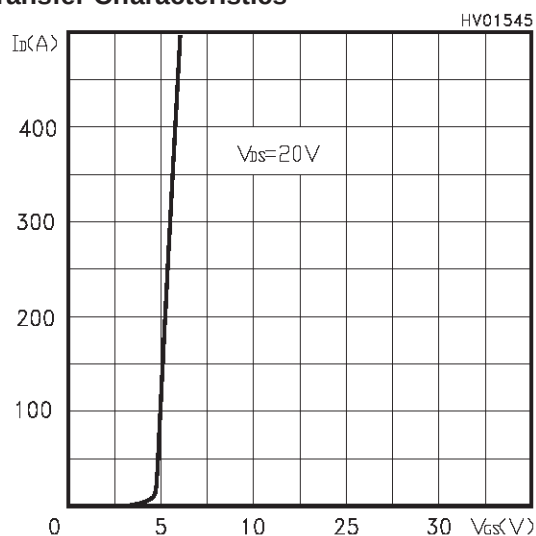
Thermal Impedance



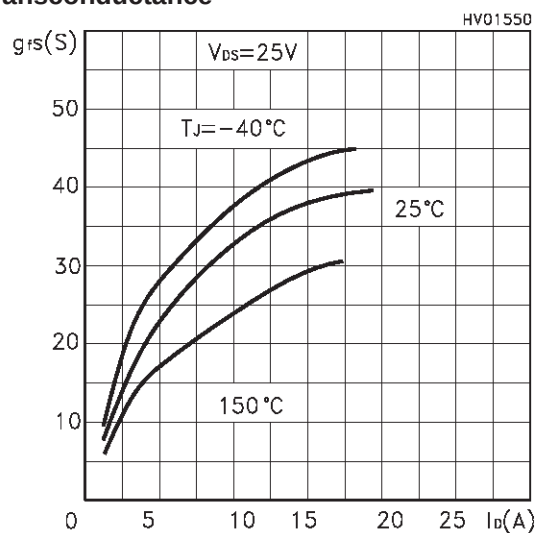
Output Characteristics



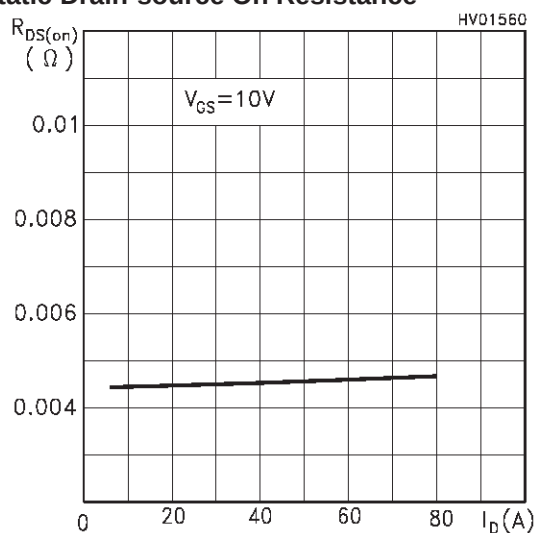
Transfer Characteristics



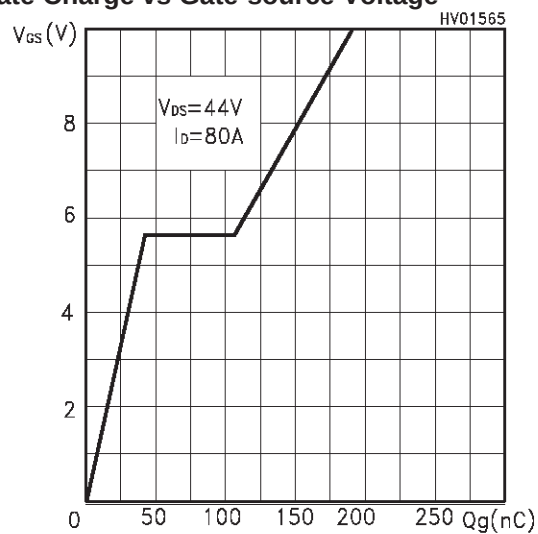
Transconductance



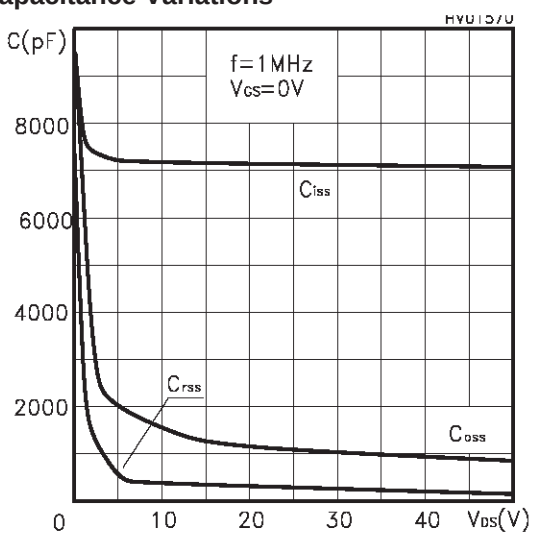
Static Drain-source On Resistance



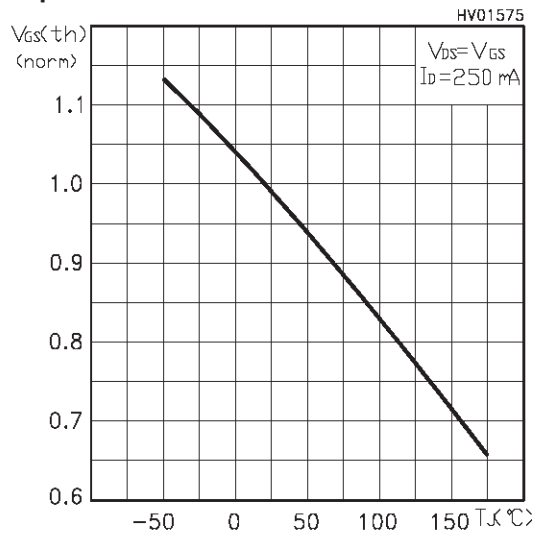
Gate Charge vs Gate-source Voltage



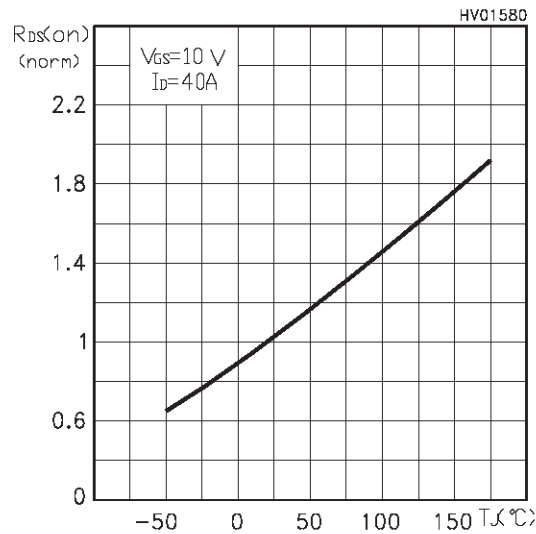
Capacitance Variations



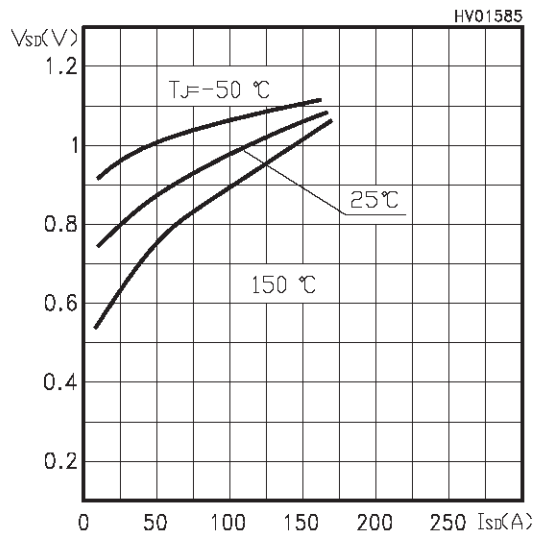
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Drain-Source Breakdown vs Temperature

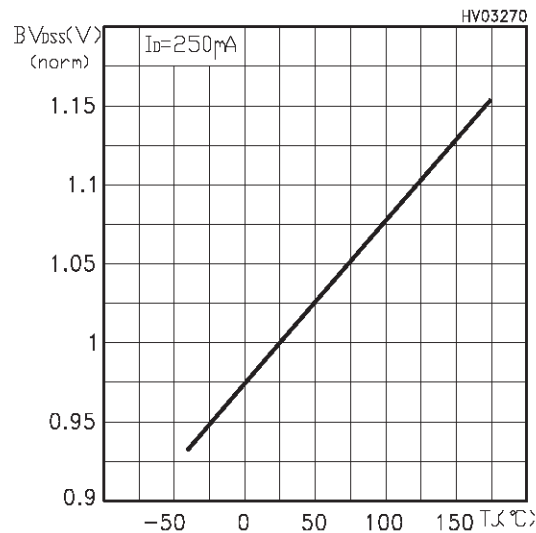


Fig. 1: Unclamped Inductive Load Test Circuit

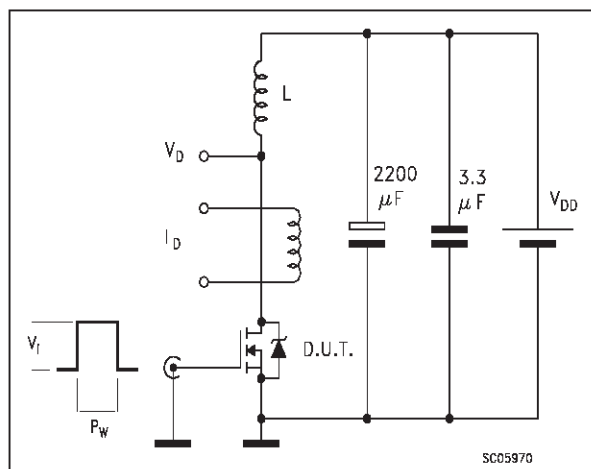


Fig. 2: Unclamped Inductive Waveform

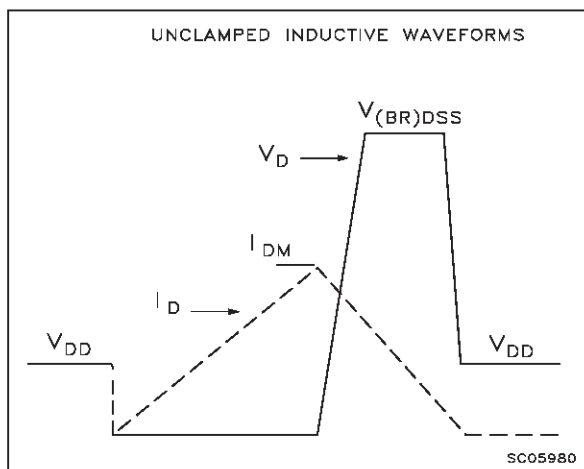


Fig. 3: Switching Times Test Circuit For Resistive Load

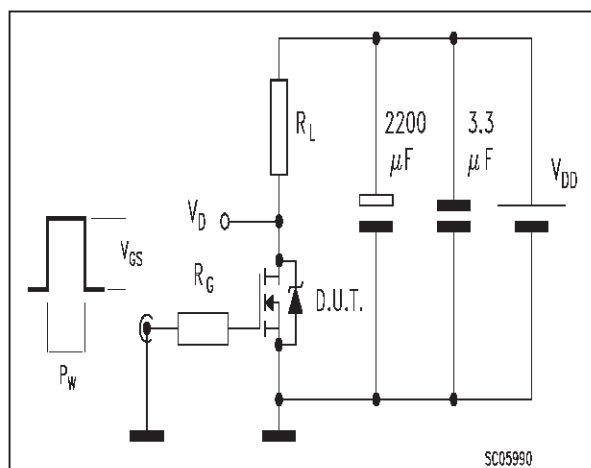


Fig. 4: Gate Charge test Circuit

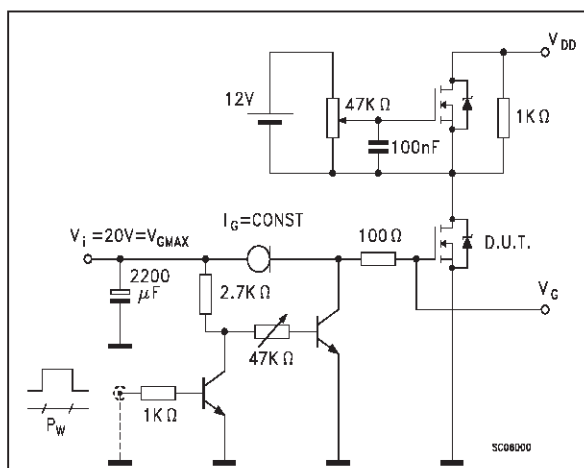
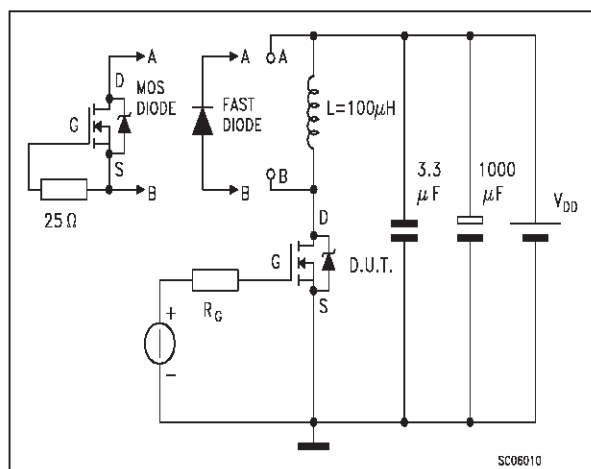
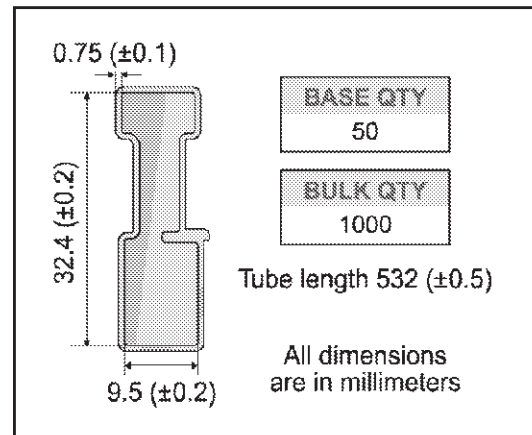


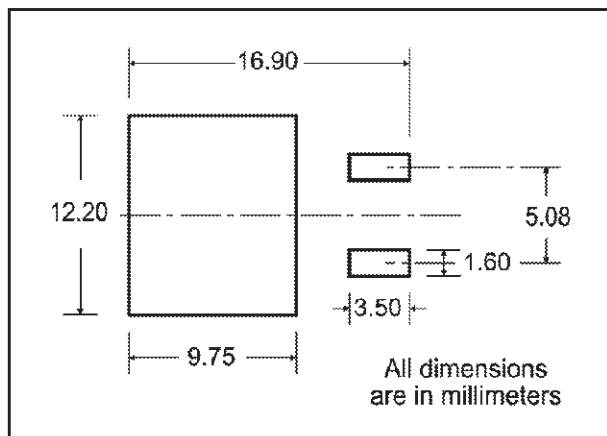
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



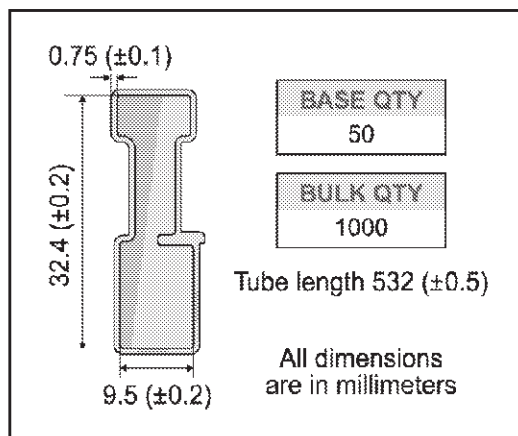
TUBE SHIPMENT (no suffix)*



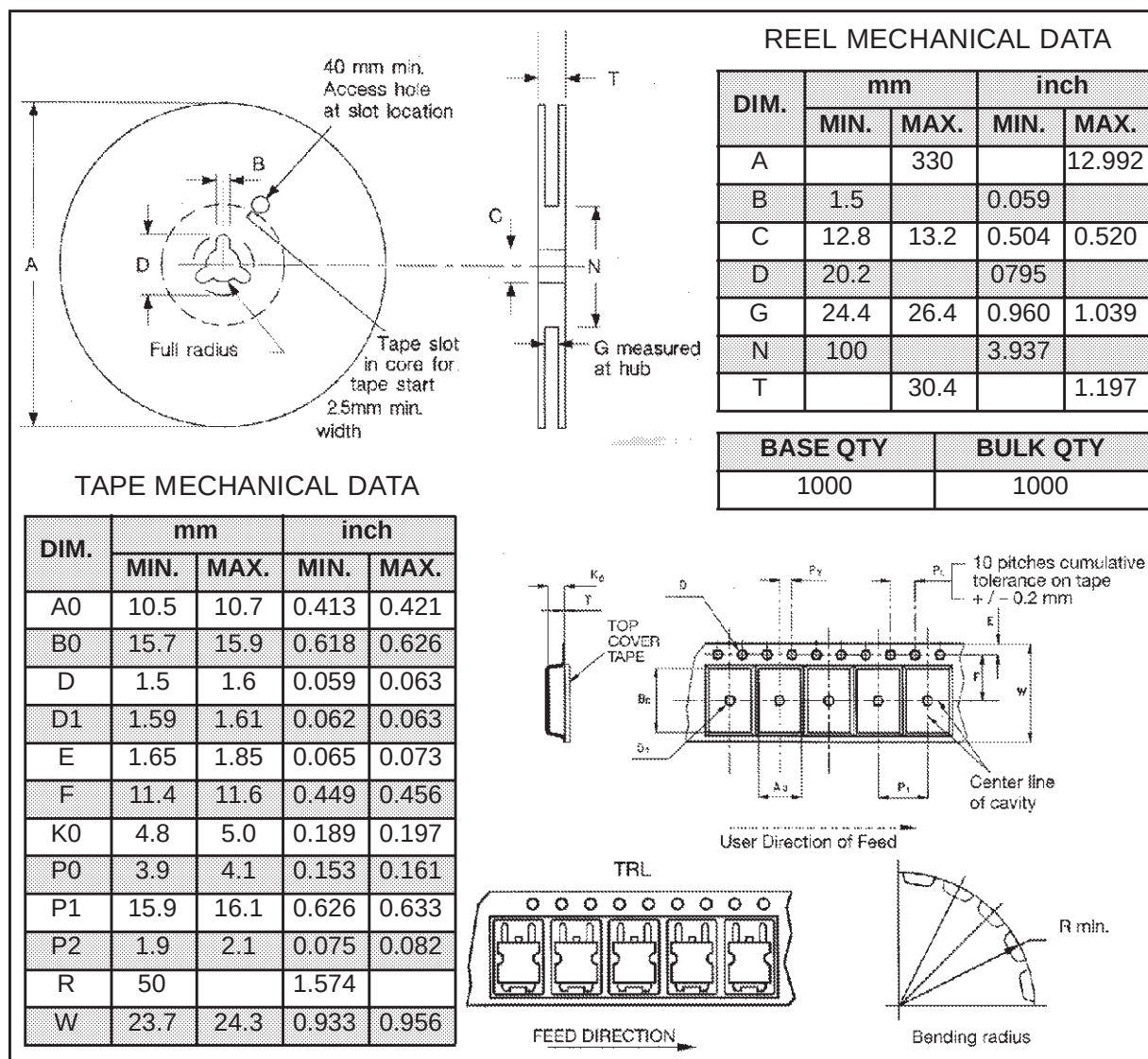
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



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