CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

DESCRIPTION

The new PLC42VA12 CMOS PLD from Philips Semiconductors exhibits a unique combination of the two architectural concepts that revolutionized the PLD marketplace.

The Philips Semiconductors unique Output Macro Cell (OMC) embodies all the advantages and none of the disadvantages associated with the “V” type Output Macro Cell devices. This new design, combined with added functionality of two programmable arrays, represents a significant advancement in the configurability and efficiency of multi-function PLDs.

The most significant improvement in the Output Macro Cell structure is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other “V” type devices, the register in the PLC42VA12 Macro Cell remains fully functional as a buried register. Both the combinatorial I/O and buried register have separate input paths (from the AND array). In most V-type architectures, the register is lost as a resource when the cell is configured as a combinatorial I/O. This feature provides the capability to operate the buried register independently from the combinatorial I/O.

The PLC42VA12 is an EPROM-based CMOS device. Designs can be generated using Philips Semiconductors SNAP PLD design software packages or one of several other commercially available JEDEC standard PLD design software packages.

FEATURES

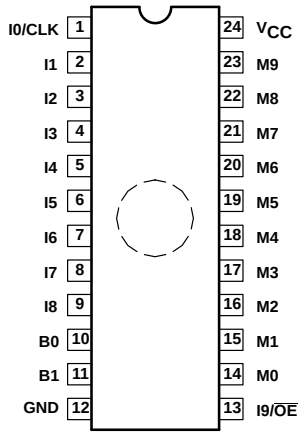
- High-speed EPROM-based CMOS Multi-Function PLD
  - Super set of 22V10, 32VX10 and 20RA10 PAL® ICs
- Two fully programmable arrays eliminate “P-term Depletion”
  - Up to 64 P-terms per OR function
- Improved Output Macro Cell Structure
  - Individually programmable as:
    - * Registered Output with feedback
    - * Registered Input
    - * Combinatorial I/O with Buried Register
    - * Dedicated I/O with feedback
    - * Dedicated Input (combinatorial)
  - Bypassed Registers are 100% functional with separate input and feedback paths
  - Individual Output Enable control functions
    - * From pin or AND array
- Reprogrammable – 100% tested for programmability
- Eleven clock sources
- Register Preload and Diagnostic Test Mode Features
- Security fuse

APPLICATIONS

- Mealy or Moore State Machines
  - Synchronous
  - Asynchronous
- Multiple, independent State Machines
- 10-bit ripple cascade
- Sequence recognition
- Bus Protocol generation
- Industrial control
- A/D Scanning

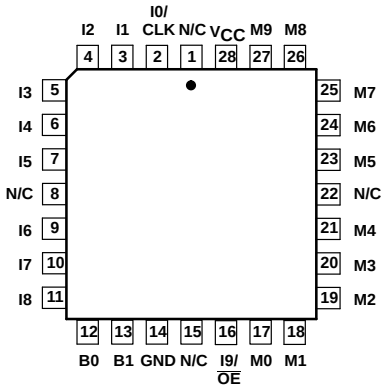
PIN CONFIGURATIONS

FA and N Packages



N = Plastic DIP (300mil-wide)
FA = Ceramic DIP with Quartz Window (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier (450mil-square)

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Ceramic Dual In-Line with window, Reprogrammable (300mil-wide)	PLC42VA12FA	1478A
24-Pin Plastic Dual In-Line, One Time Programmable (300mil-wide)	PLC42VA12N	0410D
28-Pin Plastic Leaded Chip Carrier, One Time Programmable (450mil-wide)	PLC42VA12A	0401F

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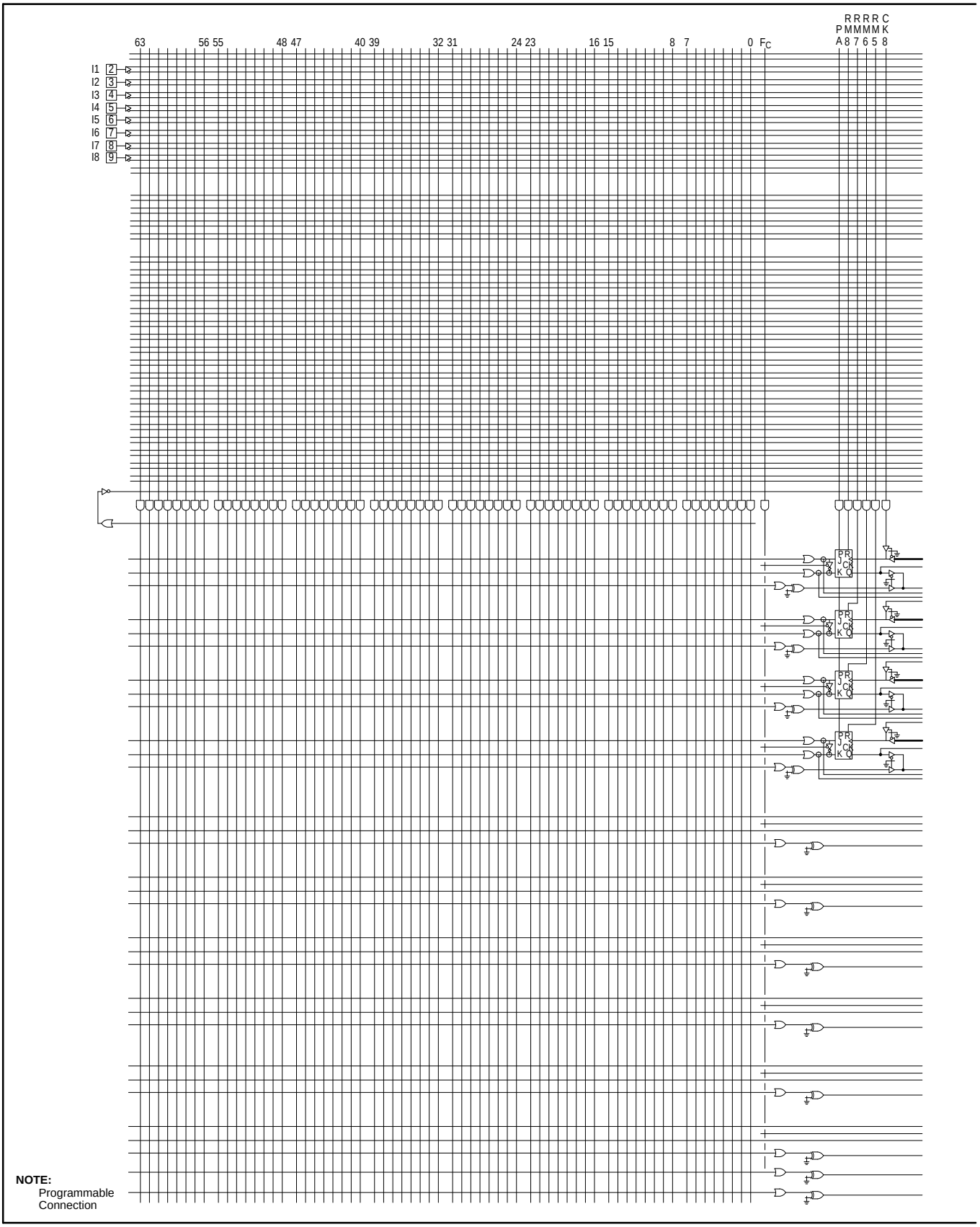
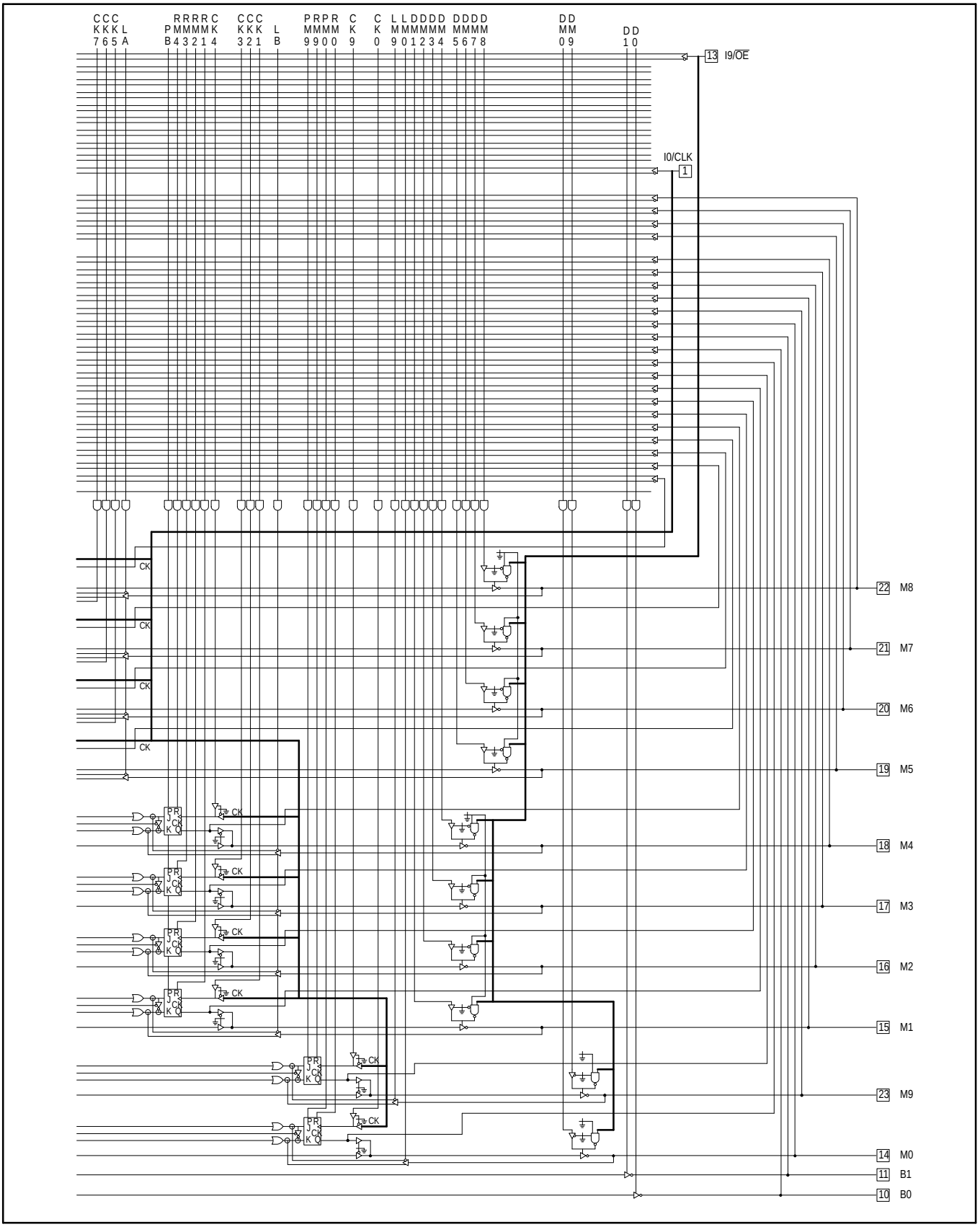
LOGIC DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

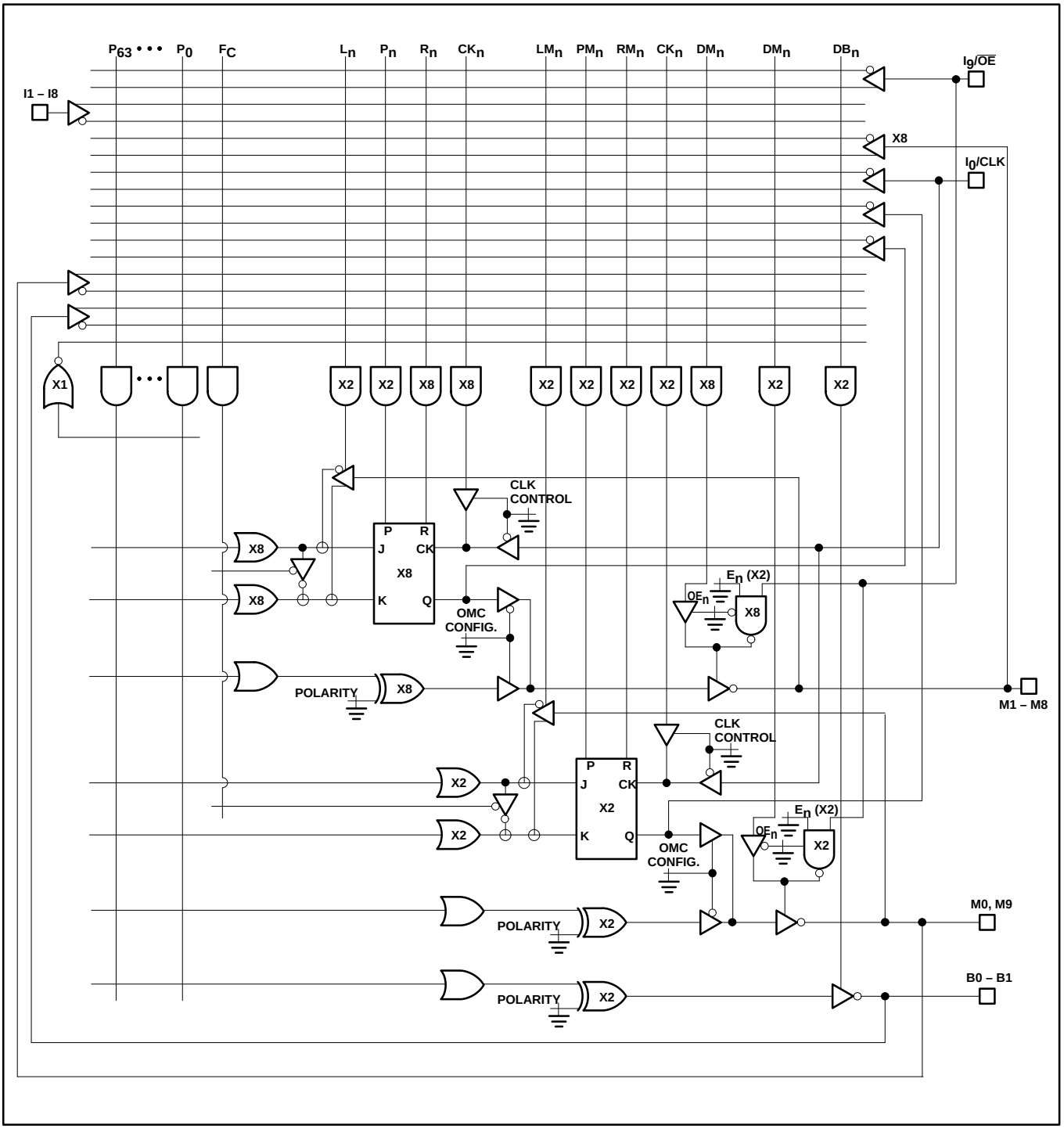
LOGIC DIAGRAM (Continued)



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

FUNCTIONAL DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

ABSOLUTE MAXIMUM RATINGS[1]

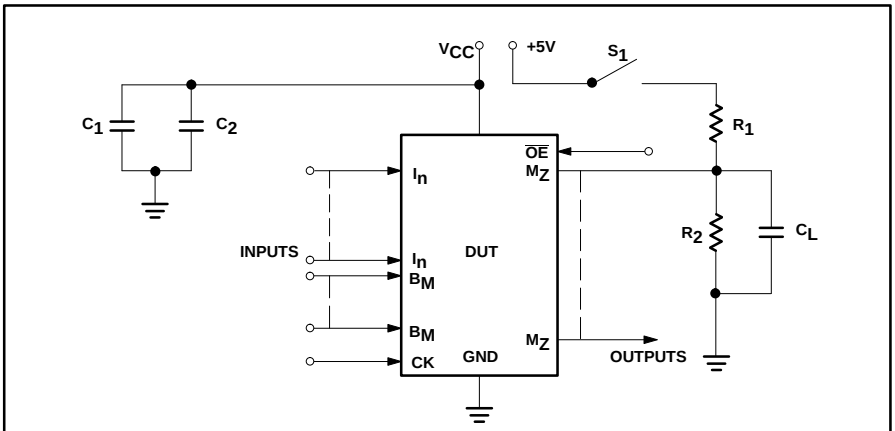
SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	–0.5 to +7	V_{DC}
V_{IN}	Input voltage	–0.5 to V_{CC} +0.5	V_{DC}
V_{OUT}	Output voltage	–0.5 to V_{CC} +0.5	V_{DC}
I_{IN}	Input currents	–10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	–65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

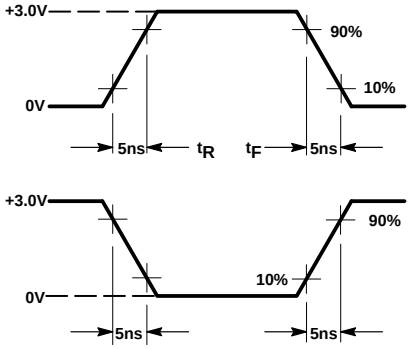
AC TEST CONDITIONS



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN	–0.3		0.8	V
V_{IH}	High	V_{CC} = MAX	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = MIN; I_{OL} = 16mA		0.3	0.5	V
V_{OH}	High	V_{CC} = MIN; I_{OH} = –3.2mA	2.4	4.3		V
Input current						
I_{IL}	Low	V_{IN} = GND		–1	–10	µA
I_{IH}	High	$V_{IN} = V_{CC}$		+1	10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	$V_{OUT} = V_{CC}$ V_{OUT} = GND		1 –1	10 –10	µA µA
I_{OS}	Short-circuit[3,7]	V_{OUT} = GND			–130	mA
I_{CC1}	V_{CC} supply current (Active)[4]	I_{OUT} = 0mA, f = 15MHz[6], V_{CC} = MAX		90	120	mA
I_{CC2}	V_{CC} supply current (Active)[5]	I_{OUT} = 0mA, f = 15MHz[6], V_{CC} = MAX		70	100	mA
Capacitance						
C_I	Input	V_{CC} = 5V; V_{IN} = 2.0V		12		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:

1. All typical values are at V_{CC} = 5V. T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short–circuit should not exceed one second. Test one at a time.
4. Tested with V_{IL} = 0.45V, V_{IH} = 2.4V.
5. Tested with V_{IL} = 0V, $V_{IH} = V_{CC}$.
6. Refer to Figure 1, ΔI_{CC} vs Frequency (worst case). (Referenced from 15MHz)
   The I_{CC} increases by 1.5mA per MHz for the frequency range of 16MHz up to 25MHz.
   The I_{CC} remains at a worst case for the frequency range of 26MHz up to 37MHz.
   The I_{CC} decreases by 1.0mA per MHz for the frequency range of 14MHz down to 1MHz.
   The worst case I_{CC} is calculated as follows:
   - All dedicated inputs are switching.
   - All OMCs are configured as JK flip-flops in the toggle mode. . .all are toggling.
   - All 12 outputs are disabled.
   - The number of product terms connected does not impact the I_{CC}.
7. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.

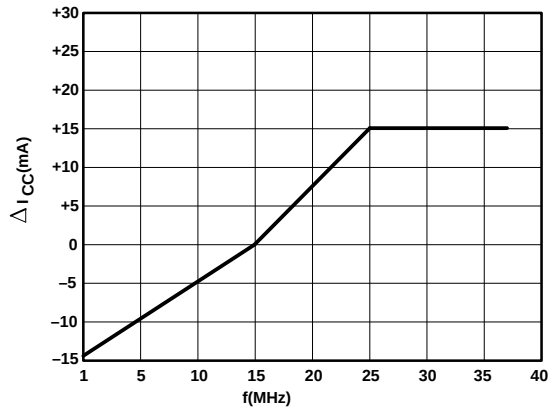


Figure 1. ΔI_{CC} vs Frequency (Worst Case) (Referenced from 15MHz)

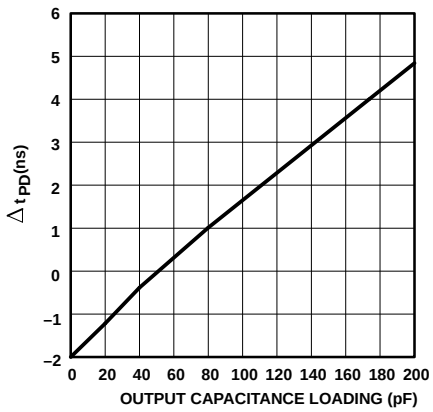


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12 MIN	PLC42VA12 TYP[1]	PLC42VA12 MAX	UNIT
Set-up Time								
t_{IS1}	Input; dedicated clock	(I, B, M) +/–	CK+	50	23	16		ns
t_{IS2}	Input; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	20	13		ns
t_{IS3}[3]	Preload; dedicated clock	(M) +/–	CK+	50	10	3.5		ns
t_{IS4}[3]	Preload; P-term clock	(M) +/–	(I, B, M) +/–	50	2	–1.0		ns
t_{IS5}[3]	Input through complement array; dedicated clock	(I, B, M) +/–	CK+	50	50	34		ns
t_{IS6}[3]	Input through complement array; P-term clock	(I, B, M) +/–	(I, B, M) +/–	50	40	30		ns
Propagation Delay								
t_{PD1}	Propagation Delay	(I, B, M) +/–	(I, B, M) +/–	50		20	35	ns
t_{PD2}	Propagation Delay with complement array (2 passes)	(I, B,) +/–	(I, B, M) +/–	50		36	55	ns
t_{CKO1}	Clock to Output; Dedicated clock	CK+	(M) +/–	50		13	17	ns
t_{CKO2}	Clock to output; P-term clock	(I, B, M) +/–	(M) +/–	50		18	27	ns
t_{RP1}	Registered operating period; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		29	40	ns
t_{RP2}	Registered operating period; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		31	47	ns
t_{RP3}[3]	Register preload operating period; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50		16.5	27	ns
t_{RP4}[3]	Register preload operating period; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50		17	29	ns
t_{RP5}[3]	Registered operating period with complement array; dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50		47	67	ns
t_{RP6}[3]	Registered operating period with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50		48	67	ns
t_{OE1}	Output Enable; from /OE pin[4]	/OE –	(M) +/–	50		10	20	ns
t_{OE2}	Output Enable; from P-term[4]	(I, B, M) +/–	(B, M) +/–	50		12.5	25	ns
t_{OD1}	Output Disable; from /OE pin[4]	/OE +	Outputs disabled	5		10	20	ns
t_{OD2}	Output Disable; from P-term[4]	(I, B, M) +/–	Outputs disabled	5		14.5	25	ns
t_{PRO}[3]	Preset to Output	(I, B, M) +/–	(M) +/–	50		25	35	ns
t_{PPR}[3]	Power-on Reset (Mn = 1)	V_{CC} +	(M) +/–	50			15	ns
Hold Time								
t_{IH1}	Input (Dedicated clock)	CK+	(I, B, M) +/–	50	0	–13		ns
t_{IH2}	Input (P-term clock)	(I, B, M) +/–	(I, B, M) +/–	50	5	–7.5		ns
t_{IH3}[3]	Input; from Mn (Dedicated clock)	CK+	(M) +/–	50	5	–1.5		ns
t_{IH4}[3]	Input; from Mn (P-term clock)	(I, B, M) +/–	(M) +/–	50	10	3.5		ns
Pulse Width								
t_{CKH1}	Clock High; Dedicated clock	CK+	CK–	50	10	5		ns
t_{CKL1}	Clock Low; Dedicated clock	CK–	CK+	50	10	5		ns
t_{CKH2}	Clock High; P-term clock	CK+	CK–	50	15	7		ns
t_{CKL2}	Clock Low; P-term clock	CK–	CK+	50	15	7		ns
t_{PRH}[3]	Width of preset/reset input pulse	(I, B, M) +/–	(I, B, M) +/–	50	30	7		ns

Notes on page 80.

AC ELECTRICAL CHARACTERISTICS (Continued)

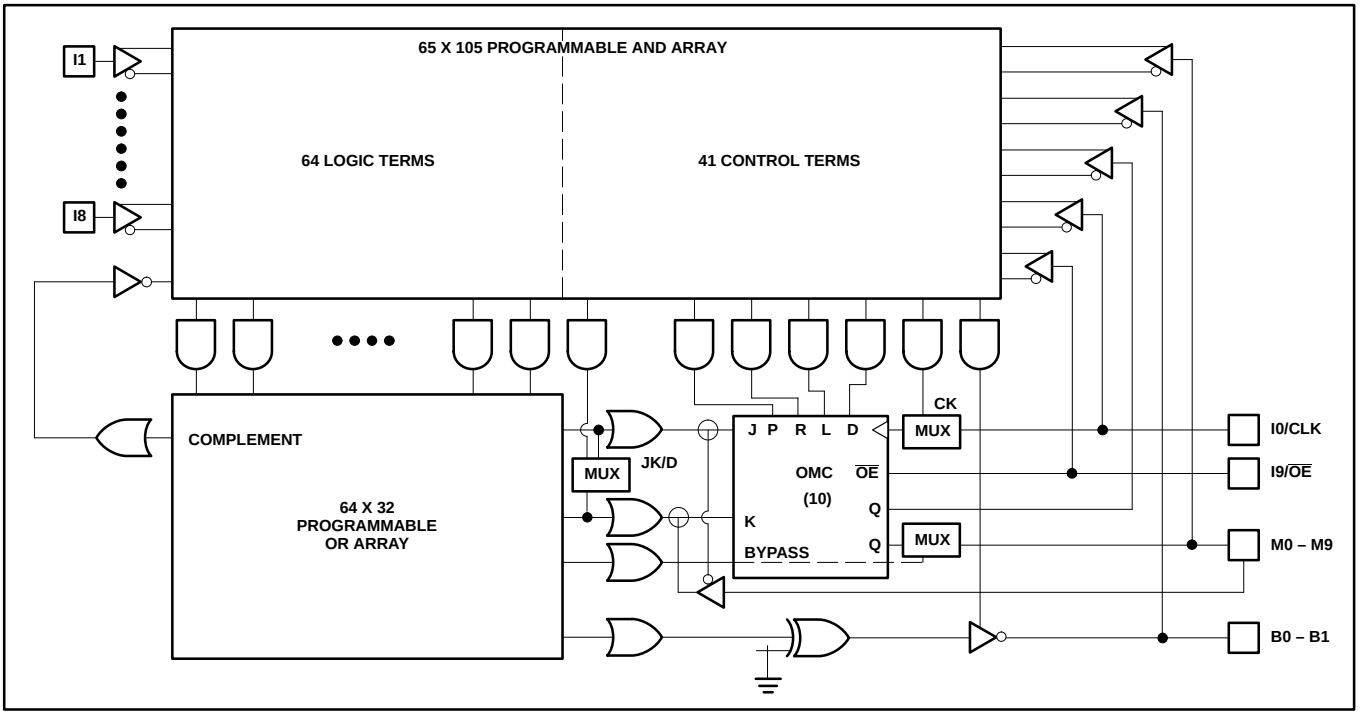
$0°C \le T_{amb} \le +75°C$, $4.75V \le V_{CC} \le 5.25V$; $R_1 = 238\Omega$, $R_2 = 170\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST[2] CONDITION (C_L (pF))	PLC42VA12 MIN	PLC42VA12 TYP[1]	PLC42VA12 MAX	UNIT
Frequency of Operation								
f_{CK1}	Dedicated clock frequency	C+	C+	50	50	100		MHz
f_{CK2}	P-term clock frequency	C+	C+	50	33	71.4		MHz
f_{MAX1}	Registered operating frequency; Dedicated clock ($t_{IS1} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	25	34.5		MHz
f_{MAX2}	Registered operating frequency; P-term clock ($t_{IS2} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	21.3	32.3		MHz
f_{MAX3}[3]	Register preload operating frequency; Dedicated clock ($t_{IS3} + t_{CKO1}$)	(M) +/–	(M) +/–	50	37	60.6		MHz
f_{MAX4}[3]	Register preload operating frequency; P-term clock ($t_{IS4} + t_{CKO2}$)	(M) +/–	(M) +/–	50	34.5	58.8		MHz
f_{MAX5}[3]	Registered operating frequency with complement array; Dedicated clock ($t_{IS5} + t_{CKO1}$)	(I, B, M) +/–	(M) +/–	50	14.9	21.3		MHz
f_{MAX6}[3]	Registered operating frequency with complement array; P-term clock ($t_{IS6} + t_{CKO2}$)	(I, B, M) +/–	(M) +/–	50	14.9	20.8		MHz

NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$. These limits are not tested/guaranteed.
2. Refer also to AC Test Conditions (Test Load Circuit).
3. These limits are not tested, but are characterized periodically and are guaranteed by design.
4. For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.

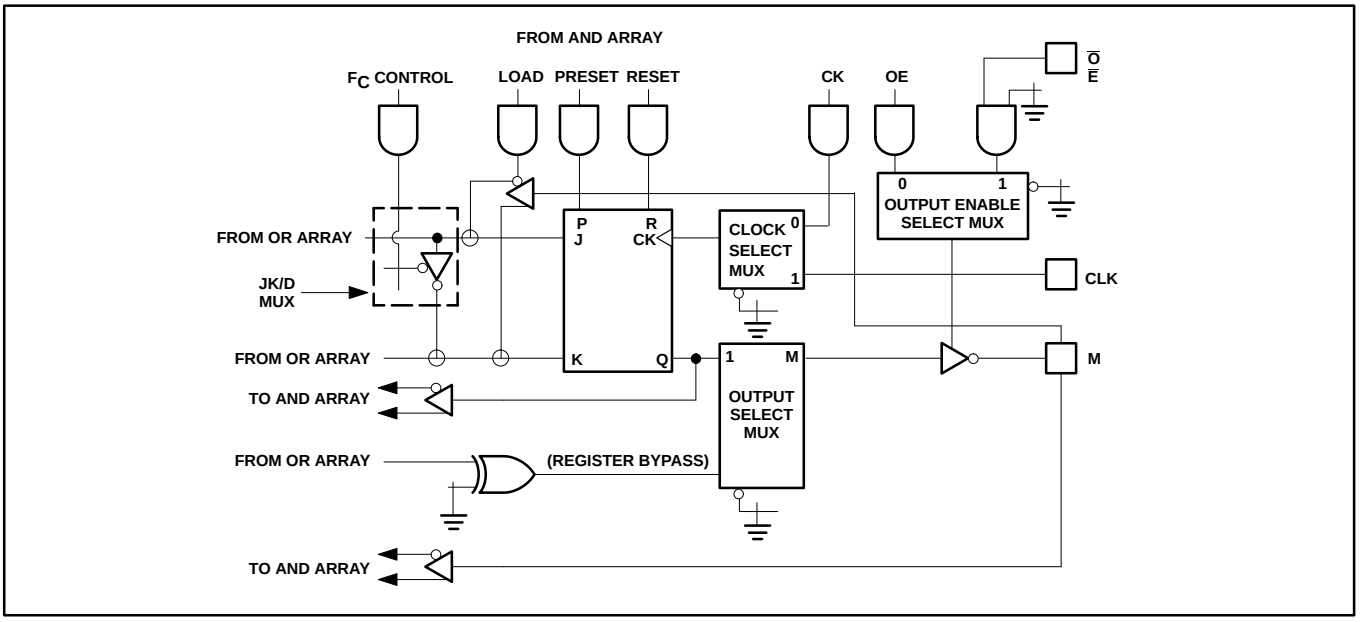
BLOCK DIAGRAM



CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

OUTPUT MACRO CELL (OMC)



Output Macro Cell Configuration

Philips Semiconductors unique Output Macro Cell design represents a significant advancement in the configurability of multi-function Programmable Logic Devices.

The PLC42VA12 has 10 programmable Output Macro Cells. Each can be individually programmed in any of 5 basic configurations:

- Dedicated I/O (combinatorial) with feedback to AND array
- Dedicated Input
- Combinatorial I/O with feedback and Buried Register with feedback (register bypass)
- Registered Input
- Registered Output with feedback

Each of the registered options can be further customized as J-K type or D-type, with either an internally derived clock (from the AND array) or clocked from an external source. With these additional programmable options, it is possible to program each Output Macro Cell in any one of 14 different configurations.

These 14 configurations, combined with the fully programmable OR array, make the PLC42VA12 the most versatile and silicon efficient of all the Output Macro Cell-type PLDs.

The most significant Output Macro Cell (OMC) feature is the implementation of the register bypass function. Any of the 10 J-K/D registers can be individually bypassed, thus creating a combinatorial I/O path from the AND array to the output pin. Unlike other Output Macro Cell-type devices, the register in the OMC is fully functional as a buried register. Furthermore, both the combinatorial I/O and the buried register have separate input paths (from the AND array) and separate feedback paths (to the AND array). This feature provides the capability to operate the buried register independently from the combinatorial I/O.

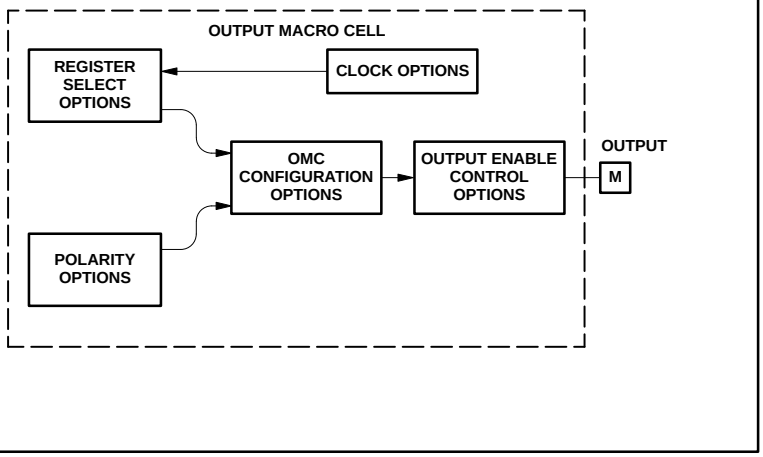
The PLC42VA12 is ideally suited for both synchronous and asynchronous logic functions. Eleven clock sources – 10 driven from the AND array and one from an external source – make it possible to design synchronous state machine functions, event-driven state machine functions and combinatorial (asynchronous) functions all on the same chip.

Sophisticated control functions support individual OE control and Reset functions from the AND array. OE control is also available from the I9/$\overline{OE}$ pin. Register Preset and Load functions are controlled from the AND array, in 2 banks of 4 for OMCs M1 – M8. Output Macro Cells M0 and M9 have individual Preset and Load Control terms.

Output Polarity for the combinatorial I/O paths is configurable via 12 programmable EX-OR gates. The output of each register can be configured as inverting (active Low) or non-inverting (active High) via manipulation of the logic equations.

The output of each buried register can also be configured as inverting or non-inverting via the input buffer which feeds back to the AND array.

OUTPUT MACRO CELL PROGRAMMABLE OPTIONS



OMC Programmable Options

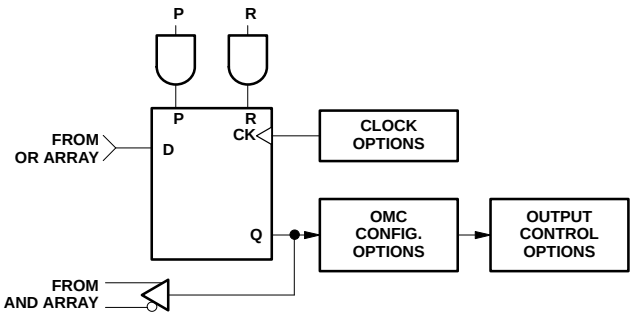
For purposes of programming, the Output Macro Cell should be considered to be partitioned into five separate blocks. As shown in the drawing titled “Output Macro Cell Programmable Options”, the programmable blocks are: Register Select Options, Polarity Options, Clock Options, OMC Configuration Options and Output Enable Control Options.

There is one programmable location associated with each block except the Output Enable Control block which has two programmable fuse locations per OMC.

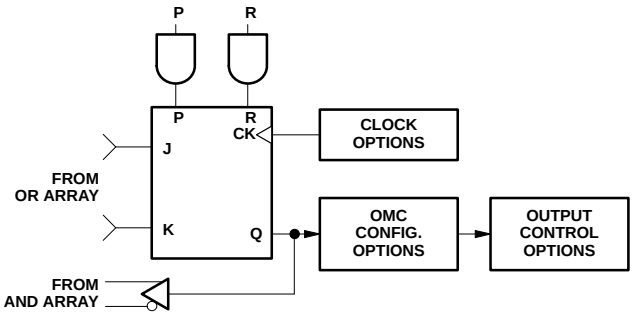
The following drawings detail the options associated with each programmable block. The associated programming codes are also included. The table titled “Output Macro Cell Configurations” (page 87) lists all the possible combinations of the five programmable options.

ARCHITECTURAL OPTIONS

REGISTER SELECT OPTIONS



REGISTER MODE (D or JK)	CODE
D-TYPE	A
F_C CONTROL P-TERM	L



REGISTER MODE (D or JK)	CODE
JK-TYPE	●
F_C CONTROL P-TERM	–

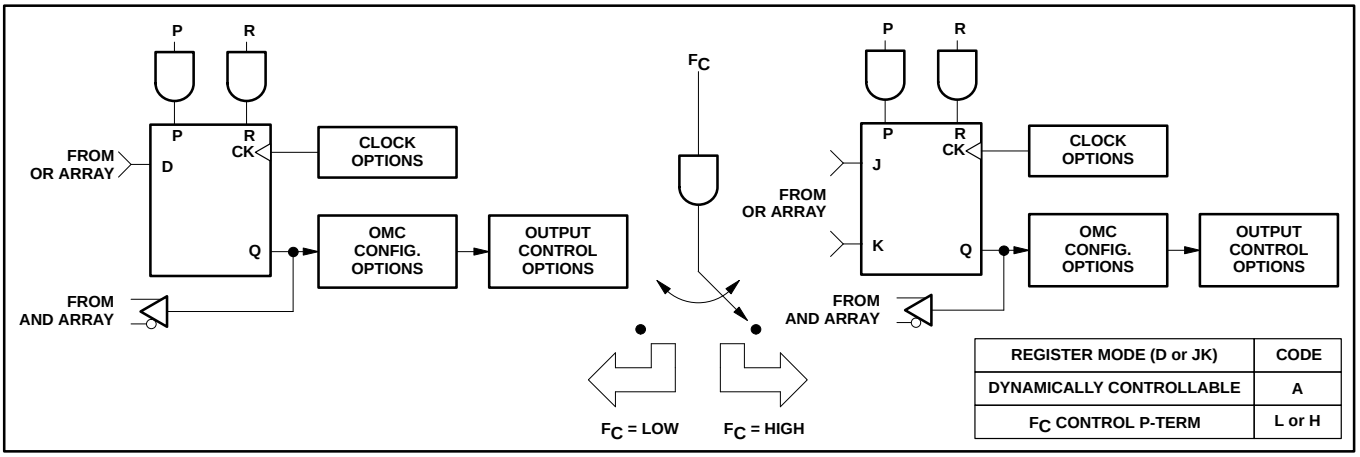
Register Select Options

Each OMC Register can be configured either as a dedicated D-type or a J-K flip-flop. The Flip-Flop Control term, Fc, provides the option to control each Register dynamically—switching from D-type to J-K type, based on the Fc control signal.

Register Preset and Reset are controlled from the AND array. Each OMC has an individual Reset Control term (RMn). The Register Preset function is controlled in two banks of 4 for OMCs M1 – M3 and M4 – M8 (via the control terms PA and PB). OMCs M0 and M9 have individual control terms (PM0 and PM9 respectively).

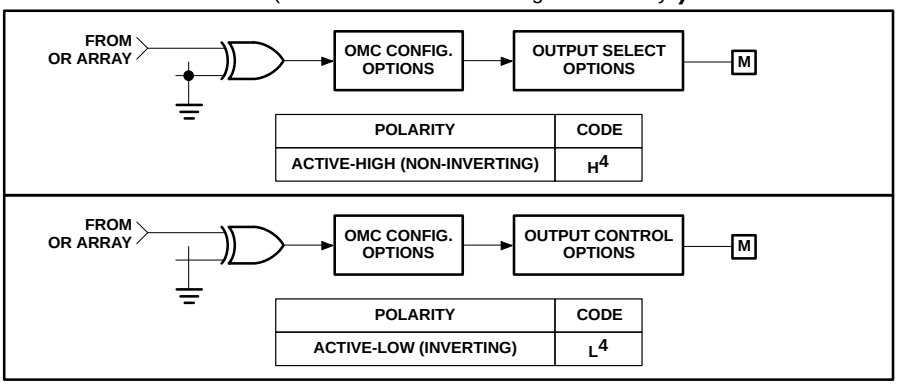
Notes on page 87.

REGISTER SELECT OPTIONS (Continued)



REGISTER MODE (D or JK)	CODE
DYNAMICALLY CONTROLLABLE	A
F_C CONTROL P-TERM	L or H

POLARITY OPTIONS (for Combinatorial I/O Configurations Only[1])



POLARITY	CODE
ACTIVE-HIGH (NON-INVERTING)	H[4]

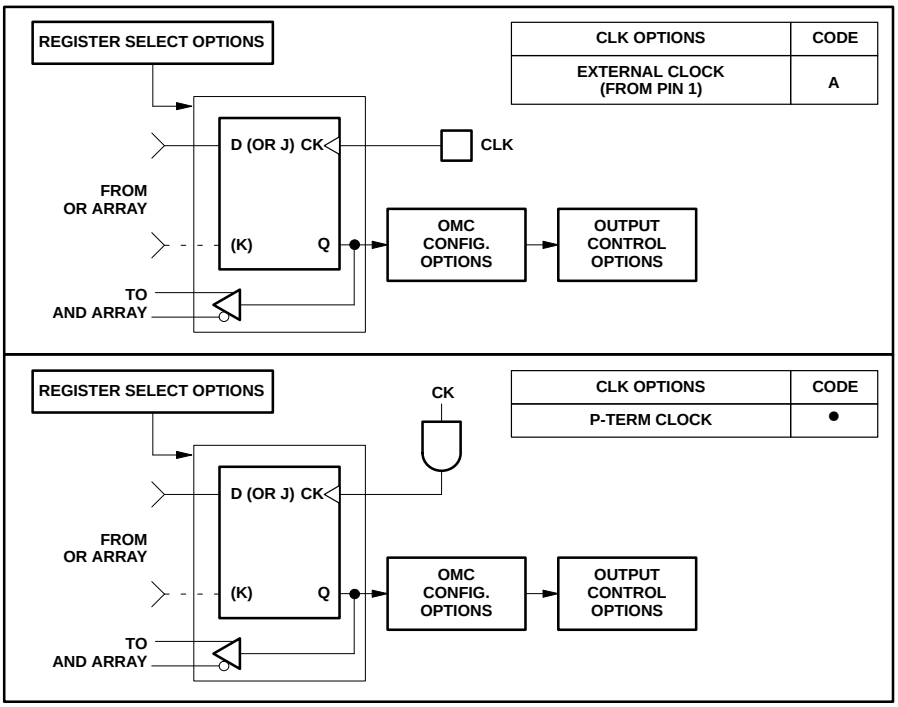
POLARITY	CODE
ACTIVE-LOW (INVERTING)	L[4]

Polarity Options

When an OMC is configured as a Combinatorial I/O with Buried Register, the polarity of the combinatorial path can be programmed as Active-High or Active-Low. A configurable EX-OR gate provides polarity control.

If an OMC is configured as a Registered Output, /Q is propagated to the output pin. Note that either Q or /Q can be fedback to the AND array by manipulating the feedback logic equations. (TRUE or COMPLEMENT).

CLOCK OPTIONS



CLK OPTIONS	CODE
EXTERNAL CLOCK (FROM PIN 1)	A

CLK OPTIONS	CODE
P-TERM CLOCK	•

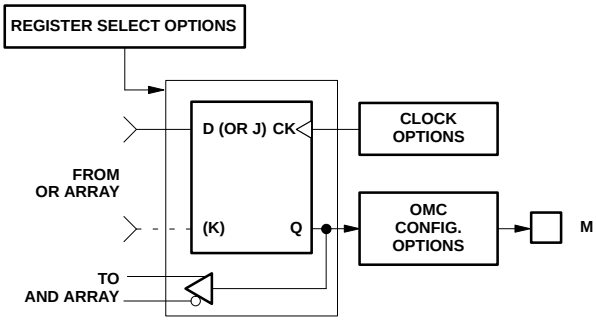
Clock Options

In the unprogrammed state, all Output Macro Cell clock sources are connected to the External Clock pin (I_0/CLK pin 1). Each OMC can be individually programmed such that its P-term Clock (CK_n) is enabled, thus disabling it from the External Clock and providing event-driven clocking capability.

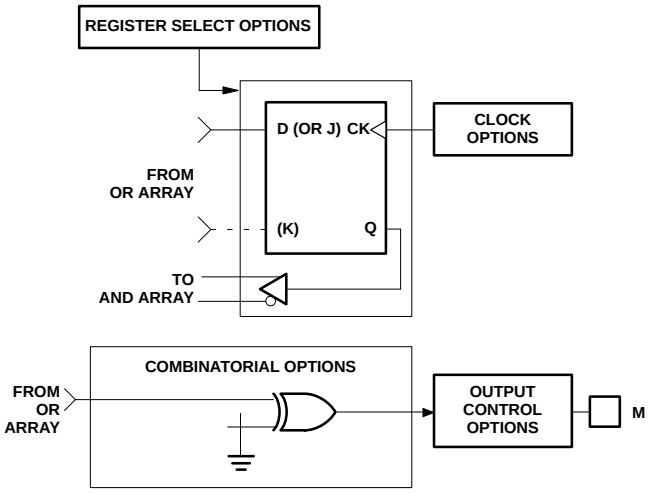
This feature supports multiple state machines, clocked at several different rates, all on one chip, or the ability to collect large amounts of random logic, including 10 separately clocked flip-flops.

Notes on page 87.

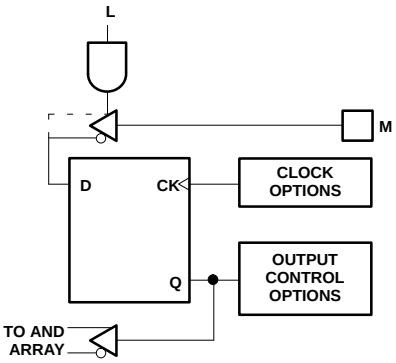
OUTPUT MACRO CELL CONFIGURATION OPTIONS



OMC CONFIGURATION	CODE
REGISTERED OUTPUT (D or JK)	A



OMC CONFIGURATION	CODE
COMBINATORIAL OUTPUT WITH BURIED REGISTER (D or JK)	●



OMC CONFIGURATION	CODE
REGISTERED INPUT	A or ●[5]
LOAD CONTROL P-TERM	H[6]

Notes on page 87.

OMC Configuration Options

Each OMC can be configured as a Registered Output with feedback, a Registered Input or a Combinatorial I/O with Buried Register. Dedicated Input and dedicated I/O configurations are also possible.

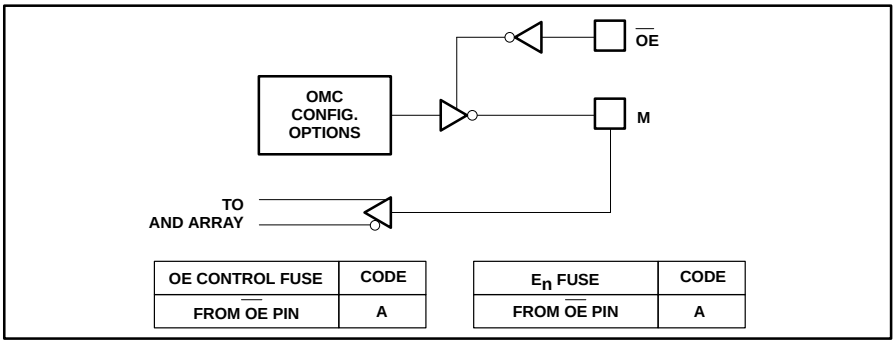
When the Combinatorial I/O option is selected, (the Register Bypass option), the Buried Register remains 100% functional, with its own inputs from the AND array and a separate feedback path. This unique feature is ideal for designing any type of state machine; synchronous Mealy-types that require both Buried and Output Registers, or asynchronous Mealy-types that require buried registers and combinatorial output functions. Both synchronous and asynchronous Moore-type state machines can also be easily accommodated with the flexible OMC structure.

Note that an OMC can be configured as either a Combinatorial I/O (with Buried Register) or a Registered Output with feedback and it can still be used as a Registered Input. By disabling the outputs via any OE control function, the M pin can be used as an input. When the Load Control P-term is asserted HIGH, the register is preloaded from the M pin(s). When the L_C P-term is Active-Low and the output is enabled, the OMC will again function as configured (either a combinatorial I/O or a registered output with feedback). This feature is suited for synchronizing input signals prior to commencing a state sequence.

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

OUTPUT CONTROL OPTIONS



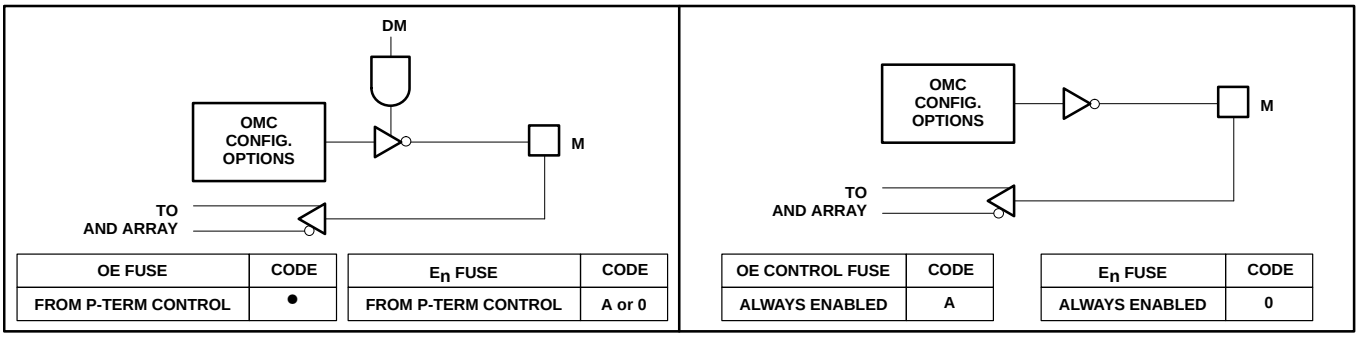
OE CONTROL FUSE	CODE
FROM $\overline{OE}$ PIN	A

E_n FUSE	CODE
FROM $\overline{OE}$ PIN	A

Output Enable Control Options

Similar to the Clock Options, the Output Enable Control for each OMC can be connected either to an external source (I9/$\overline{OE}$, pin 13) or controlled from the AND array (P-terms DM_n). Each Output can also be permanently enabled.

Output Enable control for the two bi-directional I/O (B pins 10 and 11) is from the AND array only (P-terms DB0 and DB1 respectively).



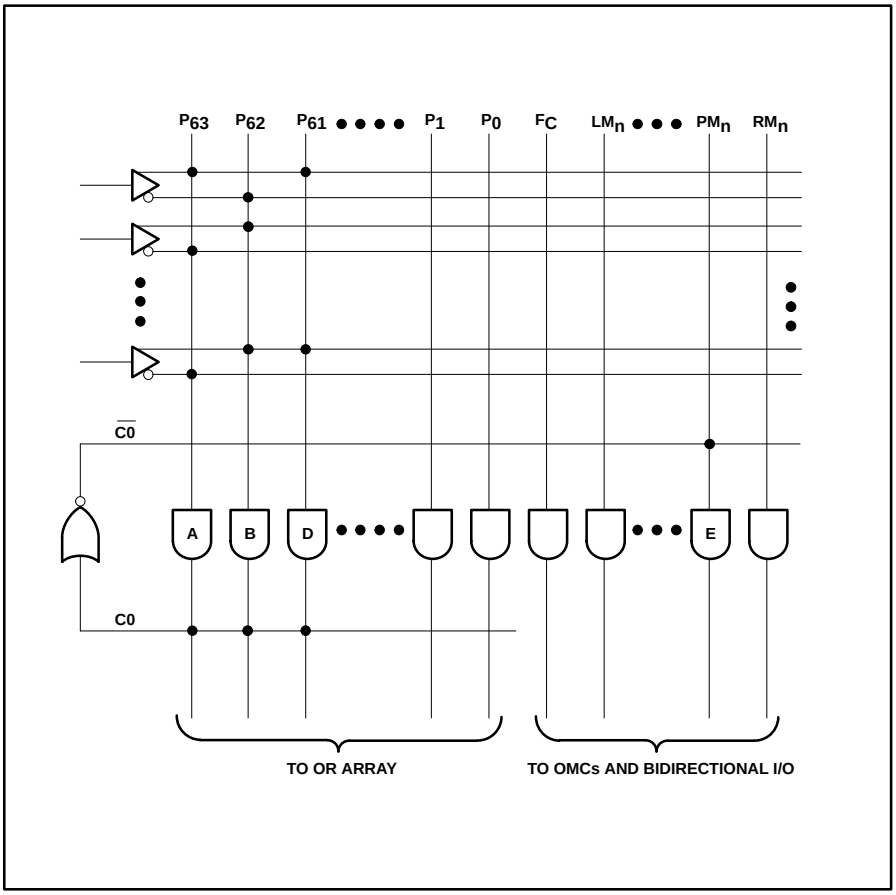
OE FUSE	CODE
FROM P-TERM CONTROL	●

E_n FUSE	CODE
FROM P-TERM CONTROL	A or 0

OE CONTROL FUSE	CODE
ALWAYS ENABLED	A

E_n FUSE	CODE
ALWAYS ENABLED	0

COMPLEMENT ARRAY DETAIL



Notes on page 87.

Complement Array Detail

The complement array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A * /B * /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The complement array is a single OR gate with inputs from the AND array. The output of the complement array is inverted and fedback to the AND array (NOR function). The output of the array will be LOW if any one or more of the AND terms connected to it are active (HIGH). If, however, all the connected terms are inactive (LOW), which is a classic unknown state, the output of the complement array will be HIGH.

Consider the product terms A, B and D that represent defined states. They are also connected to the input of the complement array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to product term E, which could be used in turn to preset the state machine to known state. Without the complement array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, such an approach can be prohibitive, both in terms of time and wasted resources.

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

LOGIC PROGRAMMING

The PLC42VA12 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ and CUPL™ design software packages also support the PLC42VA12 architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLC42VA12 logic designs can also be generated using the program table entry format, which is detailed on the following pages. This program table entry format is supported by SNAP only.

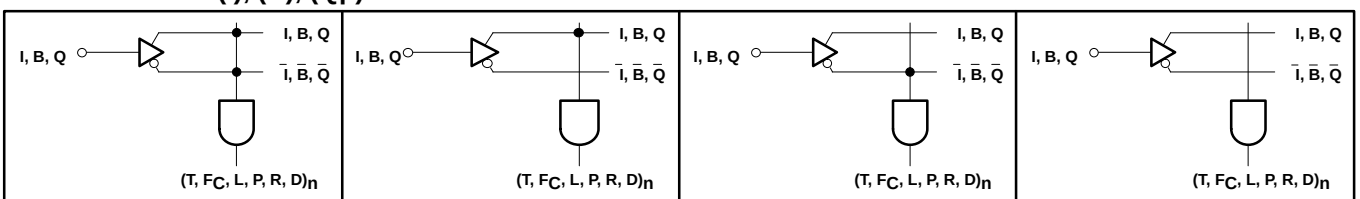
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below. Symbols for OMC configuration have been previously defined in the Architectural Options section.

PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-party Programmer/ Software Support)* of this data handbook for additional information.

LOGIC IMPLEMENTATION

"AND" ARRAY – (I), (B), (Qp)



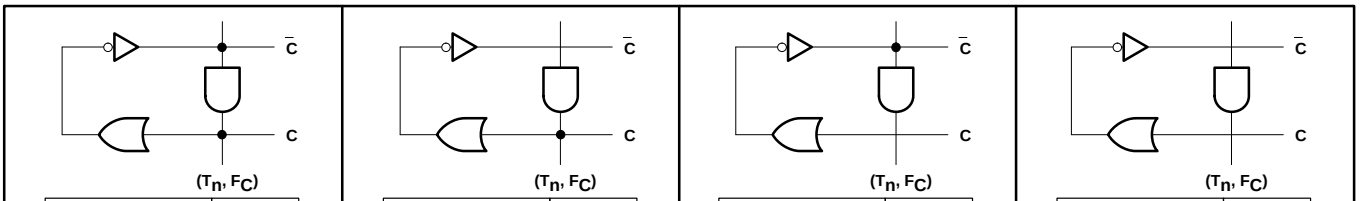
STATE	CODE
INACTIVE[1]	O

STATE	CODE
I, B, Q	H

STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

STATE	CODE
DON'T CARE	–

"COMPLEMENT" ARRAY – (C)



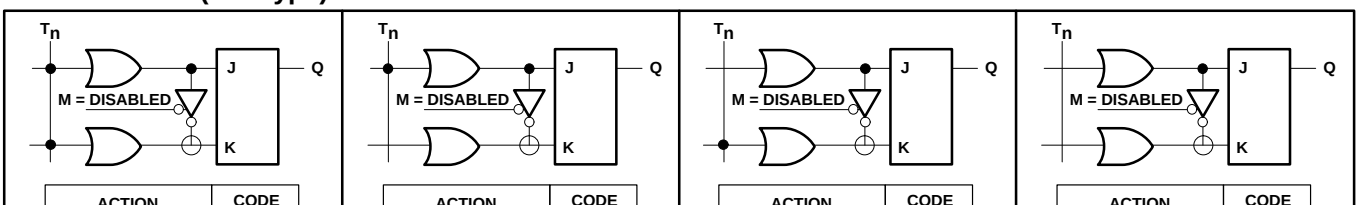
ACTION	CODE
INACTIVE[1, 3]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	●

ACTION	CODE
TRANSPARENT	–

"OR" ARRAY – (J-K Type)



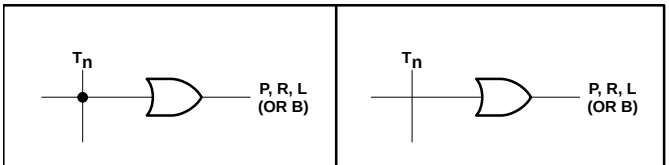
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

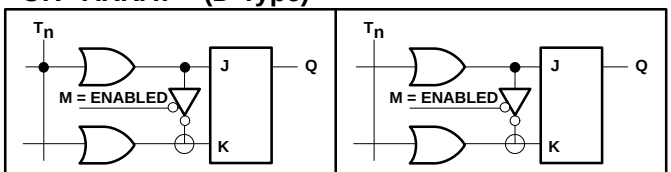
"OR" ARRAY



T_n STATUS	CODE
ACTIVE[1]	A

T_n STATUS	CODE
INACTIVE	●

"OR" ARRAY – (D-Type)



T_n STATUS	CODE
ACTIVE (SET)	A

T_n STATUS	CODE
INACTIVE (RESET)	●

Notes on page 87.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

LOGIC IMPLEMENTATION (Continued)

OUTPUT MACRO CELL CONFIGURATIONS

OUTPUT MACRO CELL CONFIGURATION	PROGRAMMING CODES			
	REGISTER SELECT FUSE	OMC CONFIGURATION FUSE	POLARITY FUSE	CLOCK FUSE
Combinatorial I/O with Buried D-type register				
External clock source	A	●	H or L	A
P-term clock source	A	●	H or L	●
Combinatorial I/O with Buried J-K type register				
External clock source	●	●	H or L	A
P-term clock source	●	●	H or L	●
Registered Output (D-type) with feedback				
External clock source	A	A	N/A	A
P-term clock source	A	A	N/A	●
Registered Output (J-K type) with feedback				
External clock source	●	A	N/A	A
P-term clock source	●	A	N/A	●
Registered Input (Clocked Preload) with feedback				
External clock source	A	A or ●[5]	Optional[5]	A
P-term clock source	A	A or ●[5]	Optional[5]	●

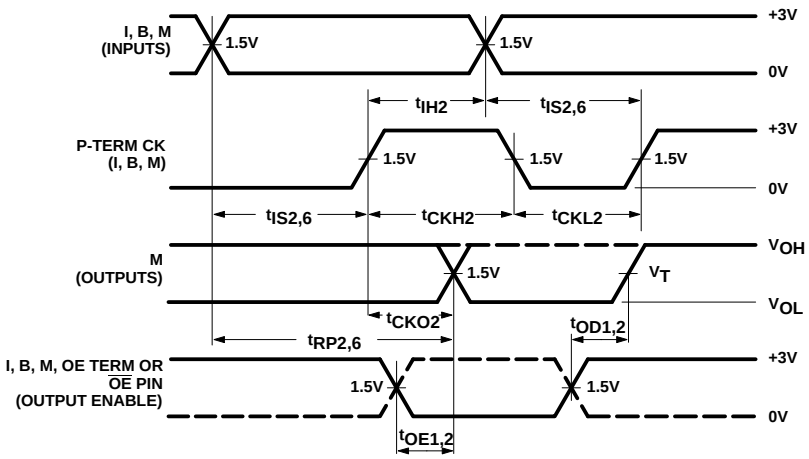
OUTPUT ENABLE CONTROL[8] CONFIGURATION	OUTPUT CONTROL FUSES		CONTROL SIGNAL
	OE CONTROL FUSE	En FUSES	
OMC controlled by /OE pin	A	A	
Output Enabled			Low
Output Disabled			High
OMC controlled by P-term	●	A or 0	
Output Enabled			High
Output Disabled			Low
Output always Enabled	A	0	Not Applicable

NOTES:
1. This is the initial (unprogrammed) state of the device.
2. Any gate will be unconditionally inhibited if both the TRUE and COMPLEMENT fuses are left intact.
3. To prevent oscillations, this state is not allowed for Complement Array fuse pairs that are coupled to active product terms.
4. The OMC Configuration fuse must be programmed as Combinatorial I/O in order to make use of the Polarity Option.
5. Regardless of the programmed state of the OMC Configuration fuse, an OMC can be used as a Registered Input. Note that the Load Control P-term must be asserted Active-High.
6. Output must be disabled.
7. Program code definitions:
   - A = Active (unprogrammed fuse)
   - 0, ● = Inactive (programmed fuse)
   - – = Don’t Care (both TRUE and COMPLEMENT fuses unprogrammed)
   - H = Active-High connection
   - L = Active-Low connection
8. OE control for B0 and B1 (Pins 10 and 11) is from the AND array only.

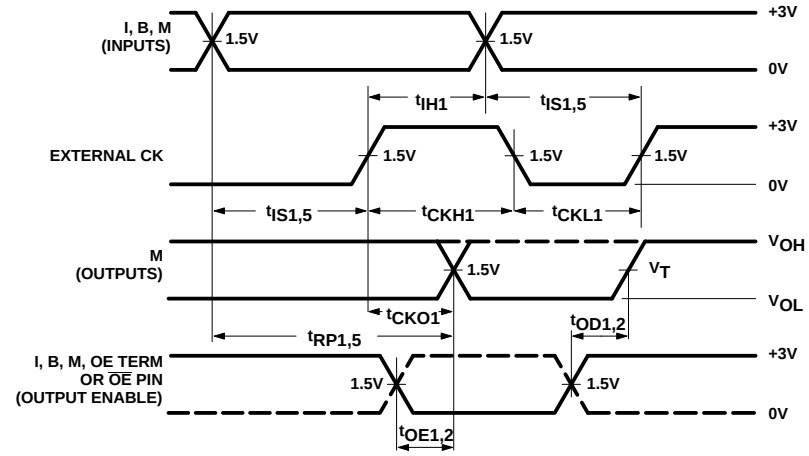
CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

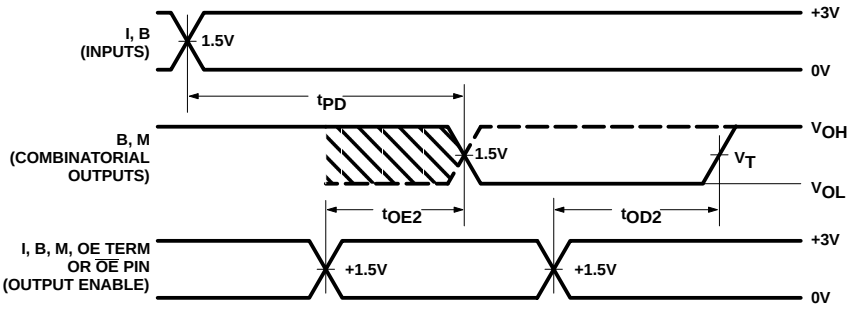
TIMING DIAGRAMS



Flip-Flop Outputs with P-term Clock



Flip-Flop Outputs with External Clock

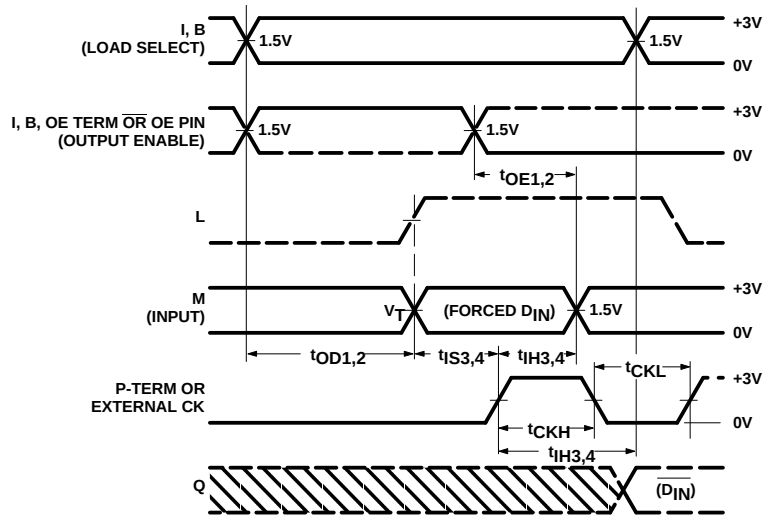


Gated Outputs

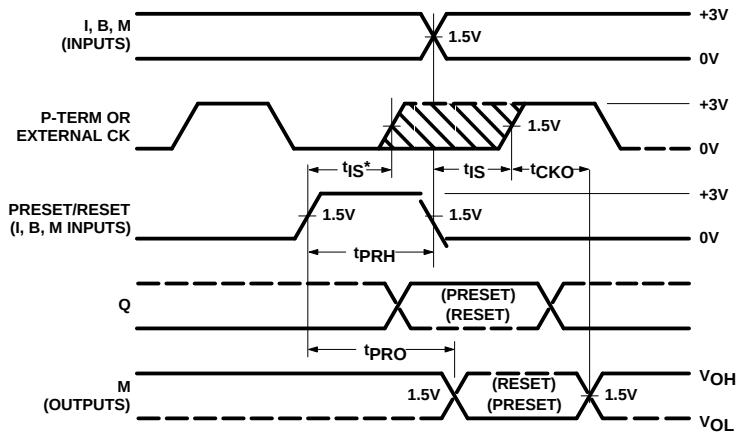
TIMING DEFINITIONS

SYMBOL	PARAMETER
f_{CK1}	Clock Frequency; External Clock
f_{CK2}	Clock Frequency; P-term Clock
t_{CKH1}	Width of Input Clock Pulse; External Clock
t_{CKH2}	Width of Input Clock Pulse; P-term Clock
t_{CKL1}	Interval between Clock pulses; External Clock
t_{CKL2}	Interval between Clock Pulses; P-term Clock
t_{CKO1}	Delay between the Positive Transition of External Clock and when M Outputs become valid.
t_{CKO2}	Delay between the Positive Transition of P-term Clock and when M Outputs become valid.
t_{RP1}	Delay between beginning of Valid Input and when the M outputs become Valid when using External Clock.
t_{RP2}	Delay between beginning of Valid Input and when the M outputs become Valid when using P-term Clock.
t_{RP3}	Delay between beginning of Valid Input and when the M outputs become Valid when using Preload Inputs (from M pins) and External Clock.
t_{RP4}	Delay between beginning of Valid Input and when the M outputs become valid when using Preload inputs (from M pins) and P-term Clock.
t_{RP5}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and External clock.
t_{RP6}	Delay between beginning of Valid Input and when the M outputs become Valid when using Complement Array and P-term Clock.
f_{MAX1}	Minimum guaranteed Operating Frequency; Dedicated Clock
f_{MAX2}	Minimum guaranteed Operating Frequency; P-term Clock
f_{MAX3}	Minimum guaranteed Operating Frequency using Preload; Dedicated Clock (M pin to M pin)
f_{MAX4}	Minimum guaranteed Operating Frequency using Preload; P-term Clock (M pin to M pin)
f_{MAX5}	Minimum guaranteed Operating Frequency using Complement Array; Dedicated Clock
f_{MAX6}	Minimum Operating Frequency using Complement Array; P-term Clock
t_{IH1}	Required delay between positive transition of External Clock and end of valid input data.

TIMING DIAGRAMS (Continued)

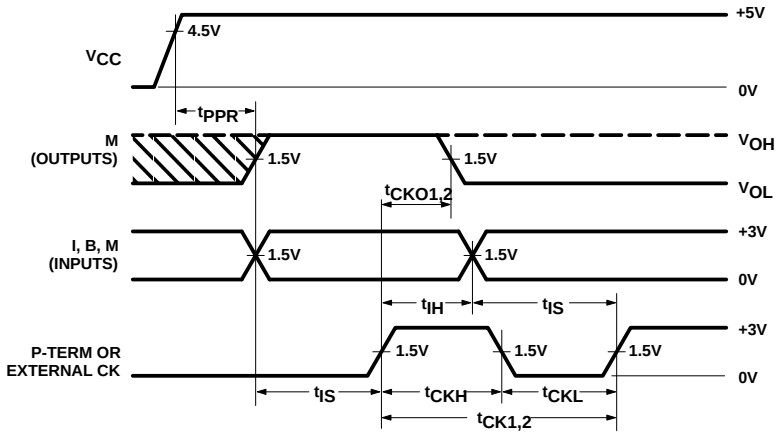


Flip-Flop Input Mode (Preload)



*Preset and Reset functions override Clock. However, M outputs may glitch with the first positive Clock Edge if t_{IS} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Power-On Reset

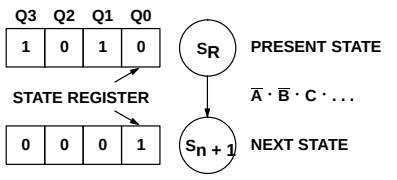
TIMING DEFINITIONS (Continued)

SYMBOL	PARAMETER
t_{IH2}	Required delay between positive transition of P-term Clock and end of valid input data.
t_{IH3}	Required delay between positive transition of External Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IH4}	Required delay between positive transition of P-term Clock and end of valid input data when using Preload Inputs (from M pins).
t_{IS1}	Required delay between beginning of valid input and positive transition of External Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of P-term Clock input.
t_{IS3}	Required delay between beginning of valid Preload input (from M pins) and positive transition of External Clock.
t_{IS4}	Required delay between beginning of valid Preload input (from M pins) and positive transition of P-term Clock input.
t_{IS5}	Required delay between beginning of valid input through Complement Array and positive transition of External Clock.
t_{IS6}	Required delay between beginning of valid input through Complement Array and positive transition of P-term Clock input.
t_{OE1}	Delay between beginning of Output Enable signal (Low) from /OE pin and when Outputs become valid.
t_{OE2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable signal (HIGH) from /OE pin and when Outputs become disabled.
t_{OD2}	Delay between beginning of Output Enable signal (High or Low) from OE P-term and when Outputs become disabled.
t_{PD}	Delay between beginning of valid input and when the Outputs become valid (Combinatorial Path).
t_{PRH}	Width of Preset/Reset Pulse.
t_{PRO}	Delay between beginning of valid Preset/Reset Input and when the registered Outputs become Preset (“1”) or Reset (“0”).
t_{PPR}	Delay between V_{CC} (after power-up) and when flip-flops become Reset to “0”. Note: Signal at Output (M pin) will be inverted.

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

LOGIC FUNCTION



SET Q_0: $J_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

RESET Q_3: $J_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

NOTE:
Similar logic functions are applicable for D mode flip-flops.

FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L_n	CK_n	P_n	R_n	J	K	Q	M
H								Hi-Z
L	X	X	X	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:
1. Positive Logic:
   $J\text{-}K = T_0 + T_1 + T_2 + \ldots + T_{31}$
   $T_n = \overline{C} \cdot (I0 \cdot I1 \cdot I2\ldots) \cdot (Q0 \cdot Q1\ldots) \cdot (B0 \cdot B1\ldots)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at M_n pin for loading the J-K flip-flop in the Input mode. The load control term, L_n must be enabled (HIGH) and the p-terms that are connected to the associated flip-flop must be forced LOW (disabled) during Preload.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop (Diagnostic mode).

PLC42VA12 UNPROGRAMMED STATE

A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

The following are:

ACTIVE:
- OR array logic terms
- Output Macro Cells M1 – M8;
  - D-type registered outputs (D = 0)
- External clock path
- Inputs: B0, B1, M0, M9

INACTIVE:
- AND array logic and control terms (except flip-flop mode control term, F_C)
- Bidirectional I/O (B0, B1);
  - Inputs are active. Outputs are 3-Stated via the OE P-terms, D0 and D1.
  - D-type registers (D = 0).
- Output Macro Cells M0 and M9;
  - Bidirectional I/O, 3-Stated via the OE P-terms, DM0 and DM9. The inputs are active.
- P-term clocks
- Complement Array
- J-K Flip-Flop mode

PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-party Programmer/ Software Support)* in this data handbook for additional information.

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

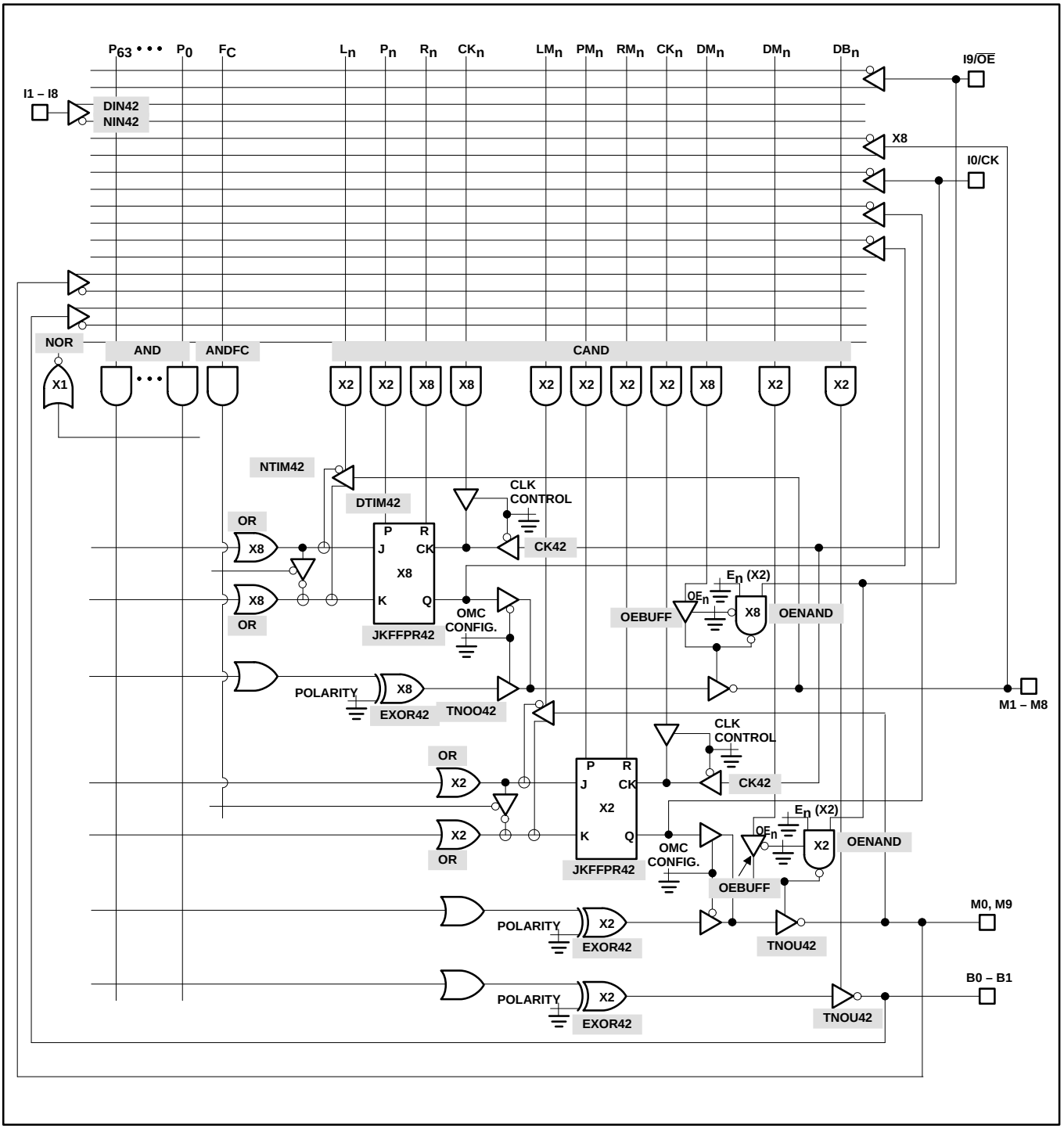
The erasure characteristics of the PLC42VA12 devices are such that erasure begins to occur upon exposure to light with wavelength shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 – 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC42VA12 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC42VA12 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC42VA12 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retentions exceeds 20 years.

PROGRAM TABLE

CMOS programmable multi-function PLD (42 × 105 × 12)

PLC42VA12

SNAP RESOURCE SUMMARY DESIGNATIONS