National Semiconductor

PRELIMINARY

NMC9816A 16,384-Bit (2k x 8) E²PROM

General Description

The NMC9816A is a fast 5V-only E²PROM which offers many desired features, making it ideally suited for efficiency and ease in system design. The added features on the NMC9816A include: 5V-only operation provided by an on-chip V_{PP} generator during erase-write; address and data latches to reduce part count and to free the microprocessor while the chip is busy doing erase-write; and automatic erase before byte-write. It can meet applications requiring up to 10^4 write cycles per byte. The NMC9816A is a product of National's advanced E²PROM stepper technology and uses the powerful XMOS™ process for reliable, non-volatile data storage.

The NMC9816A sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip address and data latching further enhances system performance.

The NMC9816A also features $\overline{DATA}$ Polling, which enables the E²PROM to signal the processor that a write operation is complete without requiring the use of any external hardware.

Improved data protection during V_{CC} power up/down transitions is provided by an on-chip V_{CC} sensing circuit which disables the initiation of all 5V-only programmable modes when V_{CC} is less than 4 volts.

The NMC9816A's very fast read access times make it compatible with high performance microprocessor applications. It uses the proven two line control architecture which eliminates bus contention in a system environment.

An optional high voltage chip erase feature is provided for quick erasure of the memory data pattern in a single 9 msec Chip Erase Cycle.

The density, and level of integrated control, make the NMC9816A suitable for users requiring minimum hardware overhead, high systems performance, minimal board space and design ease. Designing with and using the NMC9816A is extremely cost effective as the required high voltage and interfacing hardware required for other E²PROM devices has been eliminated by 5V-only operation and on-chip latches. See *Figures 1, 2,* and *3* for the NMC9816A block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply
- Self-timed byte-write with auto erase
- On-chip address and data latches
- On-chip power up/down protection
- Two line output control
- TRI-STATE® outputs
- Data polling verification
- High voltage chip erase
- Fast byte-writing
  - Write cycle (2 ms typical)
  - E/W cycle (4 ms typical)
- Very fast access time
  - NMC9816A-20—200 ns
  - NMC9816A-25—250 ns
  - NMC9816A-35—350 ns
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams

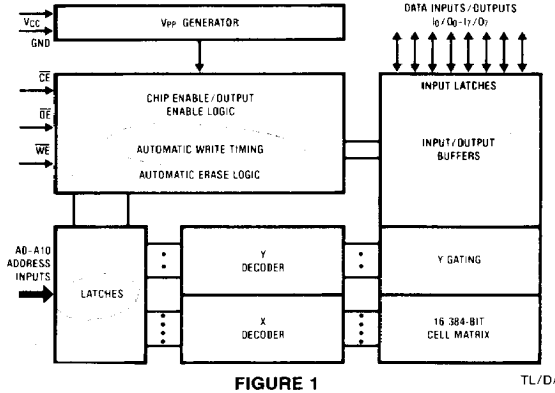

FIGURE 1

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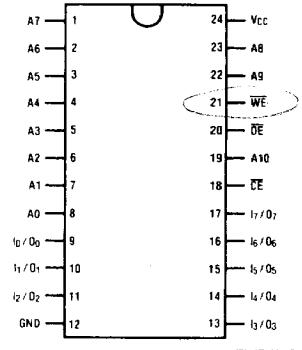
Pin Names

A0–A10	Addresses	O_0–O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0–I_7	Data Inputs
$\overline{OE}$	Output Enable	$\overline{WE}$	Write Enable

Dual-In-Line Package



Top View

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FIGURE 2

Order Number NMC9816A-20, NMC9816A-25 or NMC9816A-35
See NS Package Number J24A or N24A

Absolute Maximum Ratings

Temperature Under Bias
- NMC9816A: −10°C to +80°C
- NMC9816AE: −50°C to +95°C
- NMC9816AM: −65°C to +135°C

Storage Temperature: −65°C to +150°C

All Input or Output Voltages with Respect to Ground: +6V to −0.3V

Lead Temp. (Soldering, 10 seconds): 300°C

Operating Conditions

Temperature Range
- NMC9816A: 0°C to +70°C
- NMC9816AE: −40°C to +85°C
- NMC9816AM: −55°C to +125°C

V_{CC} Power Supply (Notes 2 and 3)
- NMC9816A: 5V ±5%
- NMC9816AE: 5V ±10%
- NMC9816AM: 5V ±10%

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Electrical Characteristics T_A for NMC9816A = 0°C to +70°C, V_{CC} = 5V ±5% (Note 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
I_{LI}	Input Leakage Current NMC9816A NMC9816AE NMC9816AM	GND to V_{CC}			10 10 10	µA
I_{LO}	Output Leakage Current NMC9816A NMC9816AE NMC9816AM	GND to V_{CC}			10 10 10	µA
I_{CCA}	V_{CC} Current (Active) NMC9816A NMC9816AE NMC9816AM	$\overline{CE} = \overline{OE} = V_{IL}$		40 40 40	80 100 100	mA
I_{CCS}	V_{CC} Current (Standby) NMC9816A NMC9816AE NMC9816AM	$\overline{CE} = V_{IH}$		12 12 12	25 30 30	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage NMC9816A NMC9816AE NMC9816AM		2.0 2.2 2.2		V_{CC} + 1 V_{CC} + 1 V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA	2.4			V
WRITE OPERATION						
I_{CCW}	V_{CC} Current (Write) NMC9816A NMC9816AE NMC9816AM			40 40 40	80 100 100	mA
V_{LKO}	V_{CC} Level for Write Lockout		4.0			V
HIGH VOLTAGE CHIP ERASE						
V_{ER}	$\overline{OE}$ and $\overline{WE}$ Voltage in Chip Erase Mode		12		22	V

Capacitance T_A = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V		5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V			10	pF

AC Test Conditions

Output Load	1 TTL gate and $C_L = 100$ pF	Timing Measurement Reference Level	
Input Pulse Levels	0.45V to 2.4V	Input	1V and 2V
		Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	NMC9816A-20			NMC9816A-25			NMC9816A-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		75	10		100	10		120	ns
t_{DF}	Output Disable to Output Float	$\overline{CE}$ or $\overline{OE} = V_{IL}$	0		80	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$, $\overline{OE} = V_{IL}$	0			0			0			ns

Write Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to Write Set-Up Time		20			ns
t_{CS}	$\overline{CE}$ to Write Set-Up Time		20			ns
t_{WP} (Note 6)	Write Pulse Width		150			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	50			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	20			ns
t_{CH}	$\overline{CE}$ Hold Time		20			ns
t_{DL}	Data Latch Time		50			ns
t_{WC}	Byte-Write Cycle Time			4	10	ms
t_{OES}	Output Enable Setup Time		10			ns
t_{OEH}	Output Enable Hold Time		10			ns

High Voltage Chip Erase AC Electrical Characteristics (Note 5)

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2, 3 & 7)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{CS}	$\overline{CE}$ Set-Up Time	$\overline{WE} = 6V$	10			ns
t_{OS}	Output Enable Set-Up Time	$\overline{WE} = 6V$	10			ns
t_{OH}	Output Enable Hold Time	$\overline{WE} = 6V$	1			μs
t_{WR}	Write Recovery Time	$\overline{WE} = 6V$	1			μs
t_{WP}	Chip Erase Pulse Width	$\overline{WE} = V_{ER}$	9		15	ms

Note 1: This parameter only sampled and not 100% tested.

Note 2: To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be applied simultaneously or before $V_{CC} = 4V$. $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be removed simultaneously or after V_{CC} falls before 4V.

Note 3: To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

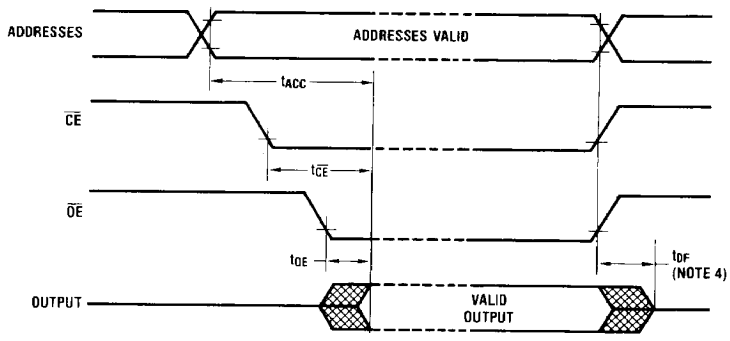
Note 5: Low voltage V_{CC} sense circuit does not inhibit the high voltage Chip Erase feature.

Note 6: $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.

Note 7: T_A for NMC9816AE = $-40°C$ to $+85°C$, $V_{CC} = 5V \pm 10\%$, T_A for NMC9816AM = $-55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$.

Switching Time Waveforms

Read



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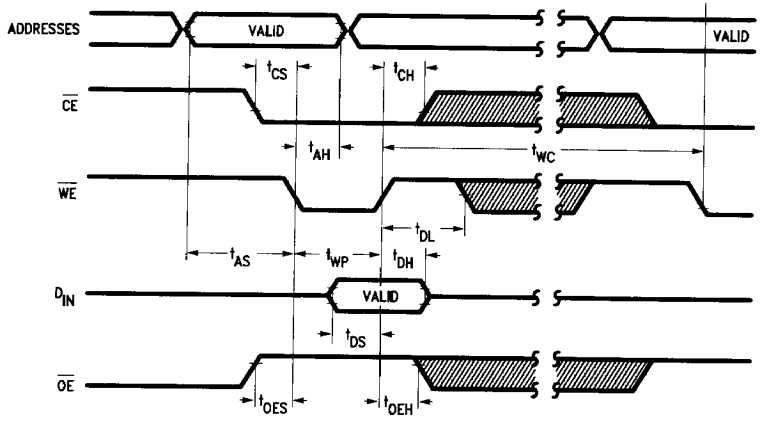
Write



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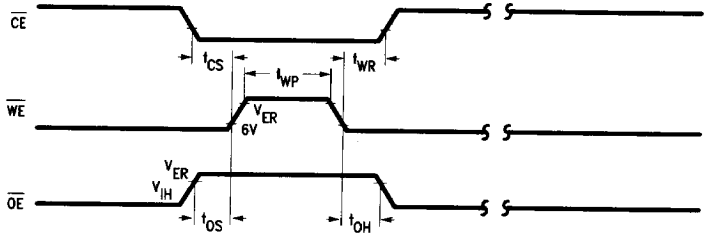
Chip Erase Cycle



DATA IN = DON'T CARE

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Device Operation

The NMC9816A has 6 modes of user operation which are detailed in Table I. All modes are designed to enhance the NMC9816A's functionality to the user and provide total microprocessor compatibility.

TABLE I. V_{CC} = 5V

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I_0/O_0-I_7/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	Hi-Z
Write	V_{IL}	V_{IH}	⊓	D_{IN}
Busy	V_{IH}	X	X	High-Z
	X	V_{IH}	X	High-Z
Data Polling	V_{IL}	V_{IL}	X	$I_7/O_7 = \overline{D_{IN}}$
Chip Erase	V_{IL}	V_{ER}	V_{ER}	X

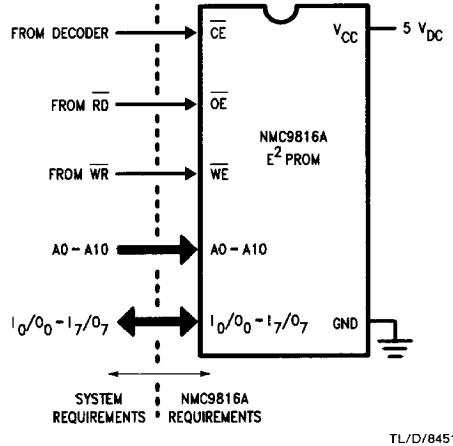

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FIGURE 3. Simple NMC9816A Interface Requirements

WRITE MODE

The NMC9816A is programmed electrically in-circuit, yet it provides the non-volatility usually obtained by optical erasure in EPROMS and by batteries with CMOS RAM. Writing to non-volatile memory has never been easier as no high voltage, external latching, erasing or timing is needed. When commanded to byte-write, the NMC9816A automatically latches the address, data, and control signals and starts the write cycle. During the write cycle V_{PP} is generated on-chip to perform an automatic byte-erase, then write.

DATA POLLING

The NMC9816A features $\overline{DATA}$ Polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_7. After completion of the write cycle, true data is available. $\overline{DATA}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DATA PROTECTION ON V_{CC} POWER UP AND POWER DOWN

An erase/write of a byte in the NMC9816A is accomplished with input signals $\overline{CE}$, $\overline{WE}$ = V_{IL}. During system (V_{CC}) power up and power down, this condition may be present as V_{CC} ramps up to or down from its steady state value of 5V. To prevent the possibility of an inadvertant byte write during this power transition period, an on-chip sensing circuit disables the internal programming circuit if V_{CC} falls below 4V (VLKO).

OPTIONAL HIGH VOLTAGE CHIP ERASE CYCLE

All data can be changed to "1" or erase state in one 10 ms cycle by raising $\overline{OE}$ to 12–22V and bringing $\overline{WE}$ to 12–22V for t_{WP} msec.

READ MODE

One aspect of the NMC9816A's high performance is its very fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMS and static RAMs. It offers a two line control architecture to eliminate bus contention. The NMC9816A can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

STANDBY MODE

The NMC9816A has a standby mode in which power consumption is reduced by 70%. This offers the user power supply cost benefits when designing a system with NMC9816A's. This mode occurs when the device is deselected ($\overline{CE}$ = V_{IH}). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

SYSTEM IMPLEMENTATION AND APPLICATION

The NMC9816A is compatible with industry standard microprocessors. It requires no interface circuitry and no support circuitry.

The NMC9816A is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a graphics terminal is an example where user defined functions, such as protocol, color, margins and character fonts can be keyed in by the user. Calibration constants could be stored by the NMC9816A in the smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics can be stored. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, could be stored in the NMC9816A. Accumulated totals for dollars, energy consumption, volume and even the logging of service done on computer boards or systems can be stored in the NMC9816A.

The NMC9816A is cost effective for lower density E^2PROM applications and can therefore be used to provide a lower system cost to the user compared to the 2816 or 2817. The user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and quality assurance. The designer will find the NMC9816A reduces design time by a sizable factor over the 2816 or 2817 due to the integration of timing, logic, latching and 5V-only operation.

Device Operation (Continued)

The NMC9816A will also open up new applications in environments where flexible parameter/data storage could not be implemented before. For example, applications with board space constraints are ideal for the NMC9816A. Several NMC9816A's can reside in the same space as one (1) 2816 with its support circuits. This is due to the reduction of all components required including the V_{PP} generator.

WRITE TIME CHARACTERISTICS

The NMC9816A's internal write cycle contains an automatic erase feature. The 2816 does not have this capability and must be given an external erase cycle prior to a write. The 2816 has a write time specification of 9 ms. Typically, these devices will write in times less than 9 ms, but the worst-case bit defines the minimum specification.

The NMC9816A's internal cycle consists of an automatic 2 ms (typical) erase followed by a 2 ms (typical) write. The total cycle is then typically 4 ms. The NMC9816A maximum specification is 10 ms.

WRITE PROTECTION

There are three features that protect the nonvolatile data from an inadvertant write.

- Noise Protection — A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense — When V_{CC} is below approximately 4V all 5V-only write functions are inhibited.
- Write Inhibit — Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power-on and power-off (V_{CC}).