

## Selectable Dual 3V/3.3V/5V 8-Bit DACs

### GENERAL DESCRIPTION

The ML2330 Selectable Dual 3V/3.3V/5V 8-bit DACs are dual voltage output digital-to-analog converters which can be independently programmed, or powered down to conserve power. The devices are intended for use in portable or low power 3V systems where space is critical.

Programming access to the DACs is provided over a high speed (10Mb/s), 3-wire serial interface which is compatible to the SPI™ and Microwire™ data formats. In addition to independent programming of the DAC output voltages, each device may be powered down, independent of the other DAC, to conserve power. Each DAC draws 2mA maximum quiescent current when operating, and typically less than 1µA when powered down.

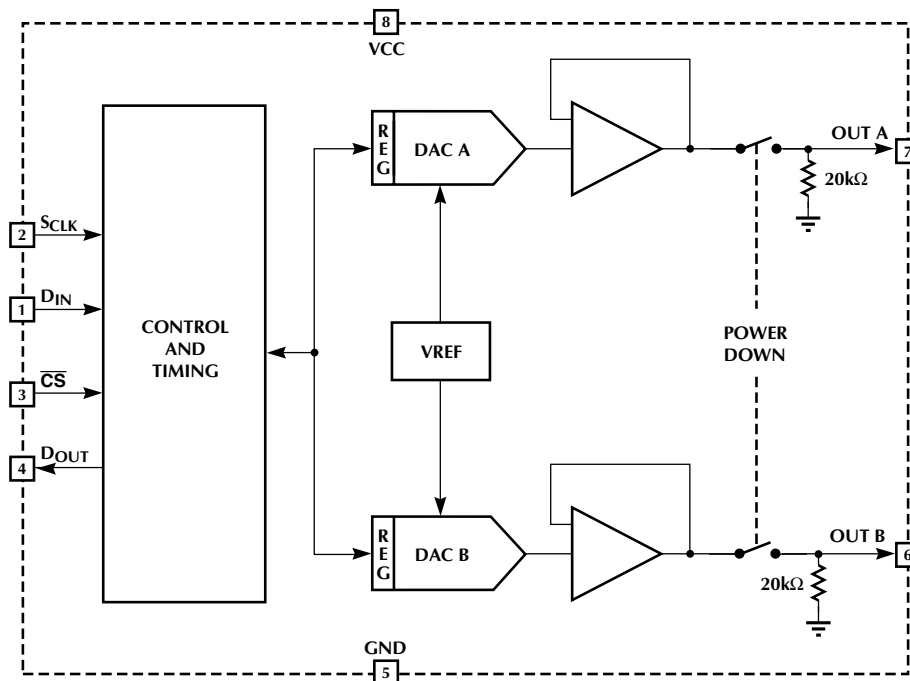
The device comes in an 8-pin SOIC package and in a special Extended Commercial temperature range (-20°C to 70°C) or Industrial temperature range (-40°C to 85°C).

### FEATURES

- 3V ±10%, 3.3 ±10% or 5V ±10% operation
- Low supply current (3.5mA max)
- Individual and full power down (down to 1µA)
- 10Mb/s three-wire serial interface, compatible to SPI and Microwire
- 8-pin SOIC package
- Available in Extended Commercial temperature range (-20°C to 70°C) and Industrial temperature range (-40°C to 85°C)
- Guaranteed monotonicity

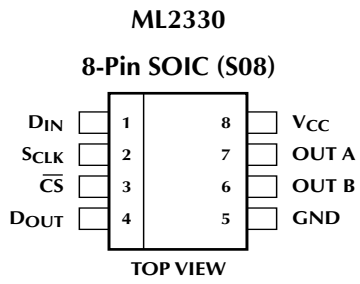
*\*Some Packages Are End Of Life Or Obsolete*

### BLOCK DIAGRAM



# ML2330

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN	NAME	FUNCTION
1	D <sub>IN</sub>	Data In
2	S <sub>CLK</sub>	Serial Clock
3	$\overline{\text{CS}}$	Chip Select
4	D <sub>OUT</sub>	Data Out
5	GND	Ground
6	OUT B	Output of DAC B
7	OUT A	Output of DAC A
8	V <sub>CC</sub>	Positive Supply

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage ( $V_{CC}$ )	6.0V
GND	-0.3V to $V_{CC} + 0.3V$
Logic Inputs	-0.3V to $V_{CC} + 0.3V$
Input Current per Pin	$\pm 25mA$
Storage Temperature	-65°C to 150°C
Package Dissipation at $T_A = 25^\circ C$	750mW
Lead Temperature (Soldering 10 sec.)	
SOIC	150°C

**OPERATING CONDITIONS**

Supply Voltage ( $V_{CC}$ )	
ML2330ES-2	3V $\pm$ 10%
ML2330ES-3	3.3V $\pm$ 10%
ML2330ES-5	5V $\pm$ 10%
Temperature Range	
ML2330ES	-20°C to 70°C
ML2330IS	-40°C to 85°C

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified,  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC}$  = Operating Supply Voltage Range,  $f_{CLK} = 10MHz$ ,  $R_L = 1k\Omega$ , ( $R_L = 2k\Omega$  for  $V_{CC} = 5V$ ),  $C_L = 100pF$  (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Converter</b>							
Resolution			8			bits	
Integral Linearity Error	ILE				$\pm 1.5$	LSB	
Differential Linearity Error	DLE				$\pm 1$	LSB	
Offset Error		$V_{CC} = 3.3V$ or $3.0V$	E Suffix	10	20	30	mV
			I Suffix	5	20	35	mV
		$V_{CC} = 5V$	E Suffix	15	25	35	mV
			I Suffix	10	25	40	mV
Gain Error					$\pm 5$	%FS	
<b>Analog Output</b>							
Output Drive Current	$I_{OUTPP}$	Full scale output			2	mA	
Power Supply Rejection Ratio	PSRR	@00 & FF		40		dB	
<b>Digital and DC</b>							
Logic Input Low	$V_{IL}$	$V_{CC} = 3V, 3.3V, \text{ or } 5V$			0.8	V	
Logic Input High	$V_{IH}$	$V_{CC} = 3V$ or $3.3V$	2.0			V	
		$V_{CC} = 5V$	2.8			V	
Logic Input Low Current	$I_{IL}$	$V_{IN} = GND$	-1			$\mu A$	
Logic Input High Current	$I_{IH}$	$V_{IN} = V_{CC}$			1	$\mu A$	
Logic Output Low	$V_{OL}$	$I = 3.2mA$			0.4	V	
Logic Output High	$V_{OH}$	$I = 0.4mA$	2.4			V	
Supply Current	$I_{CC}$	$R_L = \infty$		2.5	3.5	mA	
Power Down Current		All digital inputs at static 0V or $V_{CC}$	$V_{CC} = 3V$		3	$\mu A$	
			$V_{CC} = 5V$		5	$\mu A$	
<b>AC Performance</b>							
Settling Time	$t_S$	$\pm 1/2$ LSB		5	10	$\mu s$	
Slew Rate				1.4		V/ $\mu s$	
Crosstalk			60			dB	

**Note 1:** Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.

# ML2330

## TIMING CHARACTERISTICS (Serial Interface)

$V_{CC}$  = Operating Supply Voltage Range,  $C_L = 50\text{pF}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Converter</b>						
$\overline{CS}$ Fall to $S_{CLK}$ Setup Time	$t_{CSS}$		20			ns
$S_{CLK}$ Rise to $\overline{CS}$ Rise Hold Time	$t_{CSH}$		50			ns
$D_{IN}$ to $S_{CLK}$ Rise Setup Time	$t_{DS}$		20			ns
$D_{IN}$ to $S_{CLK}$ Rise Hold Time	$t_{DH}$		20			ns
$S_{CLK}$ Frequency	$f_{CLK}$			10		MHz
$S_{CLK}$ Duty Cycle			40		60	%
$S_{CLK}$ to $D_{OUT}$ Valid	$t_{DO}$	$V_{CC} = 3.3\text{V}$ or $5\text{V}$		30	60	ns
		$V_{CC} = 3\text{V}$		45	90	ns

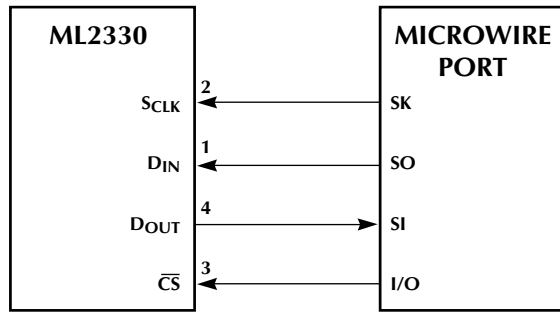


Figure 1a. Connections for Microwire.

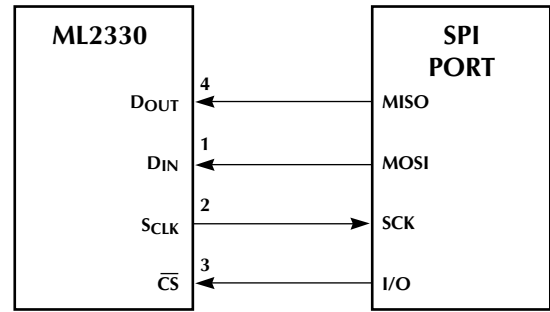
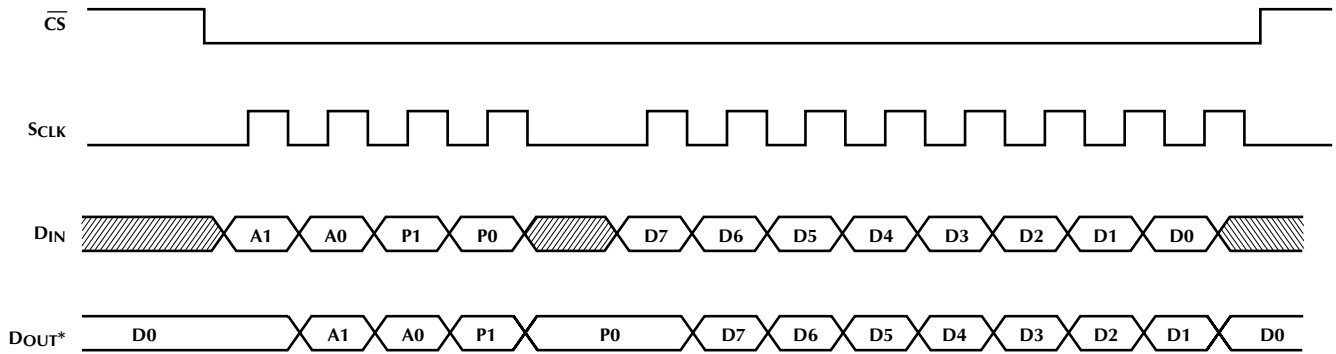


Figure 1b. Connections for SPI.



\*DOUT is the data from previous input.

Figure 1c. Interface Timing

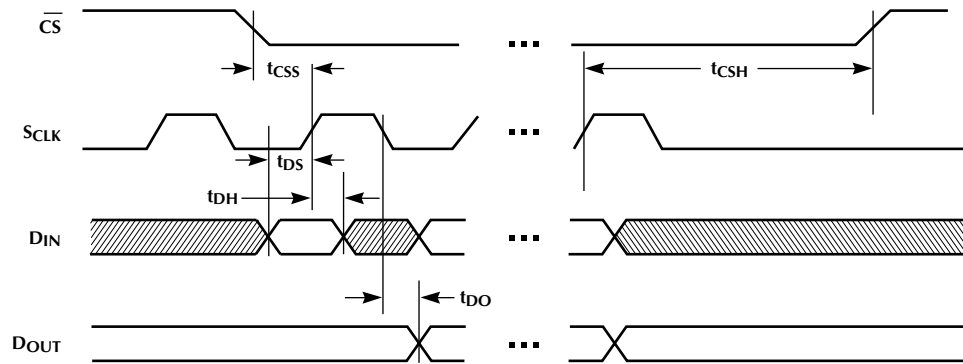


Figure 2. Detail Interface Timing

## FUNCTIONAL DESCRIPTION

### SERIAL INTERFACE

The ML2330 communicates with microprocessors through a synchronous, full-duplex, 3-wire interface (figure 1A & B). At power on, the control registers are cleared and both DACs have high impedance outputs. Data timing shown in Figure 1C is sent MSB-first and can be transmitted in one 4-bit and one 8-bit packet or in one 12-bit word. If a 16-bit control word is used, the first four bits are ignored. The serial clock ( $S_{CLK}$ ) synchronizes the data transfer. Data is transmitted and received simultaneously. Figure 2 shows detailed serial interface timing. Note that the clock should be low between updates.  $D_{OUT}$  does not go into a high impedance state if the clock idles or  $\overline{CS}$  is high.

Serial data is clocked into the data registers in MSB-first format, with the address and configuration information preceding the actual DAC data. Data is sampled on the  $S_{CLK}$ 's rising edge while  $\overline{CS}$  is low. Data at  $D_{OUT}$  is clocked out 12.5 clock cycles later, on the  $S_{CLK}$ 's falling edge.

Chip Select ( $\overline{CS}$ ) must be low to enable the read or write operation. If  $\overline{CS}$  is high, the interface is disabled and  $D_{OUT}$  remains unchanged.  $\overline{CS}$  must go low at least 10ns before the first clock pulse to properly clock in the first bit. With  $\overline{CS}$  low, data is clocked into the ML2330's internal shift register on the rising edge of the external serial clock.  $S_{CLK}$  can be driven at rates up to 10MHz.

### SERIAL INPUT DATA FORMAT AND CONFIGURATION CODES

The 12-bit serial input format shown in Figure 3 comprises two DAC address bits (A1, A0), two power down control bits (P1, P0) and eight bits of data (D7 . . . D0).

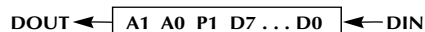


Figure 3. Serial Input Format

The 4-bit address/control code configures the DAC as shown in Table 1.

A1	A0	Function
0	0	No operation
0	1	Select control bits and DAC A
1	0	Select control bits and DAC B
1	1	Select control bits and both DACs

Table 1.1 Address Selection

P1	P0	Function
0	0	Normal
0	1	Power down DAC A
1	0	Power down DAC B
1	1	Power down entire chip

Table 1.2 Power Down Selection

### DAC OPERATION

The DACs are implemented using an array of equal current sources that are decoded linearly for the four most significant bits to improve differential linearity and to reduce output glitch around major carries. A voltage difference between on-board bandgap reference voltage and GND is converted to a reference current using an internal resistor to set up the appropriate current level in the DACs. The DACs output current is then converted to a voltage output by an output buffer and a resistive network. The matching among the on-chip resistors preserves the gain accuracy between these conversions.

# ML2330

## VOLTAGE REFERENCE

A bandgap voltage reference is incorporated on the ML2330. It is trimmed for zero temperature coefficient at 25°C to minimize output voltage drift over the specified operating temperature range.

## OUTPUT BUFFER AND GAIN SETTING

The output buffer converts the DAC output current to a voltage output using a resistive network. The outputs can swing from GND +0.02V to either 2.02V (3V) or 4.02V (5V). The DAC transfer function is:

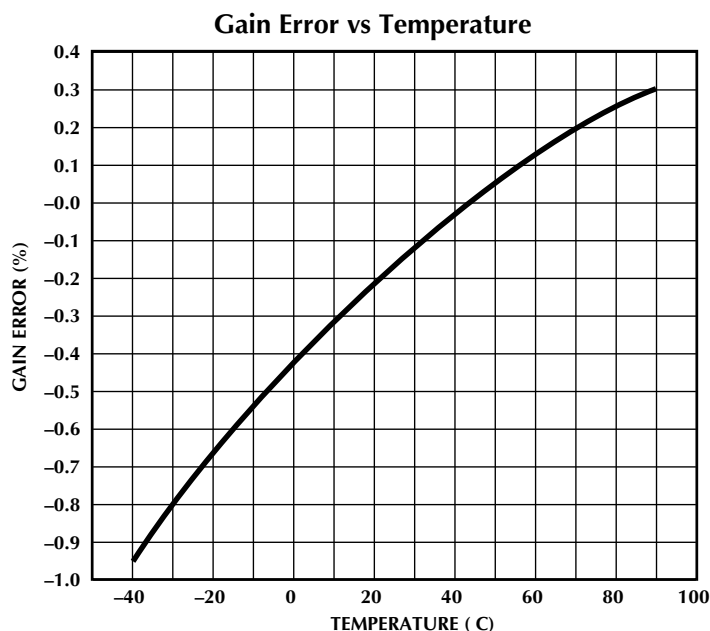
$$V_{OUT} = \frac{K \times DATA}{256} + 0.02$$

where  $K = 2$  if  $V_{CC} = 3V$  and  $K = 4$  if  $V_{CC} = 5V$

In the 3V operation, the amplifier outputs will settle to 1/2LSB in 10 $\mu$ s when loads are greater than 1k $\Omega$  (2k $\Omega$  for 5V operation) and capacitive loads smaller than 100pF.

## GAIN ERROR

The graph below shows how gain error varies with temperature when  $V_{CC} = 3.3V$ .

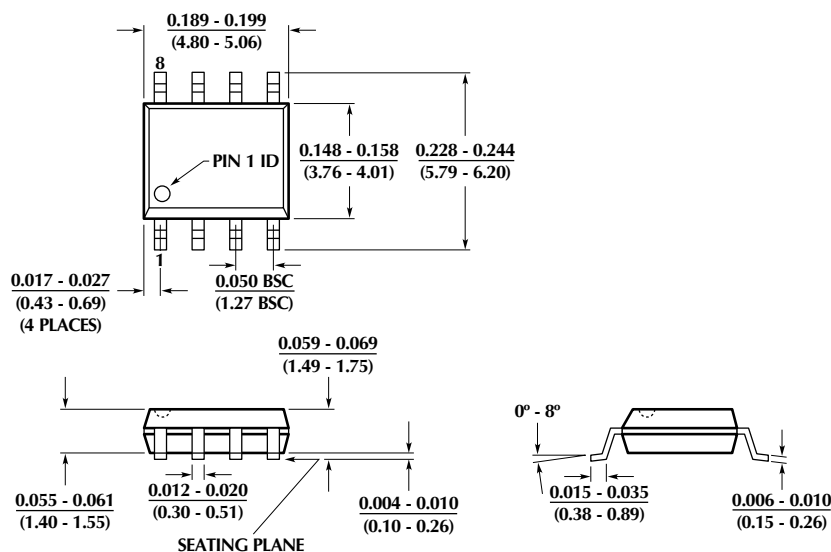


## POWER DOWN MODE

There are three power-down modes in the ML2330. By clearing the control bits P1-P0 (Table 3.2), the entire chip will be powered down with a supply current less than 5 $\mu$ A. Individual DACs can also be powered down to save power (1.75mA per DAC).

## PHYSICAL DIMENSIONS inches (millimeters)

Package: S08  
8-Pin SOIC



## ORDERING INFORMATION

PART NUMBER	V <sub>CC</sub>	TEMPERATURE RANGE	PACKAGE
ML2330ES-2	3V	-20°C to 70°C	8-Pin SOIC (S08)
ML2330ES-3 (End Of Life)	3.3V	-20°C to 70°C	8-Pin SOIC (S08)
ML2330ES-5 (End Of Life)	5V	-20°C to 70°C	8-Pin SOIC (S08)
ML2330IS-2	3V	-40°C to 85°C	8-Pin SOIC (S08)
ML2330IS-3 (Obsolete)	3.3V	-40°C to 85°C	8-Pin SOIC (S08)
ML2330IS-5	5V	-40°C to 85°C	8-Pin SOIC (S08)

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