Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

PRELIMINARY
IDT 61298S
IDT 61298L

T-46-23-10

4

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  - Military: 25/35/45/55/70ns (max.)
  - Commercial: 20/25/35/45/55ns (max.)
- Low power consumption
  - IDT61298S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - IDT61298L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery back-up operation—2V data retention (L version only)
- JEDEC standard pinout
- 28-pin DIP
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61298 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

The IDT61298 features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298's overall flexibility in high-speed memory applications.

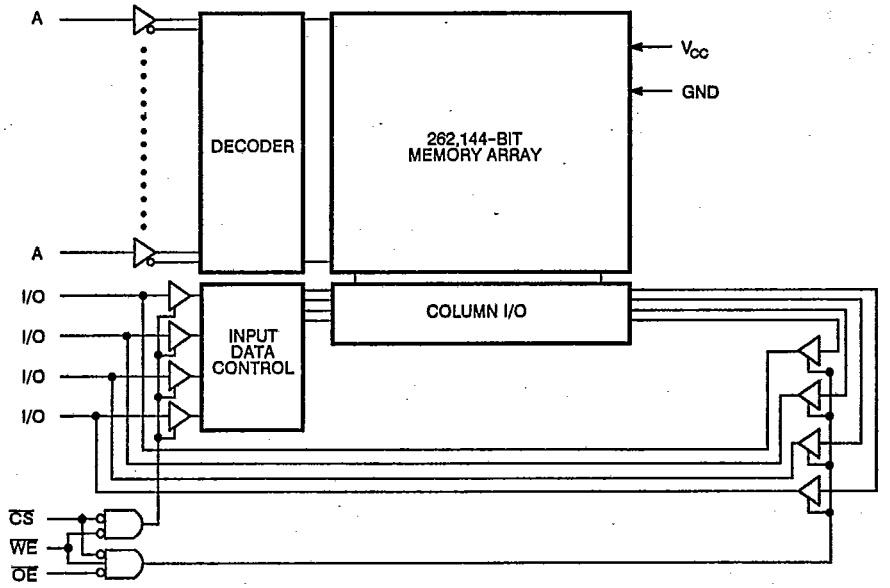
Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT61298 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous circuitry, along with matching access and cycle times, favor the simplified system design approach.

The IDT61298 is packaged in a 28-pin sidebraze or plastic 300mil DIP plus an SOIC, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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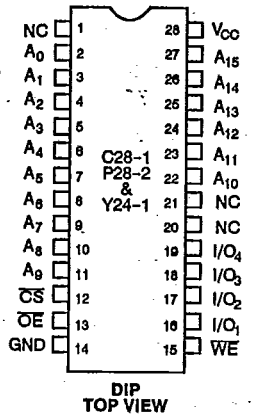
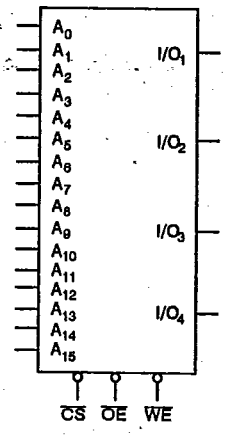
PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0–A_{15}	Address Inputs	I/O_{1-4}	Data Input/Output
$\overline{CS}$	Chip Select	V_{CC}	Power
$\overline{WE}$	Write Enable	GND	Ground
$\overline{OE}$	Output Enable		

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT61298S MIN.	IDT61298S TYP.(1)	IDT61298S MAX.	IDT61298L MIN.	IDT61298L TYP.(1)	IDT61298L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

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DC ELECTRICAL CHARACTERISTICS (1) V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	POWER	FUNCTION	61298S20 61298L20		61298S25 (2) 61298L25 (2)		61298S35 61298L35		61298S45 61298L45		61298S55 61298L55		61298S70 61298L70		UNIT
				COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	COM'L.	MIL.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0 (3)	S	READ	70	–	60	70	50	60	50	60	50	60	–	60	mA
			WRITE (4)	120	–	110	120	100	110	100	110	100	110	–	110	
		L	READ	50	–	40	50	30	40	30	40	30	40	–	40	
			WRITE (4)	110	–	100	110	90	100	90	100	90	100	–	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (3)	S	READ	170	–	160	170	150	160	150	160	150	160	–	160	mA
			WRITE (4)	170	–	160	170	150	160	150	160	150	160	–	160	
		L	READ	150	–	140	150	130	140	130	140	130	140	–	140	
			WRITE (4)	150	–	140	150	130	140	130	140	130	140	–	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH} V_{CC} = Max., f = f_{MAX} (3) Outputs Open.	S		35	–	35	35	35	35	35	35	35	35	–	35	mA
		L		20	–	20	20	20	20	20	20	20	20	–	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC} V_{CC} = Max., f = 0 (3)	S		30	–	30	35	30	35	30	35	30	35	–	35	mA
		L		1.5	–	1.5	4.5	1.5	4.5	1.5	4.5	1.5	4.5	–	4.5	

NOTES:

1. All values are maximum guaranteed values.
2. Preliminary data for military devices only.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Write cycle current specifications are included to aid in the design of extremely sensitive applications. It should be noted that in most systems the ratio of read cycles to write cycles is extremely high. When calculating total current consumption, the designer should weight these figures by the percentage of "On" time as well as the anticipated ratio of read to write cycles (usually greater than 90%).

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DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL.	–	50	75	2000	3000	µA
			COM'L.	–	50	75	500	750	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:
1. $T_A = +25°C$
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

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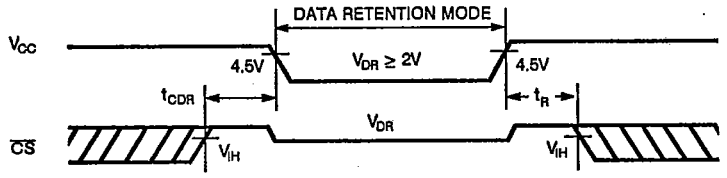
LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

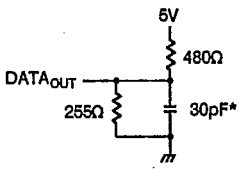


Figure 1. Output Load

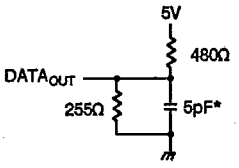


Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	61298S20[1] 61298L20[1] MIN.	MAX.	61298S25[4] 61298L25[4] MIN.	MAX.	61298S35 61298L35 MIN.	MAX.	61298S45 61298L45 MIN.	MAX.	61298S55 61298L55 MIN.	MAX.	61298S70[2] 61298L70[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	70	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	35	–	45	–	55	–	70	ns
t_{CLZ}[3]	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	12	–	15	–	25	–	30	–	35	–	45	ns
t_{OLZ}[3]	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}[3]	Chip Select to Output in High Z	–	10	–	13	–	15	–	20	–	25	–	30	ns
t_{OHZ}[3]	Output Disable to Output in High Z	–	10	–	13	–	15	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}[3]	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}[3]	Chip Deselect to Power Down Time	–	20	–	25	–	35	–	45	–	55	–	70	ns

NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for military devices only.

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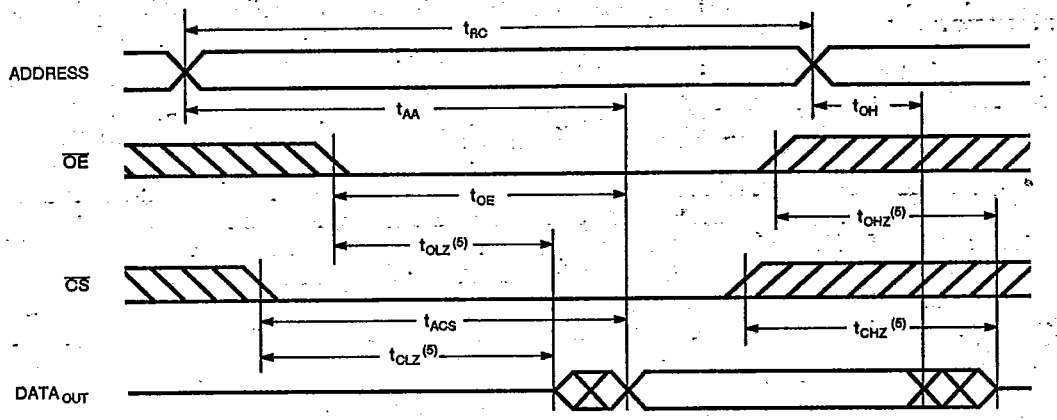
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



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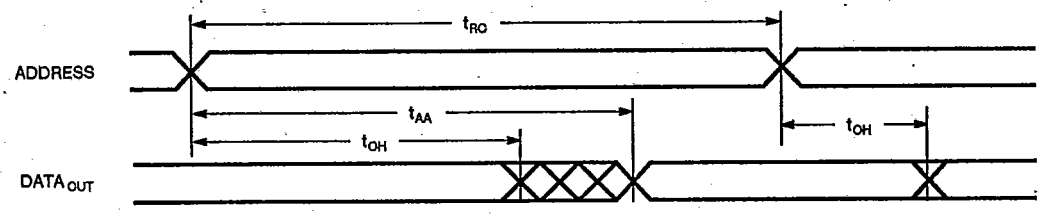
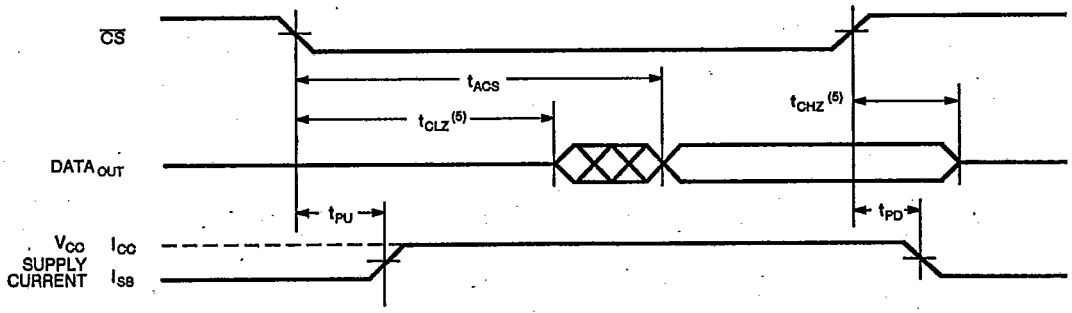
TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

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AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	61298S20[1] 61298L20[1] MIN.	MAX.	61298S25[4] 61298L25[4] MIN.	MAX.	61298S35 61298L35 MIN.	MAX.	61298S45 61298L45 MIN.	MAX.	61298S55 61298L55 MIN.	MAX.	61298S70[2] 61298L70[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{CW}	Chip Select to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AW}	Address Valid to End of Write	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	20	–	20	–	30	–	40	–	50	–	60	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}[3]	Write Enable to Output in High Z	–	13	–	13	–	15	–	20	–	25	–	30	ns
t_{DW}	Data Valid to End of Write	15	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}[3]	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for military devices only.

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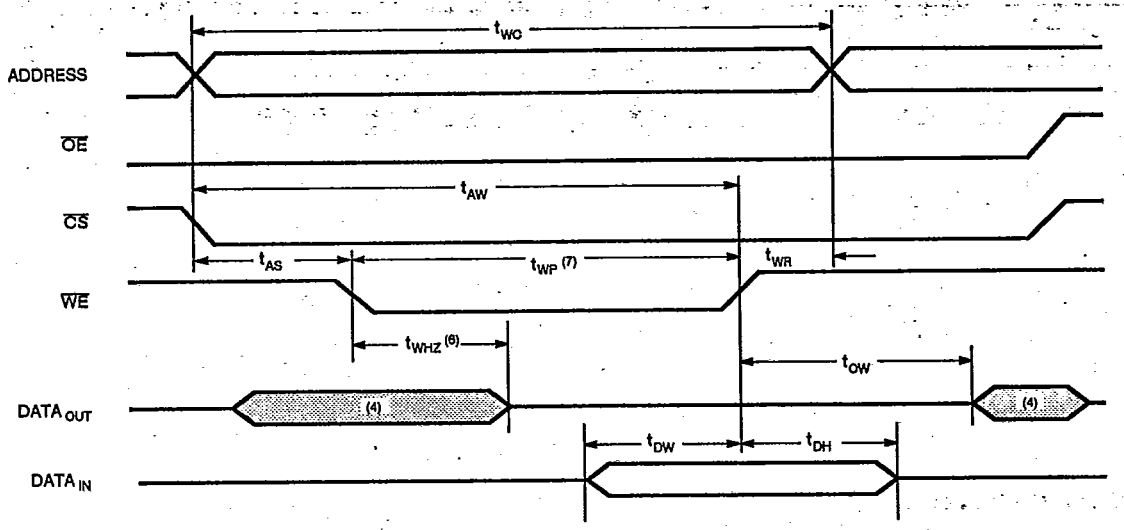
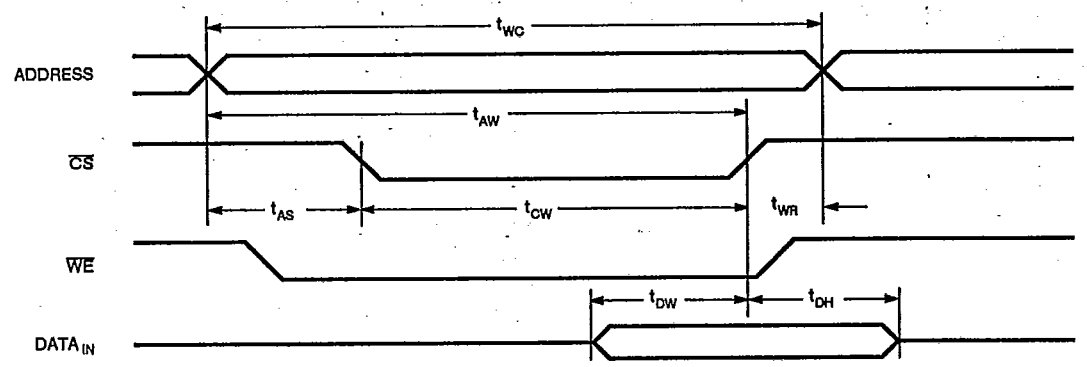
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING) (1, 2, 3, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING) (1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±200 mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	POWER
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

ORDERING INFORMATION