Integrated Circuit Systems, Inc.

ICS90C61A

Dual Video/Memory Clock Generator

Introduction

The Integrated Circuit Systems **ICS90C61A** is a dual clock generator for VGA applications. It simultaneously generates two clocks. One clock is for the video memory, and the other is the video dot clock.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, AC/DC characteristics, timing diagrams, and package mechanical information.

Description

The Integrated Circuit Systems Video Graphics Array Clock Generator (**ICS90C61A**) is capable of producing different output frequencies under firmware control. The video output frequency is derived from a 14.318 MHz system clock available in IBM PC/XT/AT and Personal System/2 computers. It is designed to work with Western Digital Imaging Video Graphics Array and 8514/A devices to optimize video subsystem performance.

The video dot clock output may be one of seven internally-generated frequencies or two external inputs. The selection of the video dot clock frequency is done through four inputs.

- SEL0
- SEL1
- VGATTL
- FCLKSEL

SEL0 and SEL1 are latched by the SELEN signal. VGATTL and FCLKSEL are used as direct inputs to the VCLK selection. Table 1-1 is the truth table for VCLK selection.

The input and truth table have been designed to allow a direct connection to one of the many Western Digital Imaging VGA controllers or 8514/A chip sets.

The MCLK output is one of four internally-generated frequencies as shown in Table 1-2. The various VCLK and MCLK frequencies are derived from the 14.318 MHz input frequency.

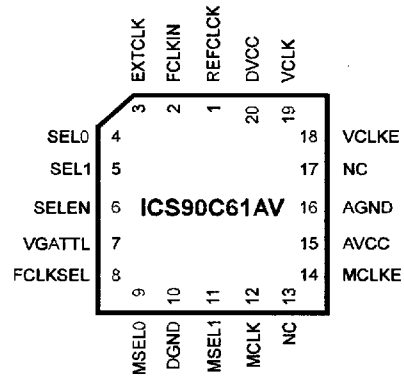
The VCLKE and MCLKE input can tristate the VCLK and MCLK outputs to facilitate board level testing.

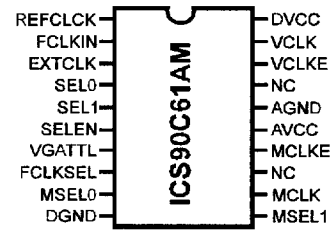
The **ICS90C61A** is capable of extended frequency output up to 80 MHz in custom applications. See page 5 for details.

Features

- Dual Clock generator for the IBM-compatible Western Digital Imaging Video Graphics Array (VGA) LSI devices, and 8514/A chip sets
- Integral loop filter components
- Generates seven video clock frequencies derived from a 14.318 MHz system clock reference frequency
- Video clock which is selectable among the seven internally generated clocks and two external clocks
- On-chip generation of four memory clock frequencies
- CMOS technology
- Available in 20-pin PLCC, SOIC, and DIP packages
- Extended frequency capabilities to 80 MHz in custom frequency patterns

Pin Configuration





Note: ICS90C61AN (DIP) pin-out is identical to ICS90C61AM (SOIC) pin-out.

ICS90C61A VGA Interface

The **ICS90C61A** has two system interfaces: System Bus and VGA Controller, and six user-programmable inputs. Figure 2-1 shows how the Integrated Circuit Systems VGA Clock **ICS90C61A** is connected to a VGA controller. Western Digital Imaging VGA controllers normally have a status bit that indicates to the VGA controller that it is working with a clock chip. When working with a clock chip the VGA controller changes two of its clock inputs, VCLK1 and VCLK2, to outputs. These outputs are used to select the required video frequency.

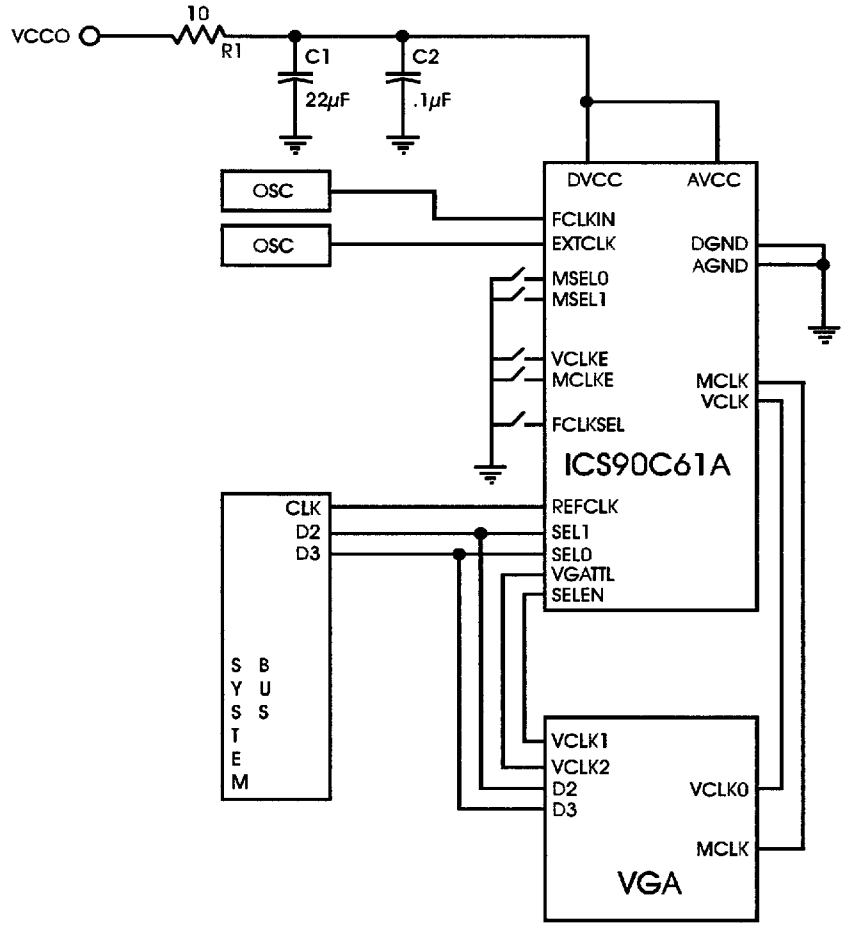


Figure 2-1 ICS90C61A Interface

Note:

C_2 should be placed as close as possible to the **ICS90C61A** AVCC pin.

System Bus Inputs

The system bus inputs are:

- REFCLK
- SEL0
- SEL1

The **ICS90C61A** uses the system bus 14.318 MHz clock as a reference to generate all its frequencies for both video and memory clocks. Data lines D2 and D3 are commonly used as inputs to VSEL0 and VSEL1 for video frequency selection.

Inputs from VGA Controller

The VGA controller input to the **ICS90C61A** is:

- SELEN

The **ICS90C61A** is programmed to generate different video clock frequencies using the inputs of SEL0, SEL1, VGATTL, and FCLKSEL. The signals VGATTL and FCLKSEL may be supplied by the VGA controller as is the case in Western Digital Imaging VGA controllers. The inputs SEL0-1 are latched with the signal SELEN. The SELEN input should be an active low pulse. This active low pulse is generated in Western Digital Imaging VGA controllers during I/O writes to internal register 3C2h.

Note: Only SEL0 and SEL1 are latched with signal SELEN.

Outputs to VGA Controller

The outputs from the **ICS90C61A** to the VGA controller are:

- MCLK
- VCLK

MCLK and VCLK are the two clock outputs to the VGA controller.

Analog Filters

The analog filters are integral to the **ICS90C61A** device. No external components are required. This feature reduces PC board space requirements and component costs. Phase jitter is reduced as externally-generated noise cannot easily influence the phase-locked loop filter.

User-Definable Inputs

The user-definable inputs are:

- EXTCLK
- FCLKIN
- VLCKE, MCLKE
- MSELO-1
- VGATTL, FCLKSEL

EXTCLK and FCLKIN are additional inputs that may be internally routed to the VCLK output. The additional inputs are useful for supporting modes that require frequencies not provided by the **ICS90C61A**.

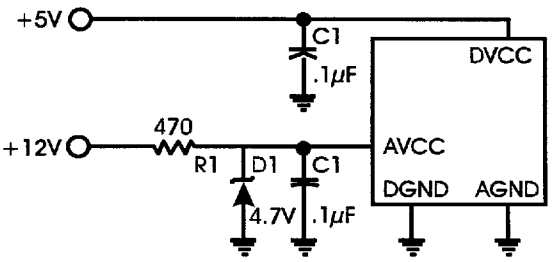
VCLKE and MCLKE are the output enable signals for VCLK and MCLK.When low, the respective output is tristated.

MSEL0-1 are the memory clock (MCLK) select lines. Table 1-2 shows how MCLK frequencies are selected. All signals in this group have internal pull-up resistors.

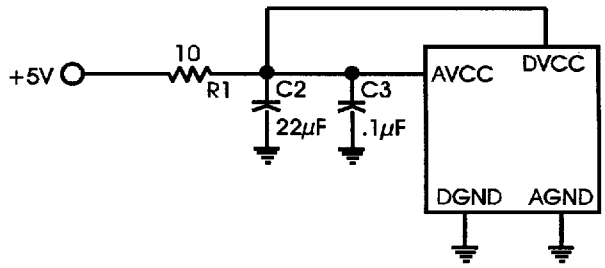
VGATTL and FCLKSEL are video clock (VCLK) select lines that can select additional VCLK frequencies. See Table 1-1.

Power Considerations

The **ICS90C61A** product requires an AV_{CC} supply free of fast rise time transients. This requirement may be met in several ways and is highly dependent on the characteristics of the host system. A VGA adapter card is unique in that it must function in an unknown environment. +5 volt power quality is dependent not only on the quality of the power supply resident in the host system, but also on the other cards plugged into the host's backplane. Power supply noise ranges from fair to terrible. As the VGA adapter manufacturer has no control over this, he must assume the worst. The best solution is to create a clean +5 volts by deriving it from the +12 volt supply by using a zener diode and dropping resister. A 470 Ohm resistor and 4.7 volt Zener diode are the least costly way to accomplish this. A .047 to .1 microfarad bypass capacitor tied from AV_{CC} to AGND insures good high-frequency decoupling of this point.



Laptop and notebook computers have entirely different problems with power. Typically they have no +12 volt supply; however, they are much quieter electrically. Because the designer has complete control of the system architecture, he can place sensitive components and systems such as the RAMDAC and Dual Video/Memory Clock away from DRAM and other noise-generating components. Most systems provide power that is clean enough to allow for jitter-free Dual Video/Memory Clock performance if the +5 volt supply is decoupled with a resistor and 22 microfarad Tantalum capacitor. Digital inputs that are desired to be held at static logical high level should not be tied to +5 volts as this will result in excessive current drain through the ESD protection diode. The internal pull-up resistors will adequately keep these inputs high.



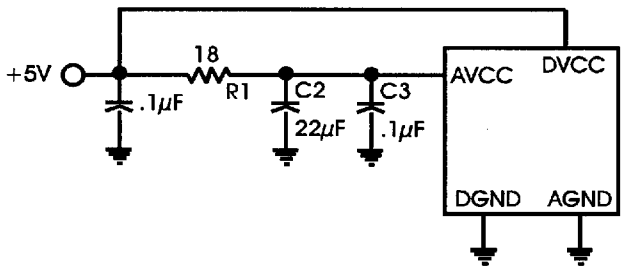


Table 1-1 VCLK SELECTION

FCLKSEL	VGATTL	SEL0	SEL1	VCLK FREQUENCY (MHz) ICS90C61A-PR2**
1	0	0	0	REFCLK
1	0	0	1	16.108
1	0	1	0	32.216
1	0	1	1	44.744
1	1	0	0	25.057
1	1	0	1	28.089
1	1	1	0	EXTCLK*
1	1	1	1	36.242
0	X	X	X	FCLKIN*

Table 1-2 MCLK SELECTION

MSEL1	MSEL0	MCLK FREQUENCIES (MHz) ICS90C61A-PR2**
0	0	41.612
0	1	37.585
1	0	36.242
1	1	44.744

*Note: FCLKIN and EXTCLK may be programmed to output custom frequencies up to 80 MHz in applications which require this capability. Custom frequencies in these addresses require a significant volume committment and/or one-time mask charge. Contact ICS Sales for details.

**Note: If no "dash number" is specified, then the "–PR2" will be supplied since this version is completely compatible with the original WD90C61 frequency set.

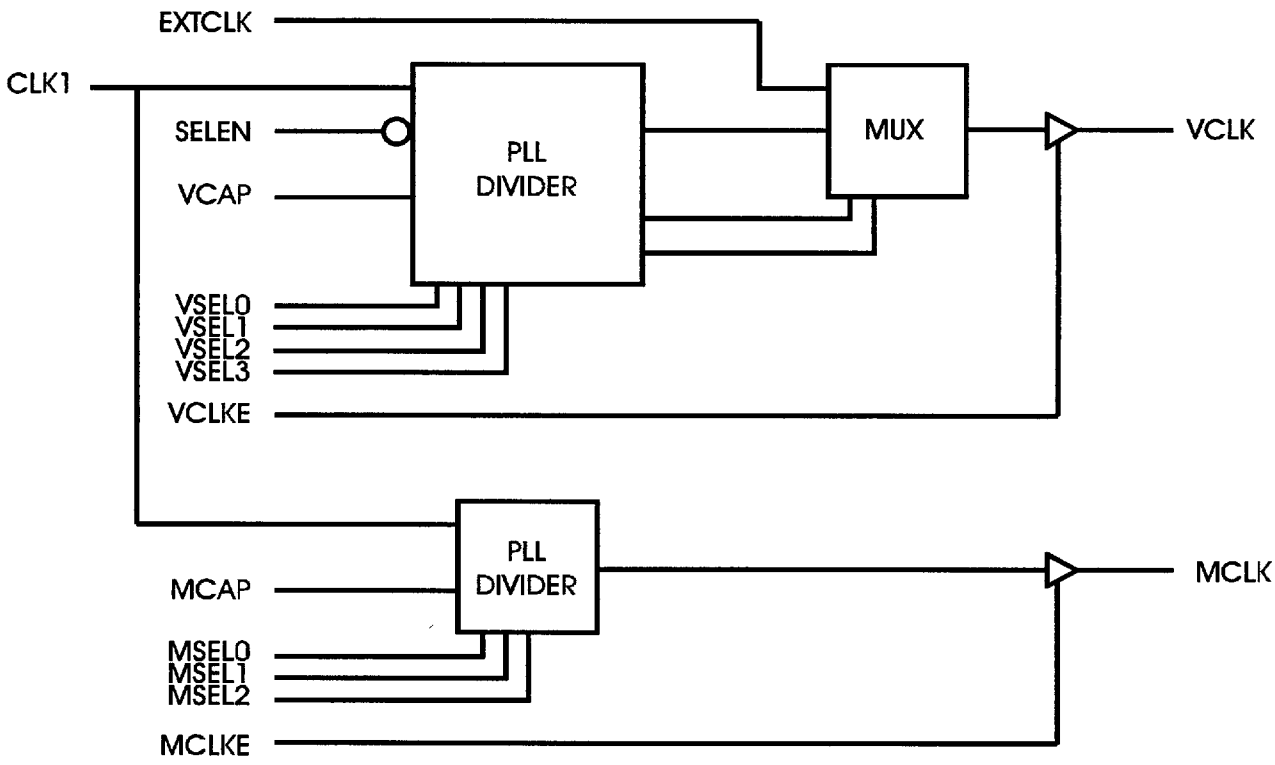


Figure 2-2 ICS90C61A Functional Block Diagram

Pin Descriptions

The following table provides the pin descriptions for the 20-pin **ICS90C61A** packages:

PIN NUMBER	PIN SYMBOL	TYPE	DESCRIPTION
1	REFCLK	IN	Reference input clock from system.
2	FCLKIN	IN	Feature clock input pin.
3	EXTCLK	IN	External clock input for an additional frequency.
4	SEL0	IN	Control input for VCLK selection.
5	SEL1	IN	Control input for VCLK selection.
6	SELEN	IN	Strobe for latching VSEL(0,1) *(low enable).*
7	VGATTL	IN	Control input for VCLK selection.
8	FCLKSEL	IN	Control input for FCLK selection.
9	MSEL0	IN	Select input for MCLK selection.
10	DGND	-	Ground for Digital Circuit.
11	MSEL1	IN	Select input for MCLK selection.
12	MCLK	OUT	Memory Clock Output.
13	NC	-	No Connection.
14	MCLKE	IN	Enable input for MCLK output *(high enables output).*
15	AVCC	-	Power supply for analog circuit.
16	AGND	-	Ground for analog circuit.
17	NC	-	No Connection.
18	VCLKE	IN	Enable input for VCLK output *(high enables output).*
19	VCLK	OUT	Video Clock Output.
20	DVCC	-	Power supply for Digital Circuit.

Note:

CLK1, EXTCLK, FCLKIN, SEL0, SEL1,VGATTL, FCLKSEL, SELEN, MSEL0, MSEL1, VCLKE, and MCLKE - input pins have internal pull-up resistors.

Absolute Maximum Ratings

Ambient temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to V_{SS}	0.5 to 7 volts

Note: Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (OV Ground). Positive current flows into the referenced pin.

Operating temperature range	0°C to 70°C
Power supply voltage	4.75 to 5.25 volts

DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS	PINS
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{CC} = 5V	SEL0-1, SELEN, VGATTL, MSEL0-1, FCLKSEL, VCLKE, MCLKE, EXTCLK
V_{IH}	Input High Voltage	2.0	V_{CC}	V	V_{CC} = 5V	SEL0-1, SELEN, VGATTL, MSEL0-1, FCLKSEL, VCLKE, MCLKE, EXTCLK
V_{IL}	Input Low Voltage	Vss	1.5	V	V_{CC} = 5V	FCLKIN
V_{IH}	Input High Voltage	V_{CC} -1.5	V_{CC}	V	V_{CC} = 5V	FCLKIN
I_{IH}	Input Leakage Current	-	20	µA	V_{in} = V_{CC}	
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 6.0 mA	
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 4.0 mA	
I_{CCD}	Digital Supply Current	-	35	mA	V_{CC} = 5V, C_L = 15pF	
I_{CCA}	Analog Supply Current	-	10	mA	V_{CC} = 5V	
R_{UP}	Internal Pull-up Resistors	25	-	K ohms	V_{CC} = 5V	
C_{in}	Input Pin Capacitance	-	8	pF	F_C = 1 MHz	
C_{out}	Output Pin Capacitance	-	12	pF	F_C = 1 MHz	

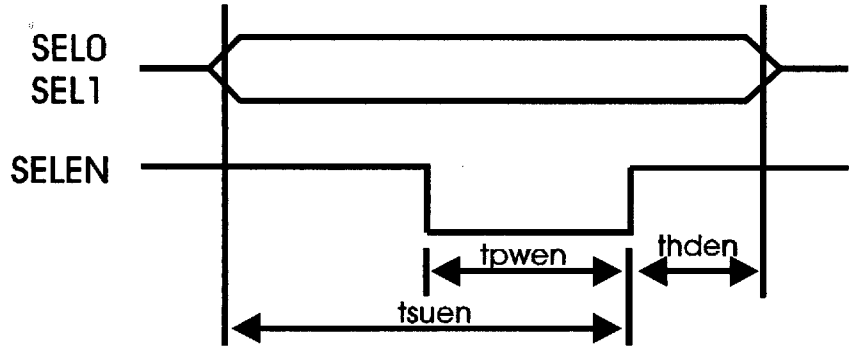
AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.

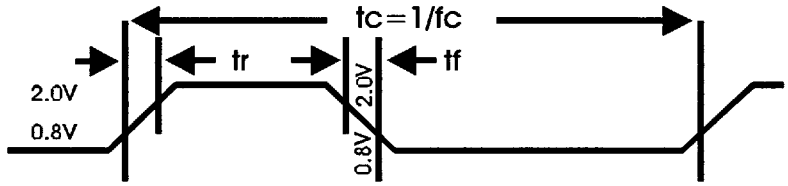
1. REFCLK = 14.318 MHz
2. $T_C = 1/F_C$
3. All units are in nanoseconds (ns).
4. Maximum jitter is within a range of 30 μ s after triggering on a 400 MHz scope.
5. Rise and fall time between 0.8 and 2.0 VDC.
6. Output pin loading = 15pF
7. Duty cycle is measured at 1.4V

SYMBOL	PARAMETER	MIN	MAX	NOTES
	SELEN TIMING			
T_{pwen}	Enable Pulse Width	20	-	
T_{suen}	Setup Time Data to Enable	20	-	
T_{hden}	Hold Time Data to Enable	10	-	
	REFERENCE INPUT CLOCK			
Tr	Rise Time	-	10	Phase-Jitter 1 ns max.
Tf	Fall Time	-	10	Duty Cycle 42.5% min. to 57.5% max.
MCLK and VCLK TIMINGS				
Tr	Rise Time	-	3	Phase-Jitter 3 ns max.
Tf	Fall Time	-	3	Duty Cycle 40%min. to 60% max.
-	Frequency Error		1.0	%
-	Maximum Frequency		80	MHz
-	Propagation Delay for Pass Through Frequency	-	20	ns
-	Output Enable to Tristate (into and out of) time		15	ns

ENABLE TIMING



CLOCK WAVEFORM



ICS90C61A Standard Patterns

FCLKSEL	VGATTL	SEL0	SEL1	VCLK FREQUENCY (MHz) ICS90C61A-PR2**
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MSEL1	MSEL0	MCLK FREQUENCIES (MHz) ICS90C61A-PR2**
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0	1	37.585
1	0	36.242
1	1	44.744

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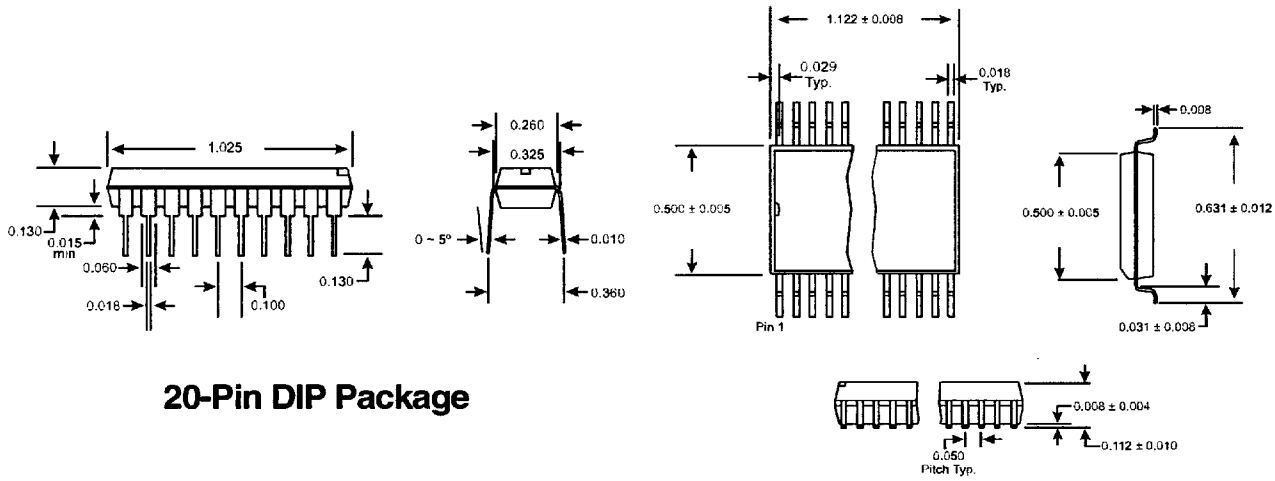
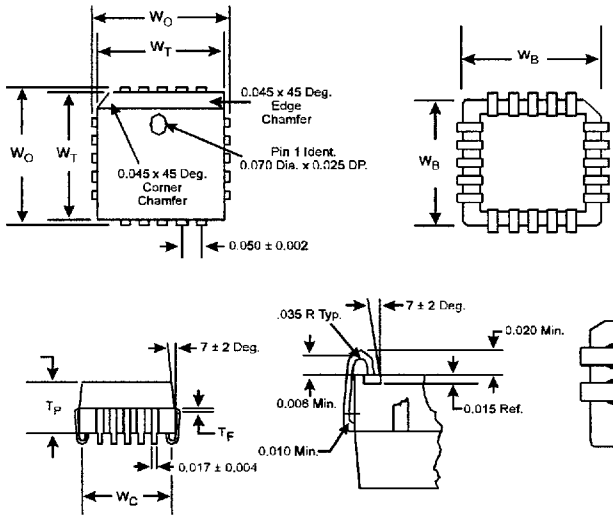


20-Pin DIP Package



LEAD COUNT	20L
DIMENSION L	0.504

20-Pin SOIC Package

PLCC Package

Ordering Information

ICS90C61AN or ICS90C61AM or ICS90C61AV

Example:

ICS XXXX-XXX N

Package Type
N=DIP (Plastic) V=PLCC
M=SOIC

Pattern Number (2 or 3 digit number for parts with ROM code patterns)
Note: Unless a specific pattern is ordered, PR2 will be shipped.

Device Type (consists of 3-6 digit numbers)

Prefix
ICS, AV=Standard Device; GSP=Genlock Device