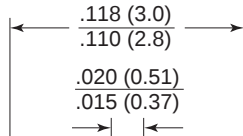




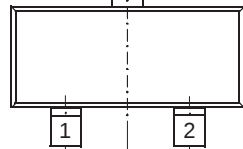
P-Channel Enhancement-Mode MOSFET

Low $V_{GS(th)}$ $V_{DS}=20V$ $R_{DS(on)} 0.13\Omega$ $I_D -2.3A$

TO-236AB (SOT-23)



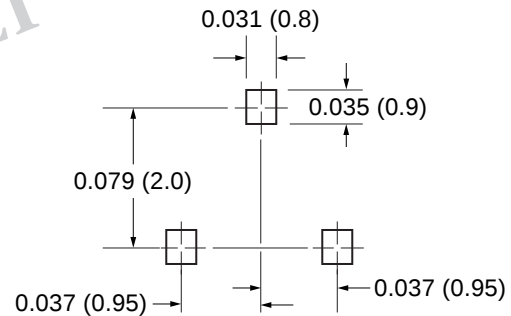
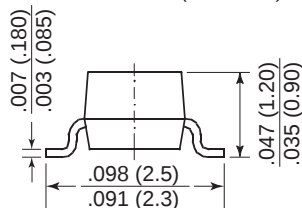
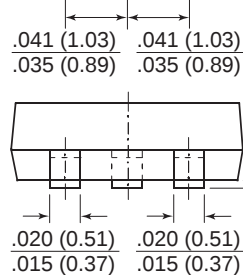
Top View



Pin Configuration

1. Gate
2. Source
3. Drain

Dimensions in inches and (millimeters)



Mounting Pad Layout

Mechanical Data

Case: SOT-23 Plastic Package

Weight: approx. 0.008g

Marking Code: 01

Features

- Advanced Trench Process Technology
- High density cell design for ultra-low on-resistance
- Popular SOT-23 package with copper lead frame for superior thermal and electrical capabilities
- Compact and low profile
- -2.5V rated

Maximum Ratings and Thermal Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source-Voltage	V_{GS}	± 8	V
Continuous Drain Current $T_J = 150^\circ C$	I_D	-2.3 -1.5	A
Pulsed Drain Current ⁽¹⁾	I_{DM}	-10	A
Maximum Power Dissipation ⁽²⁾	P_D	1.25 0.8	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ C$
Maximum Junction-to-Ambient Thermal Resistance ⁽²⁾	$R_{\theta JA}$	100	$^\circ C/W$

Note:

(1) Pulse width limited by maximum junction temperature.

(2) Surface mounted on FR4 board, $t \leq 5$ sec.

P-Channel Enhancement-Mode MOSFET

Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = -250μA	-20	—	—	V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.45	—	—	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±8V	—	—	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V	—	—	-1.0	μA
		V _{DS} = -16V, V _{GS} = 0V, T _J = 55°C	—	—	-10	
On-State Drain Current ⁽¹⁾	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} = -4.5V	-6	—	—	A
		V _{DS} ≤ -5V, V _{GS} = -2.5V	-3	—	—	
Drain-Source On-State Resistance ⁽¹⁾	R _{DS(on)}	V _{GS} = -4.5V, I _D = -2.8A	—	95	130	mΩ
		V _{GS} = -2.5V, I _D = -2.0A	—	122	190	
Forward Transconductance ⁽¹⁾	g _{fs}	V _{DS} = -5V, I _D = -2.8A	—	6.5	—	S

Dynamic

Total Gate Charge	Q _g	V _{DS} = -6V, V _{GS} = -4.5V I _D = -2.8A	—	5.4	10	nC
Gate-Source Charge	Q _{gs}		—	0.8	—	
Gate-Drain Charge	Q _{gd}		—	1.1	—	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -6V, R _L = 6Ω I _D ≈ -1A, V _{GEN} = -4.5V R _G = 6Ω	—	5	25	ns
Rise Time	t _r		—	19	60	
Turn-Off Delay Time	t _{d(off)}		—	95	110	
Fall Time	t _f		—	65	80	
Input Capacitance	C _{iss}	V _{DS} = -6V, V _{GS} = 0V f = 1.0MHz	—	447	—	pF
Output Capacitance	C _{oss}		—	124	—	
Reverse Transfer Capacitance	C _{rss}		—	80	—	

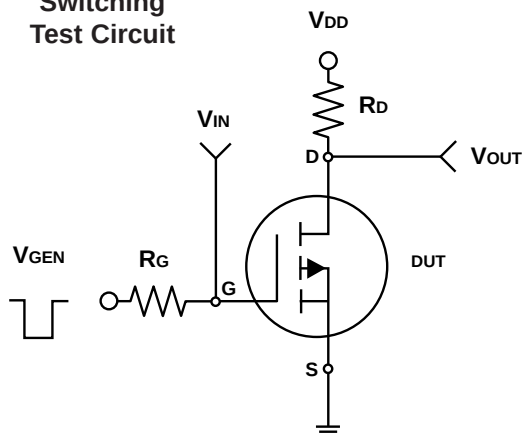
Source-Drain Diode

Maximum Diode Forward Current	I _S	—	—	—	-1.6	A
Diode Forward Voltage	V _{SD}	I _S = -1.6A, V _{GS} = 0V	—	-0.8	-1.2	V

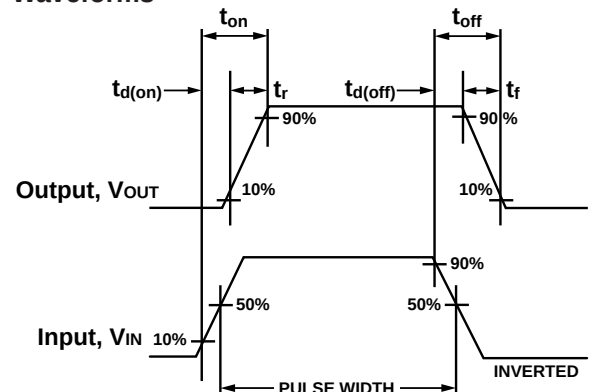
Note:

(1) Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%

Switching Test Circuit



Switching Waveforms



P-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 1 – Output Characteristics

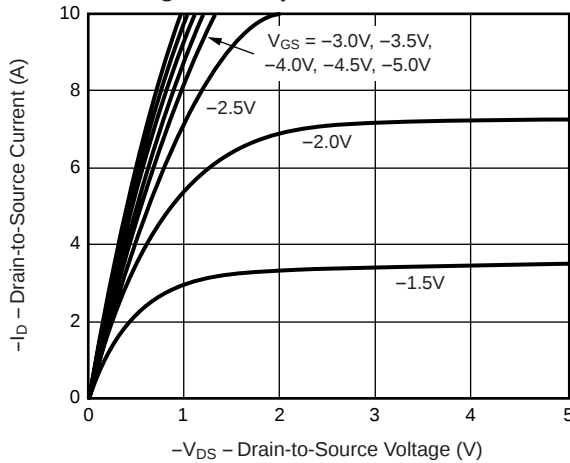
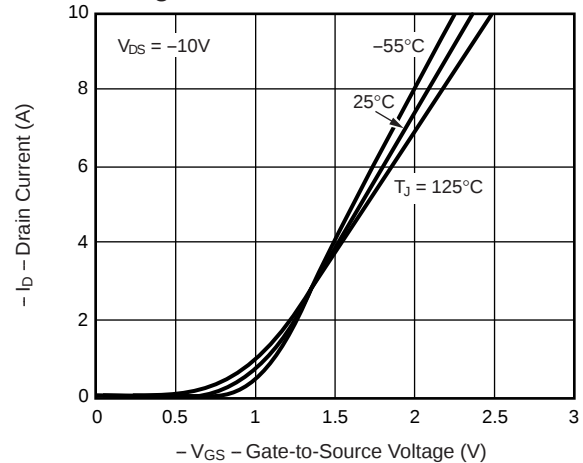
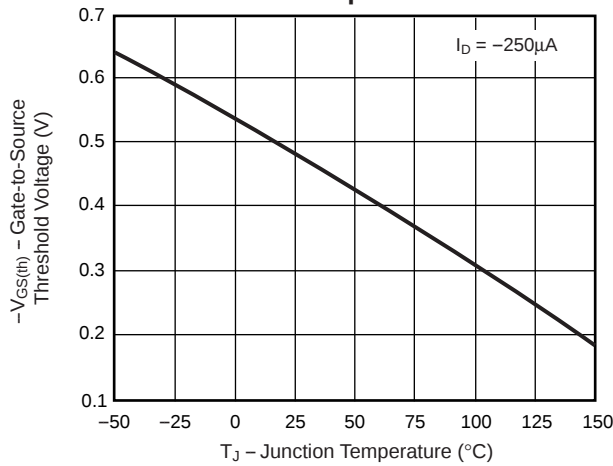


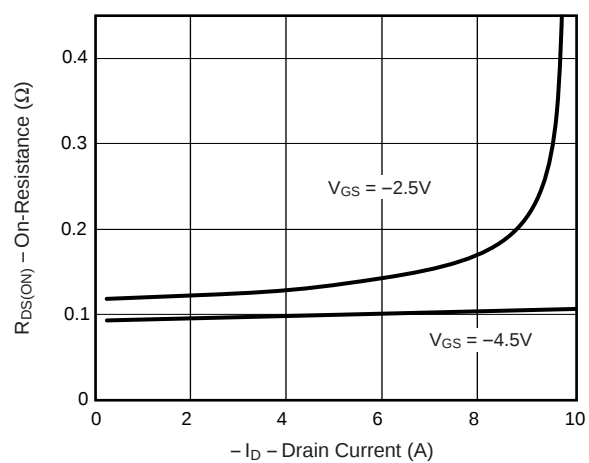
Fig. 2 – Transfer Characteristics



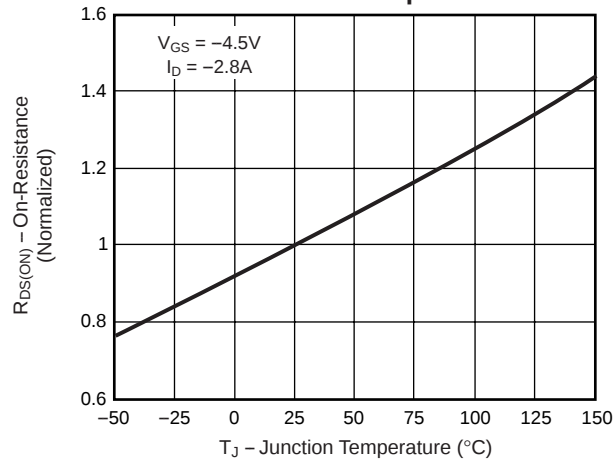
**Fig. 3 – Threshold Voltage
vs. Temperature**



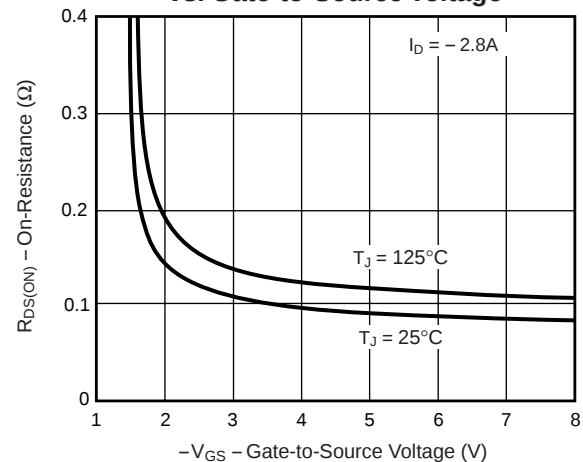
**Fig. 4 – On-Resistance
vs. Drain Current**



**Fig. 5 – On-Resistance
vs. Junction Temperature**



**Fig. 6 – On-Resistance
vs. Gate-to-Source Voltage**



P-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Fig. 7 – Gate Charge

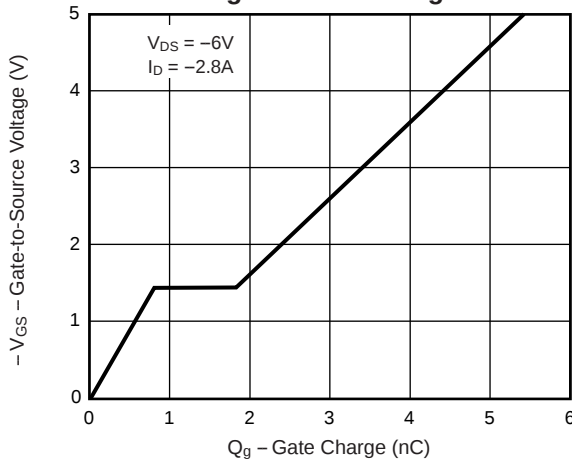


Fig. 8 – Capacitance

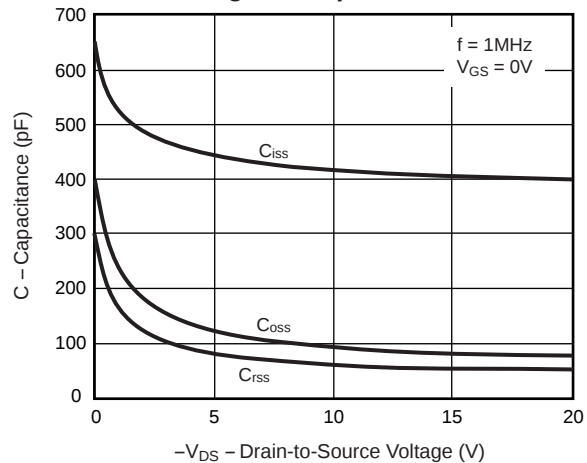


Fig. 9 – Source-Drain Diode
Forward Voltage

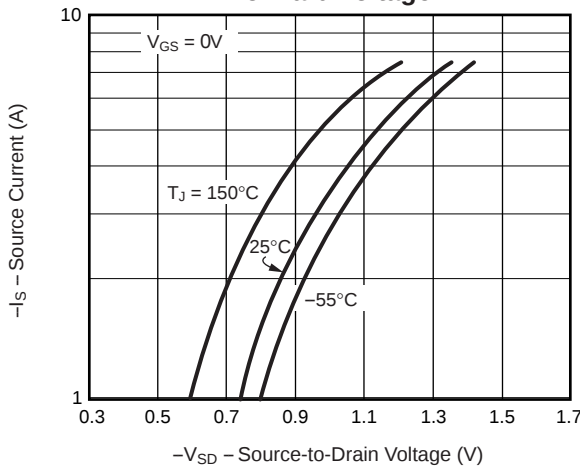


Fig. 10 – Thermal Impedance

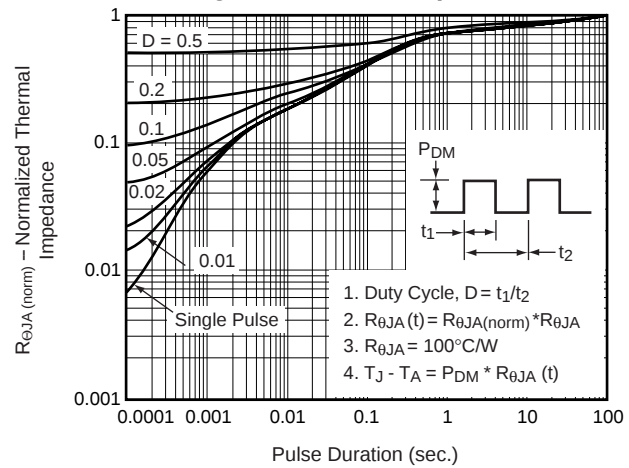


Fig. 11 – Power vs. Pulse Duration

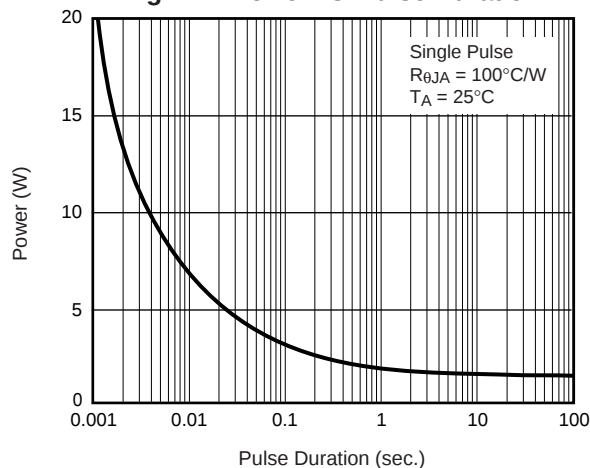


Fig. 12 – Maximum Safe Operating Area

