High-Performance
32K×32 Burst Synchronous
CMOS SRAM

AS7C33232
AS7C33232L

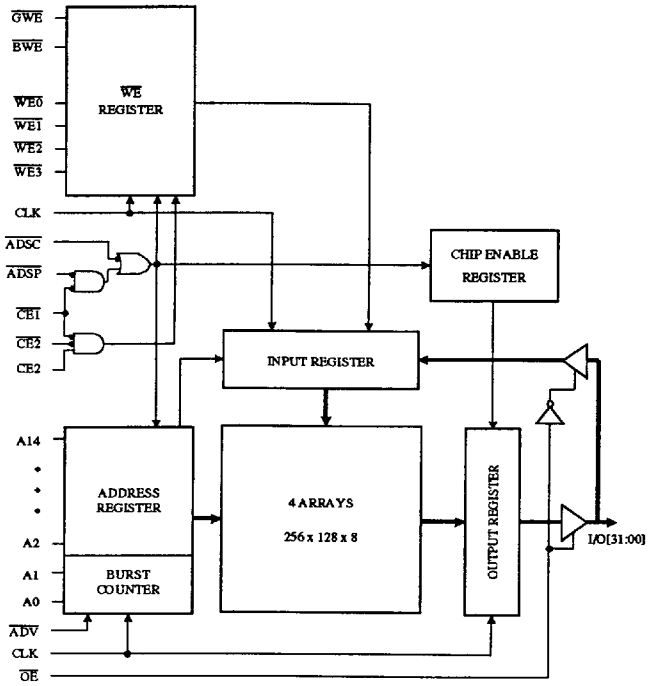
ADVANCE INFORMATION

32K×32 Synchronous Pipelined Burst SRAM

FEATURES

- Organization: 32,768 words × 32 bits
- Fully synchronous pipelined operation
- Fast clocking speed: 75/66/60 MHz
- Fast clock to data access: 6/7/8 ns
- Self-timed write cycle
- On-chip address, control, and data registers
- Byte write enable & global write enable control
- Asynchronous output enable control
- $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$ burst control pins
- Pentium™ or PowerPC™ count sequence
- Transparent logic support for 1 or 2 CPUs
- Single 3.3 ±0.3V power supply
- 5V safe inputs
- ESD protection >2000 volts
- Latch-up current > 200 mA

LOGIC BLOCK DIAGRAM



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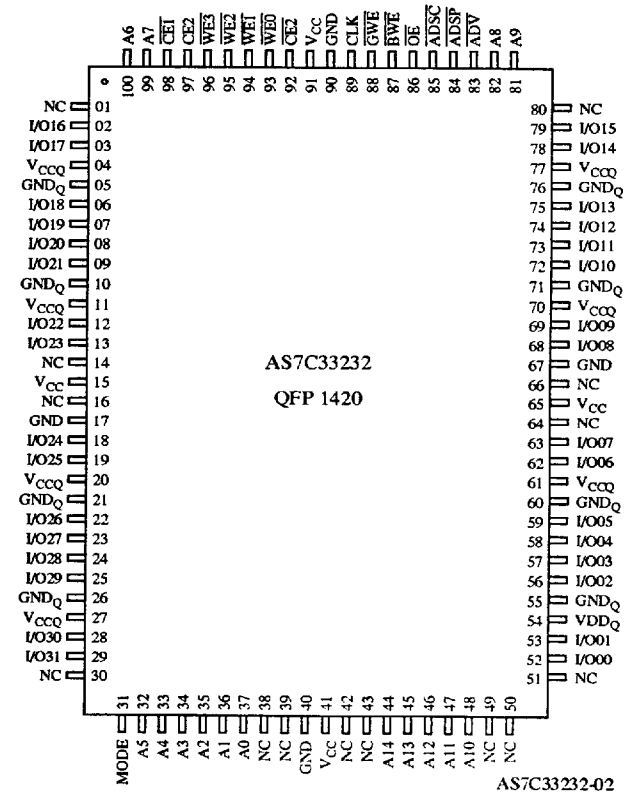
PIN ARRANGEMENT



AS7C33232-02

SELECTION GUIDE

		7C33232-13	7C33232-15	7C33232-17	Unit
Minimum cycle time		13.3	15	16.6	ns
Maximum clock frequency		75	66	60	MHz
Maximum output enable access time		5	6	7	ns
Maximum operating current		280	240	220	mA
Maximum standby current		30	30	30	mA
Maximum CMOS standby current (DC)		6	6	6	mA
	L	3	3	3	mA

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FUNCTIONAL DESCRIPTION

The AS7C33232 is a high performance CMOS 1,024,576-bit synchronous Static Random Access Memory (SRAM) organized as 32,768 words × 32 bits, and incorporating a 2-bit burst counter and output register. It is designed for high performance 3.3V Pentium™ and PowerPC™ cache applications.

Fast cycle times of 13/15/17 ns with output enable access times (t_{OE}) of 5/6/7 ns are ideal for 75, 66, and 60 MHz bus frequencies. Three chip enable inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{ADSC}$), or the processor address strobe ($\overline{ADSP}$). The burst advance pin ($\overline{ADV}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register when $\overline{ADSP}$ is sampled LOW, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. In a read operation the data accessed by the current address, registered in the address registers by the positive edge of CLK, are carried to the data-out registers on the next positive edge of CLK and driven on the output pins. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{WE}$ is sampled HIGH, $\overline{ADV}$ is sampled LOW, and both address strobes are HIGH.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting $\overline{WE}$. A global write enable $\overline{GWE}$ writes all 32 bits regardless of the state of individual $\overline{WE0}$–$\overline{WE3}$ inputs. Alternately, when $\overline{GWE}$ is HIGH, one or more bytes may be written by asserting $\overline{BWE}$ and the appropriate individual byte $\overline{WE}$ signal(s). $\overline{WE0}$ controls I/O0-I/O7; $\overline{WE1}$ controls I/O8-I/O15; $\overline{WE2}$ controls I/O16-I/O23; and $\overline{WE3}$ controls I/O24-I/O31.

$\overline{WE}$ is ignored on the clock edge that samples $\overline{ADSP}$ LOW, but is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{WE}$ is sampled LOW (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{WE}$ is sampled LOW. Address is incremented internally to the next burst of address if $\overline{WE}$ and $\overline{ADV}$ are sampled LOW.

Read or write cycles may also be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ follow.

- $\overline{ADSP}$ must be sampled HIGH when $\overline{ADSC}$ is sampled LOW to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ signals are sampled on the clock edge that samples $\overline{ADSC}$ LOW (and $\overline{ADSP}$ HIGH).
- Master chip select $\overline{CE1}$ blocks $\overline{ADSP}$, but not $\overline{ADSC}$.

Burst operation is selectable with the MODE input. With MODE unconnected or driven HIGH burst operations use a Pentium/486 count sequence. With MODE driven LOW the device uses a linear count sequence, suitable for PowerPC and many other applications (refer to the Burst Sequence Table on page 3).

The AS7C33232 operates from a single 3.3±0.3V supply. Inputs and outputs are TTL compatible and 5V tolerant. The AS7C33232 is packaged in a 100 pin 14x20 mm QFP package.

SIGNAL DESCRIPTIONS

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ are synchronous to this clock.
A0–A14	I	SYNC	Address. Sampled when all chip enables are active and $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
I/O0–I/O31	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE1}$	I	SYNC	Master Chip Enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE1}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the SYNCHRONOUS TRUTH TABLE for more information.
CE2, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active HIGH and active LOW, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE1}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address status processor. Asserted LOW to load a new bus address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address status controller. Asserted LOW to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Advance. Asserted LOW to continue burst read/write.
$\overline{GWE}$	I	SYNC default = HIGH	Global write enable. Asserted LOW to write all 32 bits. When HIGH, $\overline{BWE}$ and $\overline{WE0}$–$\overline{WE3}$ control write enable. *This signal is internally pulled HIGH.*
$\overline{BWE}$	I	SYNC default = LOW	Byte write enable. Asserted LOW with $\overline{GWE}$ = HIGH to to enable effect of $\overline{WE0}$–$\overline{WE3}$ inputs. *This signal is internally pulled LOW.*
$\overline{WE0}$–$\overline{WE3}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ = HIGH and $\overline{BWE}$ = LOW. If any of $\overline{WE0}$–$\overline{WE3}$ is active with $\overline{GWE}$ = HIGH and $\overline{BWE}$ = LOW the cycle is a write cycle. If all $\overline{WE0}$–$\overline{WE3}$ are inactive the cycle is a read cycle.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is synchronously enabled.
MODE	I	STATIC default = HIGH	Count mode. When driven HIGH, count sequence follows Intel XOR convention. When driven LOW, count sequence follows Motorola/linear convention. *This signal is internally pulled HIGH.*

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SYNCHRONOUS TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	WRITE*n*	$\overline{OE}$	Address Accessed	CLK	Operation
H	X	X	X	L	X	X	X	NA	L to H	Deselect
L	L	X	L	X	X	X	X	NA	L to H	Deselect
L	L	X	H	L	X	X	X	NA	L to H	Deselect
L	X	H	L	X	X	X	X	NA	L to H	Deselect
L	X	H	H	L	X	X	X	NA	L to H	Deselect
L	H	L	L	X	X	F	L	External	L to H	Begin burst read
L	H	L	L	X	X	F	H	External	L to H	Begin burst read
L	H	L	H	L	X	F	L	External	L to H	Begin burst read
L	H	L	H	L	X	F	H	External	L to H	Begin burst read
X	X	X	H	H	L	F	L	Next	L to H	Cont. burst read
X	X	X	H	H	L	F	H	Next	L to H	Cont. burst read
X	X	X	H	H	H	F	L	Current	L to H	Suspend burst
X	X	X	H	H	H	F	H	Current	L to H	Suspend burst
H	X	X	X	H	L	F	L	Next	L to H	Cont. burst read
H	X	X	X	H	L	F	H	Next	L to H	Cont. burst read
H	X	X	X	H	H	F	L	Current	L to H	Suspend burst
H	X	X	X	H	H	F	H	Current	L to H	Suspend burst
L	H	L	H	L	X	T	X	External	L to H	Begin burst write
X	X	X	H	H	L	T	X	Next	L to H	Cont. burst write
H	X	X	X	H	L	T	X	Next	L to H	Cont. burst write
X	X	X	H	H	H	T	H	Current	L to H	Suspend burst write
H	X	X	X	H	H	T	H	Current	L to H	Suspend burst write

Key: X = Don't Care, L = LOW, H = HIGH, T = TRUE, F = FALSE.

WRITE ENABLE TRUTH TABLE (per byte)

$\overline{GWE}$	$\overline{BWE}$	$\overline{WEn}$	WRITE*n*
L	X	X	T
X	L	L	T
H	H	X	F
H	L	H	F

Key: X = Don't Care, L = LOW, H = HIGH.

ASYNCHRONOUS $\overline{OE}$ TRUTH TABLE

$\overline{OE}$	I/O [31:0]
L	Read data
H	HIGH-Z

Note: For write cycles that follow read cycles, output buffers must be disabled with $\overline{OE}$ to prevent data bus contention.

Key: L = LOW, H = HIGH.

BURST SEQUENCE TABLE

	Mode = HIGH/No Connect Pentium Count Sequence				Mode = LOW Linear Count Sequence			
Start Address	00	01	10	11	00	01	10	11
Second Address	01	00	11	10	01	10	11	00
Third Address	10	11	00	01	10	11	00	01
Fourth Address	11	10	01	00	11	00	01	10

Note: The burst sequence wraps around to its initial state upon completion.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage relative to GND	V_{CC}	-0.5	+4.6	V
Input Voltage relative to GND	V_{IN}	-0.5	+6.0	V
Power Dissipation	P_D	–	1.2	W
Storage Temperature (Plastic)	T_{stg}	-55	+150	°C
Temperature under Bias	T_{bias}	-10	+85	°C
DC Output Current	I_{out}	–	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS (T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	GND	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.2	–	5.5	V
	V_{IL}	-0.5*	–	0.8	V

* V_{IL} min = -3.0V for pulse width less than $t_{RC}/2$.

DC OPERATING CHARACTERISTICS (V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test Conditions	-13		-15		-17		Unit
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}	-2	+2	-2	+2	-2	+2	µA
Output Leakage Current	$\|I_{LO}\|$	$\overline{OE} \geq V_{IH}$, V_{CC} = Max, V_{out} = GND to V_{CC}	-2	+2	-2	+2	-2	+2	µA
Operating Power Supply Current	I_{CC}	$\overline{CE1} = V_{IL}$, CE2 = V_{IH}, $\overline{CE2} = V_{IL}$, $f = f_{max}$, I_{out} = 0 mA	–	280	–	240	–	220	mA
Standby Power Supply Current	I_{SB}	Deselected, $f = f_{max}$	–	30	–	30	–	30	mA
	I_{SB1}	Deselected, f = 0, all $V_{IN} \leq$ 0.2V or $\geq V_{CC}$ - 0.2V	–	6	–	6	–	6	mA
		L	–	3	–	3	–	3	mA
Output Voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = -4 mA, V_{CC} = Min	2.4	–	2.4	–	2.4	–	V

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CAPACITANCE [1]

(f = 1 MHz, T_a = Room Temperature, V_{CC} = 3.3±0.3V)

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input Capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{CE2}$, $\overline{WE}$, $\overline{OE}$, $\overline{ADSP}$, $\overline{ADSC}$, $\overline{ADV}$	V_{in} = 0V	5	pF
I/O Capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

READ CYCLE, WRITE CYCLE, READ/WRITE CYCLE [2]

(V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	-13		-15		-17		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Cycle Time	t_{CYC}	13	-	15	-	17	-	ns	
Clock Access Time	t_{CD}	-	6	-	7	-	8	ns	
Output Enable to Data Valid	t_{OE}	-	5	-	6	-	7	ns	3
Clock HIGH to Output LOW-Z	t_{LZC}	2	-	2	-	2	-	ns	1, 4
Output Hold from Clock HIGH	t_{OH}	2	-	2	-	2	-	ns	1, 4
Output Enable LOW to Output LOW-Z	t_{LZOE}	2	-	2	-	2	-	ns	1, 4
Output Enable HIGH to Output HIGH-Z	t_{HZOE}	2	5	2	6	2	6	ns	1, 4
Clock HIGH to Output HIGH-Z	t_{HZC}	-	5	-	6	-	6	ns	1, 4
Clock HIGH Pulse Width	t_{CH}	4.5	-	5.5	-	6	-	ns	
Clock LOW Pulse Width	t_{CL}	4.5	-	5.5	-	6	-	ns	
Address Setup to Clock HIGH	t_{AS}	2.5	-	2.5	-	2.5	-	ns	5, 6
Address Status Setup to Clock HIGH	t_{SS}	2.5	-	2.5	-	2.5	-	ns	5, 6
Data Setup to Clock HIGH	t_{DS}	2.5	-	2.5	-	2.5	-	ns	5, 6
Write Setup to Clock HIGH	t_{WS}	2.5	-	2.5	-	2.5	-	ns	5, 6
Address Advance Setup to Clock HIGH	t_{ADVS}	2.5	-	2.5	-	2.5	-	ns	5, 6
Chip Select Setup to Clock HIGH	t_{CSS}	2.5	-	2.5	-	2.5	-	ns	5, 6
Address Hold from Clock HIGH	t_{AH}	0.5	-	0.5	-	0.5	-	ns	5, 6
Address Status Hold from Clock HIGH	t_{SH}	0.5	-	0.5	-	0.5	-	ns	5, 6
Data Hold from Clock HIGH	t_{DH}	0.5	-	0.5	-	0.5	-	ns	5, 6
Write Hold from Clock HIGH	t_{WH}	0.5	-	0.5	-	0.5	-	ns	5, 6
Address Advance Hold from Clock HIGH	t_{ADVH}	0.5	-	0.5	-	0.5	-	ns	5, 6
Chip Select Hold from Clock HIGH	t_{CSH}	0.5	-	0.5	-	0.5	-	ns	5, 6

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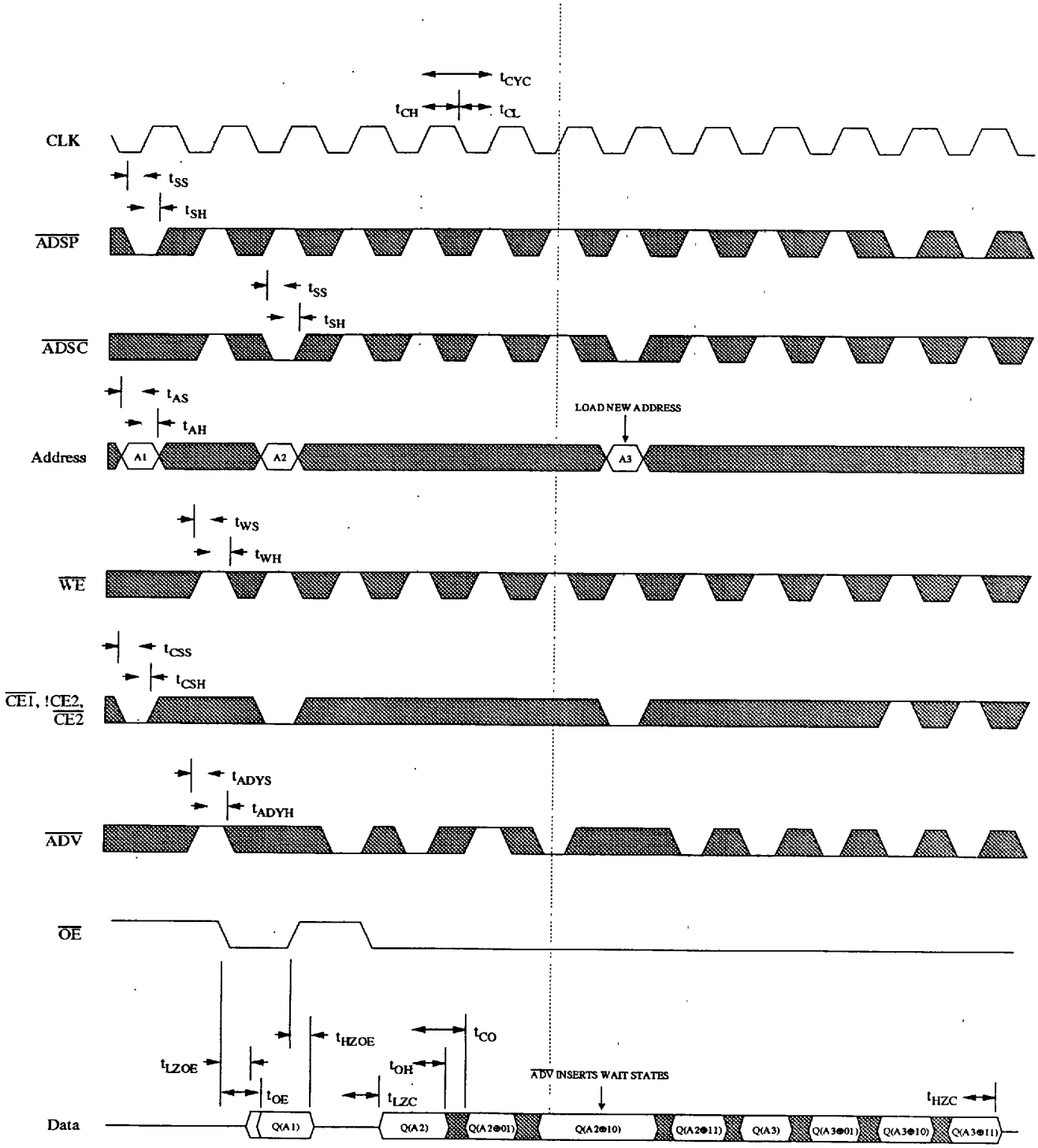
TIMING WAVEFORM OF READ CYCLE



Note: ⊕ = XOR when MODE = HIGH/No Connect; ⊕ = ADD when MODE = LOW. Refer to Burst Sequence Table, pg.3.

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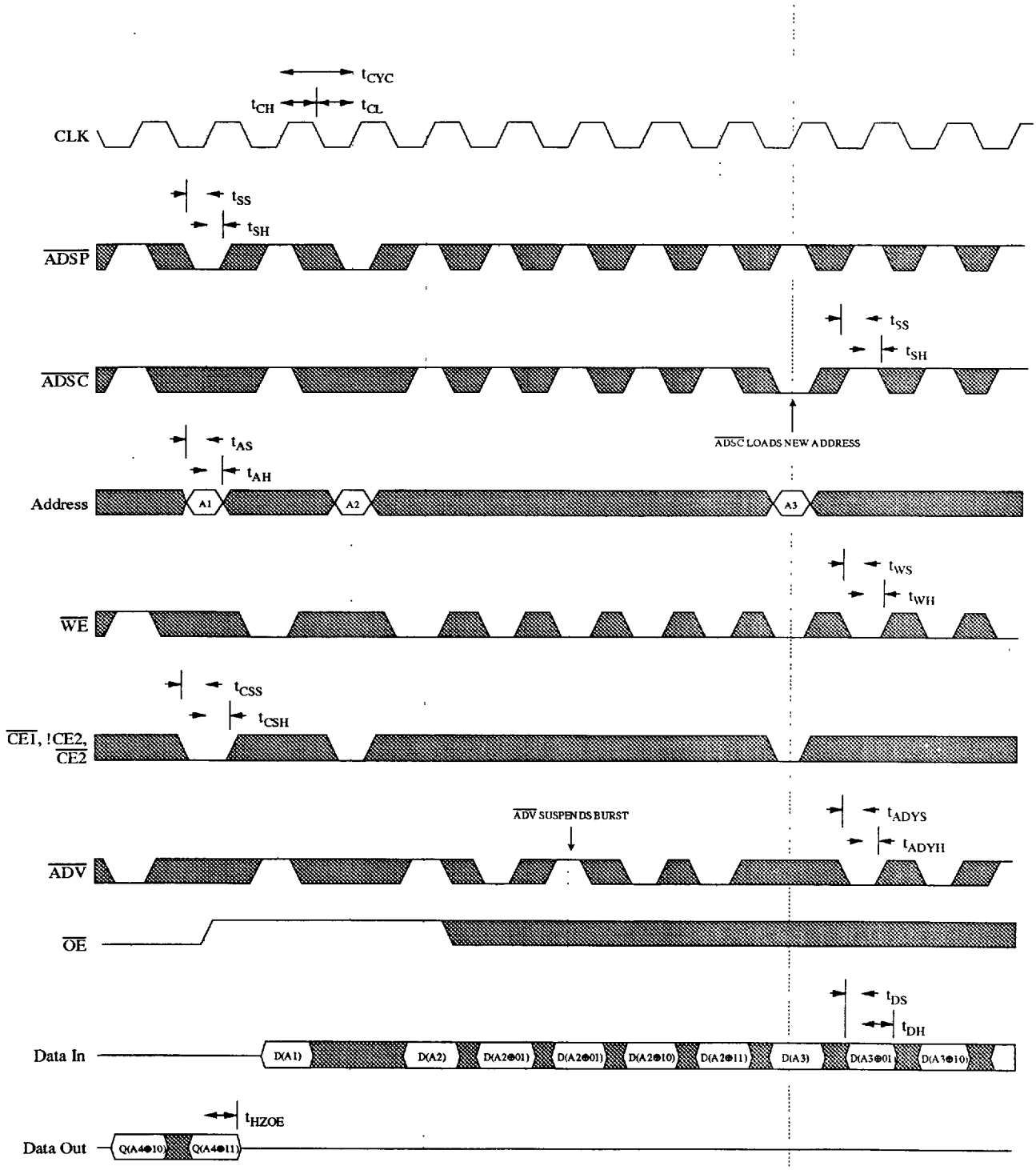
TIMING WAVEFORM OF WRITE CYCLE



Note: ⊕ = XOR when MODE = HIGH/No Connect; ⊕ = ADD when MODE = LOW. Refer to Burst Sequence Table, pg.3.

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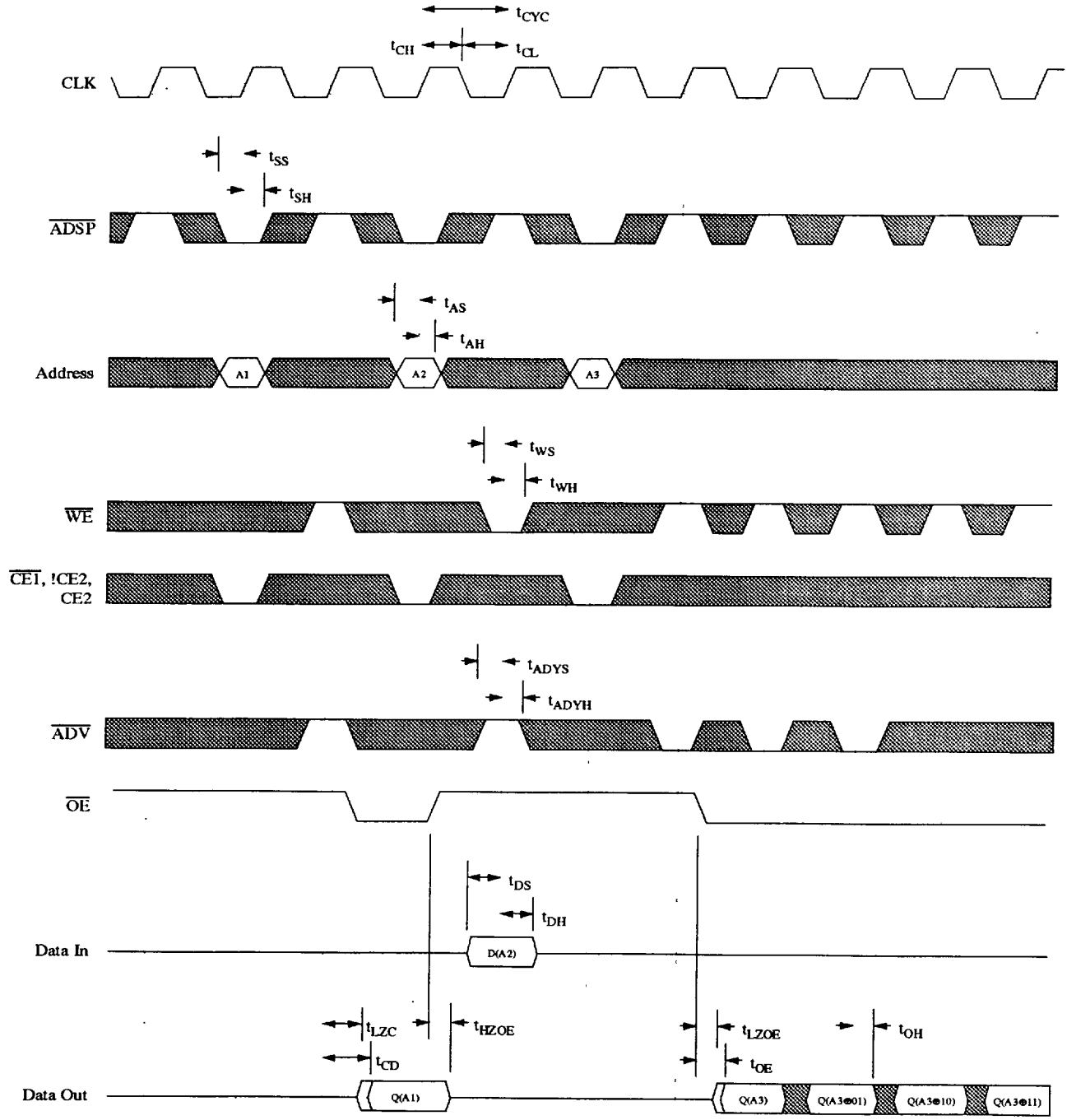
TIMING WAVEFORM OF READ/WRITE CYCLE



Note: ⊕ = XOR when MODE = HIGH/No Connect; ⊕ = ADD when MODE = LOW. Refer to Burst Sequence Table, pg.3.

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AC TEST CONDITIONS

- Output Load: see Figure B, except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC} see Figure C.
- Input Pulse Level: GND to 3V. See Figure A.
- Input Rise and Fall Time (Measured at 0.3V and 2.7V): 2 ns. See figure A.
- Input and Output Timing Reference Levels: 1.5V.

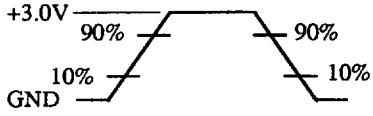

Figure A: Input Waveform

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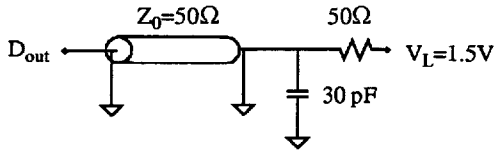

Figure B: Output Load (A)

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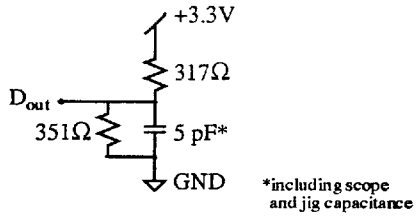

Figure C: Output Load(B) for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC}

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NOTES

1. This parameter is guaranteed but not tested.
2. For test conditions, see *AC Test Conditions*, Figures A, B, C.
3. $\overline{OE}$ state is 'don't care" when a byte write enable is sampled LOW.
4. This parameter is sampled and not 100% tested.
5. A read cycle is defined as byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A write cycle is defined as at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
6. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP or ADSC is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK with either $\overline{ADSP}$ or $\overline{ADSC}$ LOW to remain enabled.

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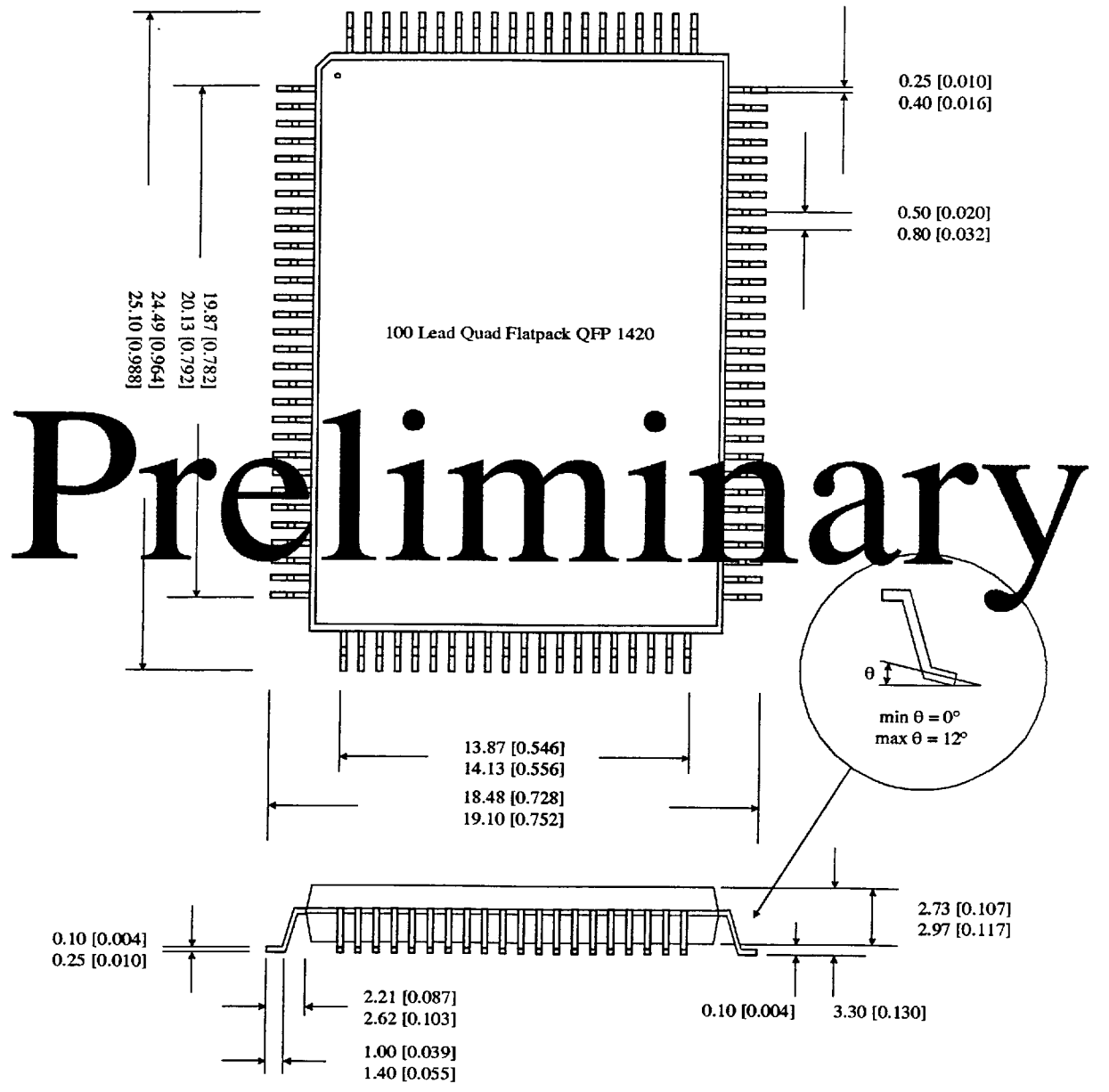
PACKAGE DIMENSIONS

Dimensions:

MIN mm. [MIN inches]
MAX mm. [MAX inches]



Preliminary

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APPLICATION CONNECTIVITY EXAMPLES

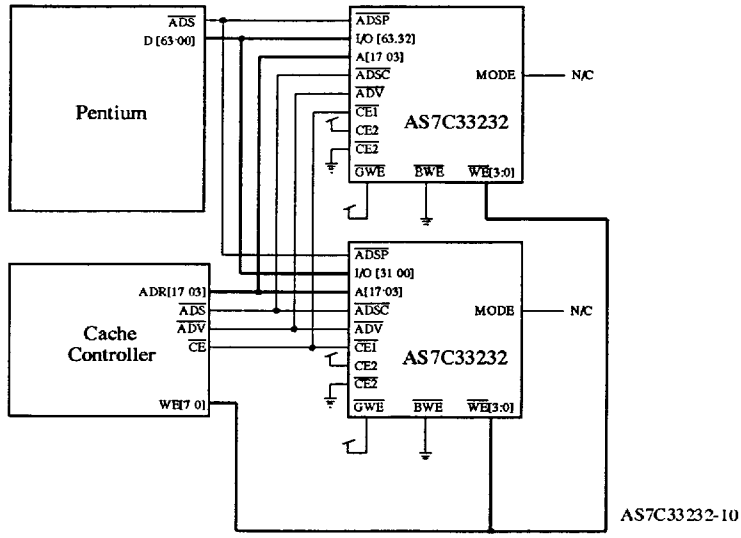

Figure A: Pentium 256K Cache

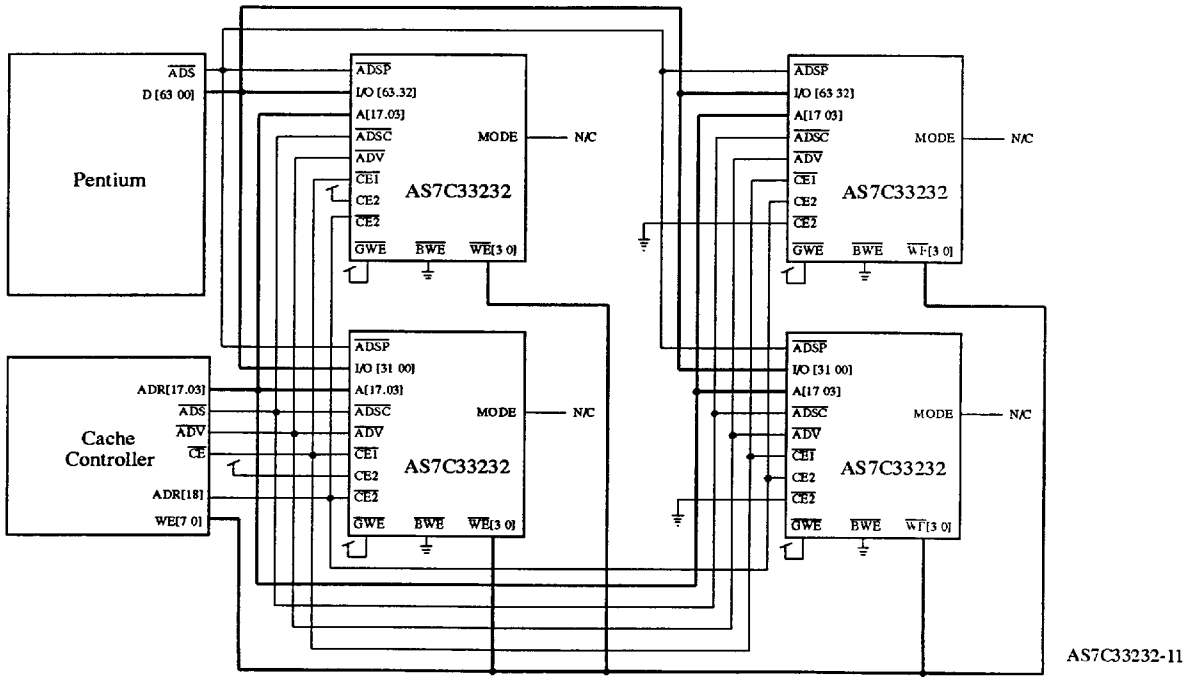

Figure B: Pentium 512K Cache

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ORDERING INFORMATION

Package \ Min Cycle Time	13 ns	15 ns	17 ns
QFP 1420	AS7C33232-13QC AS7C33232L-13QC	AS7C33232-15QC AS7C33232L-15QC	AS7C33232-17QC AS7C33232L-17QC

PART NUMBERING SYSTEM

AS7C	3	3232	X	-XX	Q	C
SRAM Prefix	Blank = 5V Supply 3 = 3.3V Supply	Device Number	Blank = Std. Power L = Low Power	Min Cycle Time	Package: Q = QFP1420	Commercial Temperature Range, 0°C to 70° C

REPRESENTATIVES, DISTRIBUTORS, AND SALES OFFICES

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