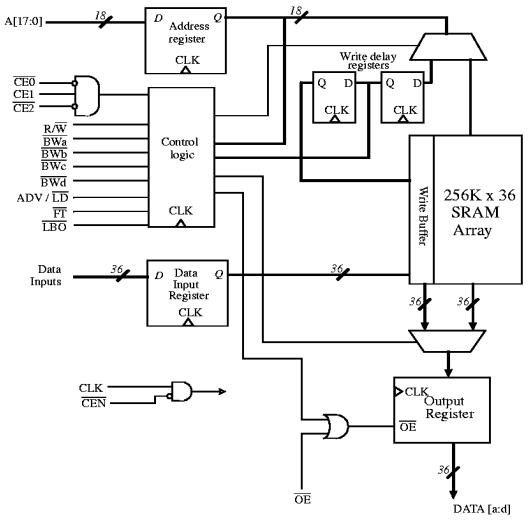
AS7C3256K36Z
AS7C3256K32Z

3.3V 256K×32/36 synchronous burst SRAM with NTD™

Features

- Organization: 262,144 words × 32 or 36 bits
- NTD™ architecture for efficient bus operation
- Fast clock speeds to 150 MHz in LVTTL/LVCMOS
- Fast clock to data access: 3.8/4/5 ns
- Fast $\overline{OE}$ access time: 3.5/3.8/4 ns
- Fully synchronous operation
- "Flow-through" mode
- Asynchronous output enable control
- Multiple packaging options
  - Economical 100-pin TQFP package
  - Chip-scale fBGA package for smallest footprint
- Byte write enables
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 3.3 core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- 10 mW typical standby power

Logic block diagram



Pin arrangement

For information on the pin arrangement for the TQFP package, refer to the section entitled "Pin arrangement for TQFP (top view)" on page page 3.

For information on the pin arrangement for the chip-scale fBGA package, refer to the section entitled "Pin arrangement for chip-scale fBGA (top view)" on page page 3.

Selection guide

	7C3256K36-3.8	7C3256K36-4	7C3256K36-5	Units
Minimum cycle time	6.7	7.5	10	ns
Maximum pipelined clock frequency	150	133.3	100	MHz
Maximum pipelined clock access time	3.8	4	5	ns
Maximum operating current	325	300	250	mA
Maximum standby current	60	60	60	mA
Maximum CMOS standby current (DC)	5	5	5	mA

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SRAM

Functional description

The AS7C3256K36Z family is a high performance CMOS 8 Mbit synchronous Static Random Access Memory (SRAM) organized as 262,144 words × 32 or 36 bits and incorporates a LATE LATE Write.

This variation of the 8Mb sychronous SRAM uses the No Turnaround Delay (NTD™) architecture, featuring an enhanced write operation that improves bandwidth over pipeline burst devices. In a normal pipeline burst device, the write data, command, and address are all applied to the device on the same clock edge. If a read command follows this write information, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or read-modify-write operations.

NTD™ devices use the memory bus more efficiently by introducing a write 'latency' which matches the two cycle read latency. Write data is applied two cycles after the write command and address, allowing the read pipeline to clear. With NTD™, write and read operations can be used in any order without producing dead bus cycles.

The single register flow-through mode of the AS7C3256K36Z and AS7C3256K32Z can disable output circuit registers. This allows the device to operate in 2-1-1-1 mode rather than 3-1-1-1 found in two-stage pipeline architecture timing. The single register flow-through mode sacrifices access and cycle times for lower latency. Consult AC timing parameters for more details.

Assert R/$\overline{W}$ low to perform write cycles. Byte write enable controls write access to specific bytes, or can be tied low for full 32/36 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable $\overline{OE}$ does not need to be toggled for write operations; it can be tied low for normal operations. Outputs go to a high impedance state when the device is de-selected by any of the three chip enable inputs In pipeline mode, a two cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read and write operations. When ADV is high, external addresses are ignored, and internal address counters increment in the count sequence specified by the $\overline{LBO}$ control. Any device operations, including burst, can be stalled using the $\overline{CEN}$ clock enable input. If $\overline{CEN}$ is high at the rising edge of clock, all operations are effectively stalled.

The AS7C3256K36Z and AS7C3256K32Z operate with a 3.3V ± 5% power supply for the device core (V_{DD}). DQ circuits use a separate power supply (V_{DDQ}) that operates across 3.3V or 2.5V ranges. These devices are available in a 100-pin 14×20 mm TQFP and 119 ball fine-pitch Ball-Grid-Array (fBGA) packaging.

Capacitance [1]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	V_{in} = V_{out} = 0V	7	pF

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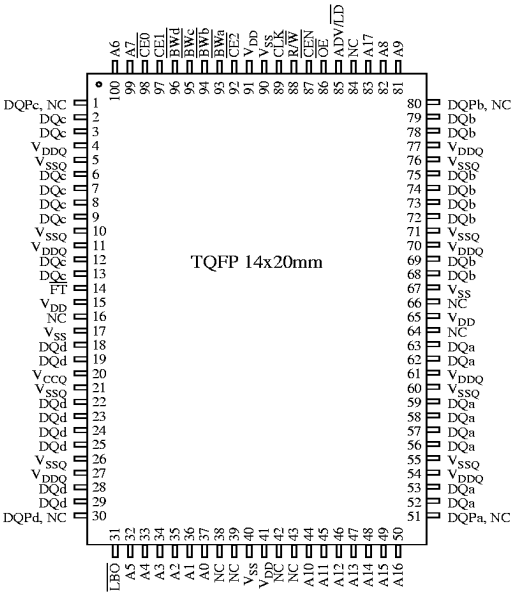
Pin arrangement for TQFP (top view)



Note: Pins 1,30,51,80 are NC for ×32

Pin arrangement for chip-scale fBGA (top view)

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	NC	A	A	V_{DDQ}
B	NC	CE1	A	ADV/$\overline{LD}$	A	A	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQc	DQPc	V_{SS}	NC	V_{SS}	DQPb	DQb
E	DQc	DQc	V_{SS}	$\overline{CE0}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{OE}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{BWc}$	NC	$\overline{BWb}$	DQb	DQb
H	DQc	DQc	V_{SS}	R/$\overline{W}$	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	Clk	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{BWd}$	NC	$\overline{BWa}$	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{CEN}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	A	V_{SS}	DQa	DQa
P	DQd	DQPd	V_{SS}	A	V_{SS}	DQPa	DQa
R	NC	A	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Note: Pins 2D, 2P, 6D, 6P are NC for ×32.

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ are synchronous to this clock.
$\overline{CEN}$	I	SYNC	Clock enable. When de-asserted HIGH, the clock input signal is masked.
A0–A17	I	SYNC	Address. Sampled when all chip enables are active and LD is asserted.
DQ[a,b,c,d]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$, CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. De-assertion of any chip enable causes power-down of the device.
ADV/$\overline{LD}$	I	SYNC	Advance or Load. When sampled HIGH, the internal burst address counter will increment in the order defined by the $\overline{LBO}$ input value. When LOW, a new address is loaded.
R/$\overline{W}$	I	SYNC	Write enable. Asserted LOW to initiate a write operation.
$\overline{BW}$[a,b,c,d]	I	SYNC	Byte write enables. Used to control write of individual bytes. When sampled LOW with $\overline{WE}$, data is accepted for write operations to DQ banks a,b,c, and d respectively.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is synchronously enabled.
$\overline{LBO}$	I	STATIC	Count mode. When driven High, count sequence follows Intel XOR convention. When driven Low, count sequence follows linear convention. This input should be static.
$\overline{FT}$	I	STATIC	Flow-through mode.When low, enables single register flow-through mode. Connect to V_{DD} if unused or for pipelined operation.
ZZ	I	ASYNC	Sleep. Places device in low power mode; data is retained. Connect to GND if unused.
nc	-	-	No connects. Note that pin 84 will be used for future address expansion to 16Mb density.

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Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.5	+4.6	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.5	V_{DDQ} + 0.5	V
Power dissipation	P_D	–	1.2	W
DC output current	I_{OUT}	–	30	mA
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature under bias	T_{bias}	–65	+135	°C

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Synchronous truth table

$\overline{CE0}$	CE1	$\overline{CE2}$	ADV/$\overline{LD}$	R/$\overline{W}$	$\overline{BW}$[a:d]	$\overline{OE}$	Address source	CLK	Operation
H	X	X	(1)	X	X	X	NA	L to H	Deselect, high-Z
X	L	X	(1)	X	X	X	NA	L to H	Deselect, high-Z
X	X	H	(1)	X	X	X	NA	L to H	Deselect, high-Z
L	H	L	L	H	X	X	External	L to H	Begin read
L	H	L	H	H	X	X	External	L to H	Begin burst read
L	H	L	L	L	L(2)	X	External	L to H	Begin write
L	H	L	H	L	L(2)	X	External	L to H	Begin burst write

Key: X = Don't Care, L = Low, H = High.

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Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{DD}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
3.3V I/O supply voltage		V_{DDQ}	3.135	3.3	3.465	V
		GND_Q	0.0	0.0	0.0	
2.5V I/O supply voltage		V_{DDQ}	2.35	2.5	2.65	V
		GND_Q	0.0	0.0	0.0	
Input voltages†	Address and control pins	V_{IH}	2.0	–	4.5	V
		V_{IL}	–0.5*	–	0.8	V
	I/O pins	V_{IH}	2.0	–	V_{DDQ} + 0.5	V
		V_{IL}	-0.5*	–	0.8	
Ambient operating temperature		T_A	0	–	70	℃

* V_{IL} min = –2.0V for pulse width less than 0.2 x t_{RC}.

† Input voltage ranges apply to 3.3V I/O operation. For 2.5V operation, contact factory for input specifications.

DC electrical characteristics

			-3.8		-4		-5		
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{DD} = Max, V_{in} = GND to V_{DD}	–	2	–	2	–	2	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{DD} = Max, V_{out} = GND to V_{DD}	–	2	–	2	–	2	µA
Operating power supply current	I_{CC}	$\overline{CE} = V_{IL}$, $CE = V_{IH}$, $\overline{CE} = V_{IL}$, f = f_{max}, I_{out} = 0 mA	–	325	–	300	–	250	mA
Standby power supply current	I_{SB}	Deselected, f = f_{max}	–	60	–	60	–	60	mA
	I_{SB1}	Deselected, f = 0, all $V_{IN} \leq$ 0.2V or $\geq V_{DD}$ - 0.2V	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.6V	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.0V	2.4	–	2.4	–	2.4	–	V

DC electrical characteristics for 2.5V I/O operation

			-166		-150		-133		-100		
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{DD} = Max, V_{out} = GND to V_{DD}	-1	1	-1	1	-1	1	-1	1	µA
Output voltage	V_{OL}	I_{OL} = 2 mA, V_{DDQ} = 2.65V	–	0.7	–	0.7	–	0.7	–	0.7	V
	V_{OH}	I_{OH} = –2 mA, V_{DDQ} = 2.35V	1.7	–	1.7	–	1.7	–	1.7	–	

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Timing characteristics over operating range

		-3.8		-4		-5			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Clock frequency	F_{MAX}	-	150	-	133	-	100	MHz	1
Cycle time (pipelined mode)	t_{CYC}	6.6	-	7.5	-	10	-	ns	
Cycle time (flow-through mode)	t_{CYCF}	10	-	12	-	15	-	ns	
Clock access time (pipelined mode)	t_{CD}	-	3.8	-	4	-	5	ns	
Clock access time (flow-through mode)	t_{CDF}	-	6.6	-	7.5	-	10	ns	
Output enable Low to data valid	t_{OE}	-	3.5	-	3.8	-	4	ns	
Clock High to output Low Z	t_{LZC}	0	-	0	-	0	-	ns	8
Data output hold from clock High	t_{OH}	1.5	-	1.5	-	2	-	ns	8
Output enable Low to output Low Z	t_{LZOE}	1	-	1.5	-	2	-	ns	8
Output enable High to output High Z	t_{HZOE}	-	3.5	-	4	-	4	ns	8
Clock High to output High Z	t_{HZC}	-	3	-	3.5	-	3.5	ns	8
Clock High to output High Z	t_{HZCN}	-	1.5	-	2	-	2.5	ns	1,9
Clock High pulse width	t_{CH}	2.6	-	2.8	-	3	-	ns	
Clock Low pulse width	t_{CL}	2.6	-	2.8	-	3	-	ns	
Address and Control setup to clock High	t_{AS}	1.3	-	1.5	-	1.5	-	ns	
Data setup to clock High	t_{DS}	1.3	-	1.5	-	1.5	-	ns	
Write setup to clock High	t_{WS}	1.3	-	1.5	-	1.5	-	ns	
Chip select setup to clock High	t_{CSS}	1.3	-	1.5	-	1.5	-	ns	
Address hold from clock High	t_{AH}	0.5	-	0.5	-	0.5	-	ns	
Data hold from clock High	t_{DH}	0.5	-	0.5	-	0.5	-	ns	
Write hold from clock High	t_{WH}	0.5	-	0.5	-	0.5	-	ns	
Chip select hold from clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	ns	
Output rise time (0 pF load)	t_R	1.5	-	1.5	-	1.5	-	V/ns	1
Output fall time (0 pF load)	t_F	1.5	-	1.5	-	1.5	-	V/ns	1

See "Notes" on page 9.

Key to switching waveforms

Rising input Falling input Undefined output/don't care

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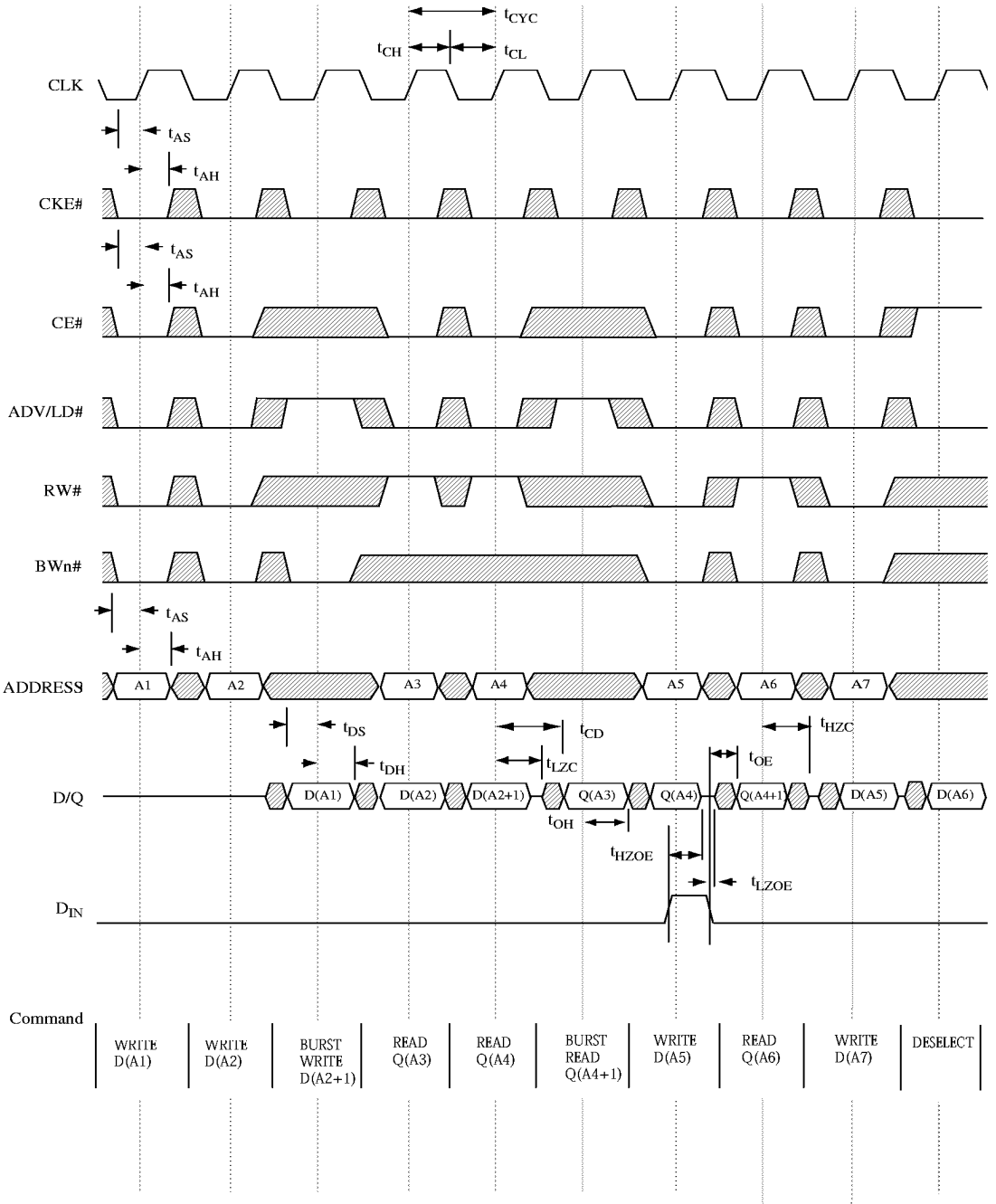
Timing waveform of read/write cycle



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.
$\overline{WE}$[0:3] is don't care.

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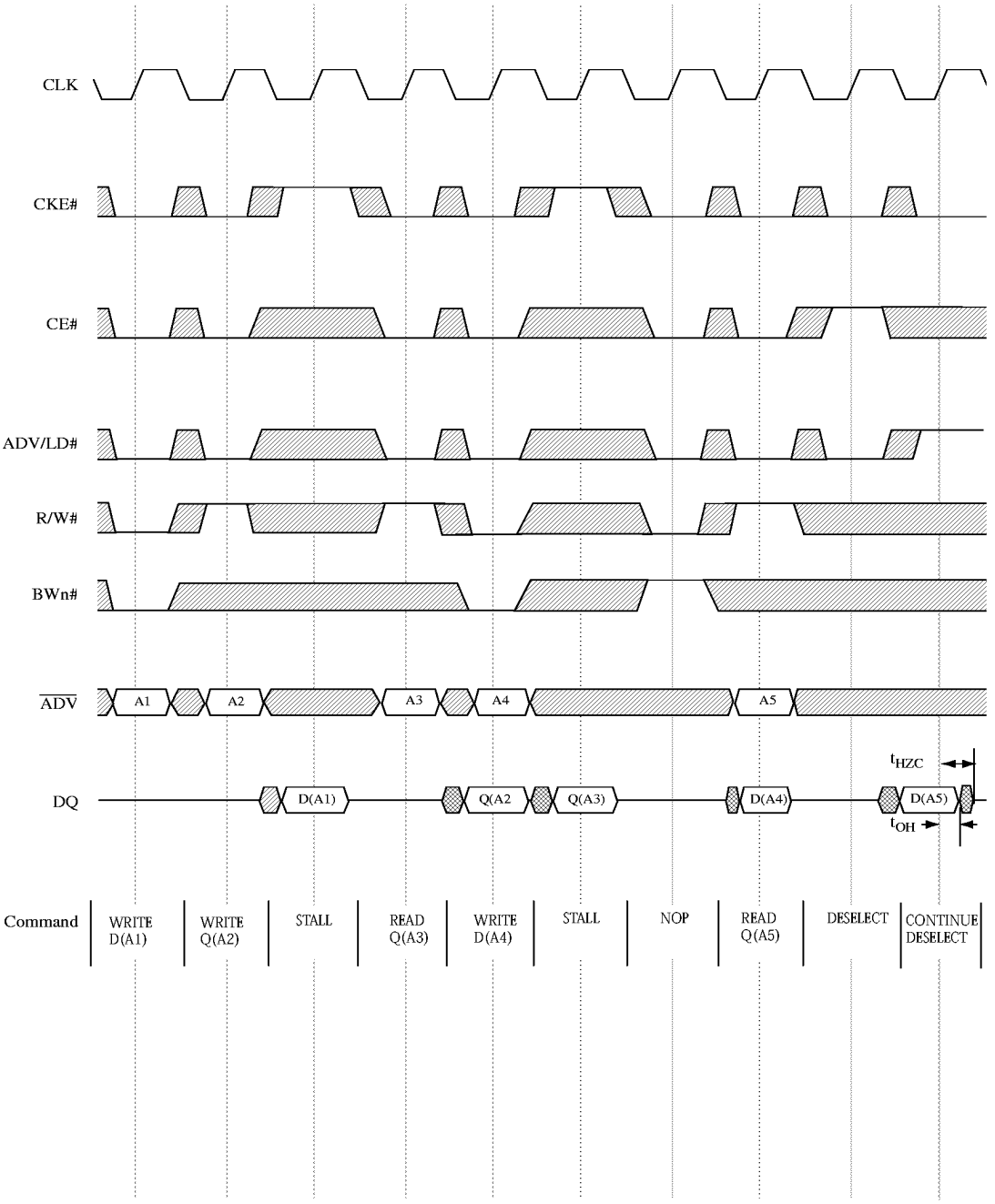
NOP, stall and deselect cycles



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.
Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.
Note: $\overline{OE}$ is Low.

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Notes

1 This parameter is guaranteed but not tested.
2 For test conditions, see AC Test Conditions, Figures A, B, C.
3 This parameter is sampled and not 100% tested.
4 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.
5 Typical values measured at 3.3V, 25 ℃ and 10 ns cycle time.
6 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.
7 Transitions are measured ±500 mV from steady state voltage. Output loading specified with C_L = 5 pF as in Figure C.
8 t_{HZOE} is less than t_{LZOE}; and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
9 t_{HZCN} is a 'no load' parameter to indicate exactly when SRAM outputs have stopped driving.

AC test conditions

- Output Load: see Figure B, except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC} see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (Measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

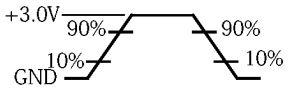

Figure A: Input waveform

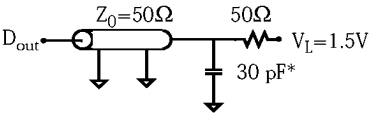

Figure B: Output load (A)

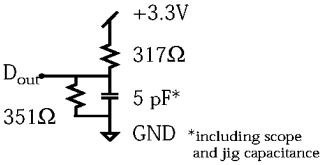

Figure C: Output load (B)

AS7C3256K32Z and AS7C3256K36Z ordering information

Package	Width	150 MHz	133 MHz	100 MHz
TQFP	×32	AS7C3256K32Z-3.8TQC	AS7C3256K32Z-4TQC	AS7C3256K32Z-5TQC
TQFP	×36	AS7C3256K36Z-3.8TQC	AS7C3256K36Z-4TQC	AS7C3256K36Z-5TQC
fBGA	×32	AS7C3256K32Z-3.8BC	AS7C3256K32Z-4BC	AS7C3256K32Z-5BC
fBGA	×36	AS7C3256K36Z-3.8BC	AS7C3256K36Z-4BC	AS7C3256K36Z-5BC

AS7C3256K32Z and AS7C3256K36Z part numbering system

AS7C	3	256K36	P	--XX	XX	C
SRAM prefix	Operating voltage	Part number, organization	Timing Z=NTD™ timing P=PBSRAM	Access time (ns)	Package: TQ = TQFP B = fBGA	Commercial temperature, 0 ℃ to 70 ℃

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