T-75-49

ADVANCE INFORMATION CONDENSED

Am79C940-16/25, Am79C945-16

Media Access Controller for Ethernet (MACE)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Am79C940 integrated with 10BASE-T transceiver and AUI port**
- **Am79C945 optimized for use with external transceivers using AUI**
- **Supports IEEE 802.3/ANSI 8802-3 and Ethernet standards**
- **Low power, CMOS design with sleep mode allows reduced power consumption for critical battery powered applications**
- **84-pin PLCC Package**
- **Modular architecture allows easy tuning to specific applications**
- **High speed, 16-bit synchronous host system interface with 2 or 3 cycles/transfer**
- **Individual 128 byte transmit and receive FIFOs provide increase of system latency and support the following features:**
  - Automatic retransmission with no FIFO reload
  - Automatic receive stripping and transmit padding (individually programmable)
  - Automatic runt packet rejection
  - Automatic deletion of collision frames
- **Direct slave access to all on board configuration/status registers and transmit/receive FIFOs**
- **Direct FIFO read/write access for simple interface to DMA controllers or I/O processors**
- **Arbitrary byte alignment and little/big endian memory interface supported**
- **Internal/external loopback capabilities**
- **External Address Detection Interface (EADI™) for external hardware address filtering in bridge/router applications**
- **JTAG Boundary Scan (IEEE 1149.1) test access port interface for board level production test**
- **Integrated Manchester Encoder/Decoder; no requirement for external Serial Interface Adaptor (SIA)**
- **Digital Attachment Interface (DAI™) allows by-passing of differential Attachment Unit Interface (AUI)**
- **Supports the following types of network interface:**
  - AUI to external 10BASE2, 10BASE5, 10BASE-T or 10BASE-F MAU
  - DAI to external 10BASE-T or 10BASE-F MAU
  - GPSI to external encoding/decoding scheme
  - Internal 10BASE-T transceiver (Am79C940 only) with automatic selection of 10BASE-T or AUI port
- **Speed grades available:**
  - Am79C940 with 16 and 25 MHz system clock
  - Am79C945 with 16 MHz system clock

GENERAL DESCRIPTION

The Media Access Controller for Ethernet (MACE) is an 84-pin CMOS VLSI device designed to provide flexibility in customized LAN design. The MACE is specifically designed to address applications where multiple I/O peripherals are present, and a centralized or system specific DMA is required. The high speed, 16-bit synchronous system interface is optimized for an external DMA or I/O processor system, and is similar to many existing peripheral devices, such as SCSI and serial link controllers.

The MACE is a slave register based peripheral. All transfers to and from the system are performed using simple memory or I/O read and write commands. In conjunction with a user defined DMA engine, the MACE provides an IEEE 802.3 interface tailored to a specific application. Its superior modular architecture and versatile system interface allow the MACE to be configured as a stand-alone device or as a connectivity cell incorporated into a larger, integrated system.

Two versions of the MACE are available. The standard version, the Am79C940, provides a complete Ethernet node solution with an integrated 10BASE-T transceiver, and supports 16 MHz and 25 MHz system clocks. The condensed version of the MACE, the Am79C945, is similar to the standard version but without the integrated 10BASE-T transceiver, and supports a 16 MHz system clock. Both the Am79C940 and the Am79C945 embody the Media Access Control (MAC) and Physical Layer Signaling (PLS) sub-layers of the IEEE 802.3 standard, and provide an IEEE defined Attachment Unit Interface (AUI) for coupling to an external Medium Attachment Unit (MAU). The MACE is compliant with 10BASE2, 10BASE5, 10BASE-T, and 10BASE-F transceivers.

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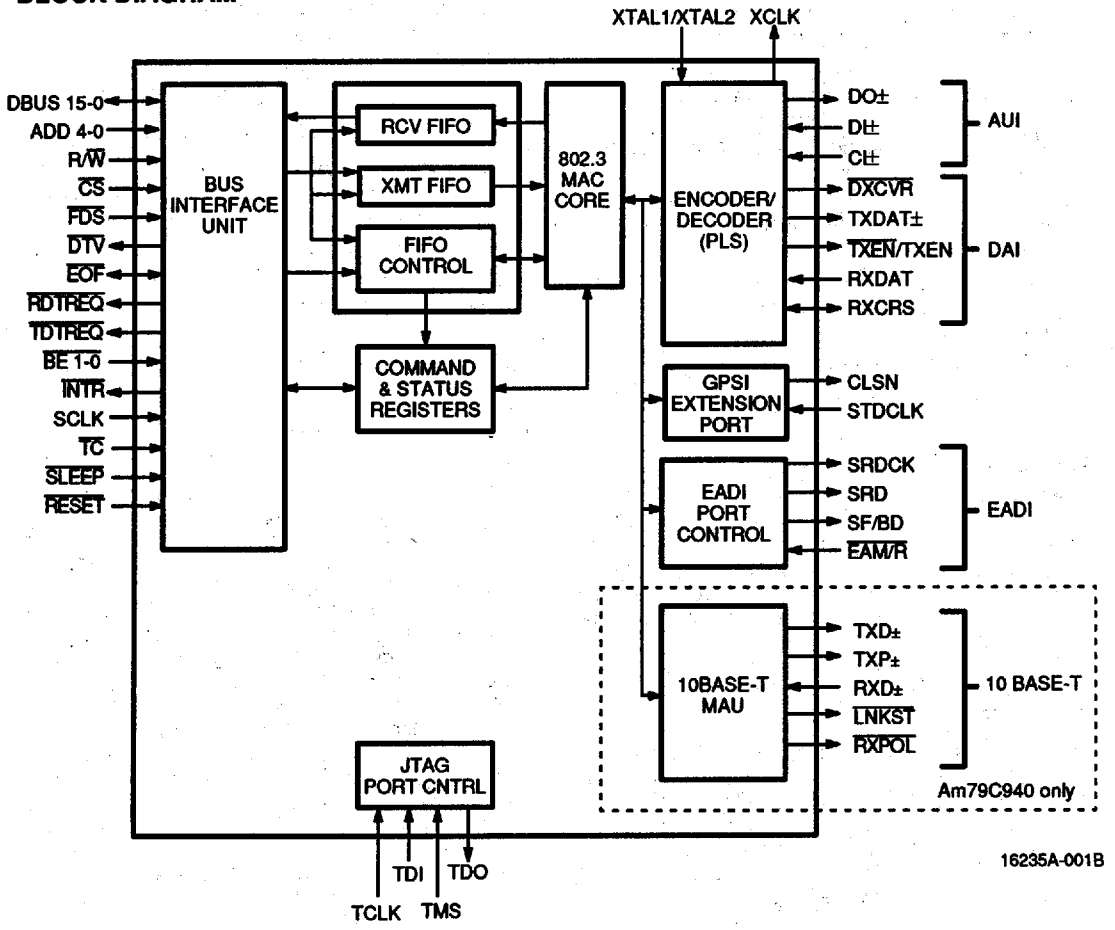
Both versions of the MACE have additional features that enhance over-all system design. The individual 128 byte transmit and receive FIFOs optimize system overhead, providing substantial latency during packet transmission and reception, and minimizing intervention during normal network error recovery. The integrated Manchester encoder/decoder eliminates the need for an external Serial Interface Adapter (SIA) in the node system. If support for an external encoding/decoding scheme is desired, the General Purpose Serial Interface (GPSI) allows direct access to/from the MAC. In addition, the Digital Attachment Interface (DAI), which is a simplified electrical attachment specification, allows implementation of MAUs that do not require DC isolation between the MAU and DTE. The DAI can also be used to indicate transmit, receive, or collision status by connecting LEDs to the port. The MACE also provides an External Address Detection Interface (EADI) to allow external hardware address filtering in internetworking applications.

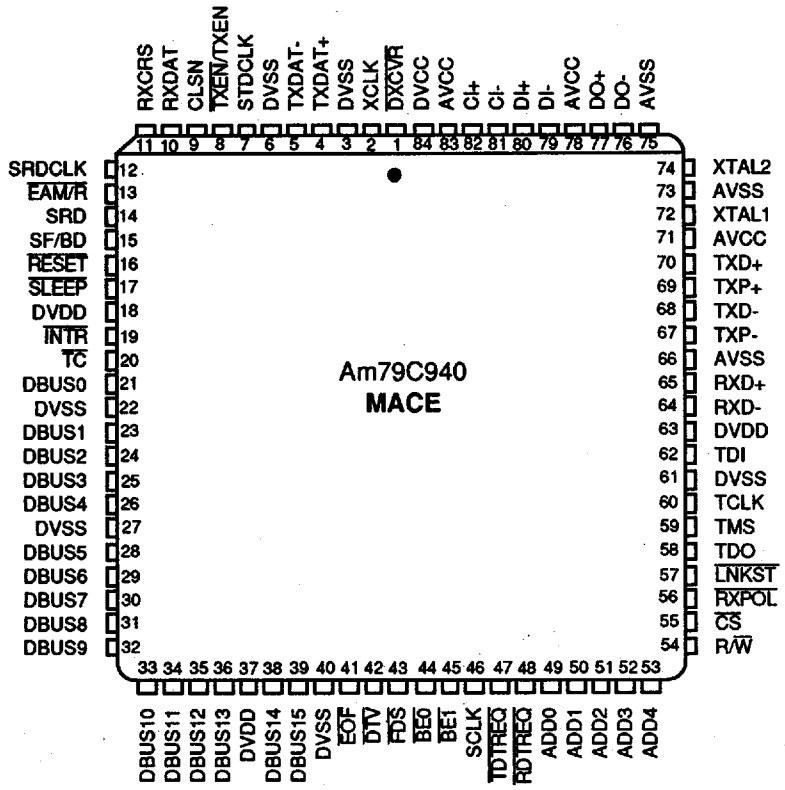
RELATED PRODUCTS

Part No.	Description
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Enhanced Twisted Pair Ethernet Transceiver (TPEX Plus)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am7997	IEEE 802.3 10BASE2/5 Compliant Tap Transceiver
Am79C980	Integrated Multiport Repeater (IMR)

BLOCK DIAGRAM



CONNECTION DIAGRAM



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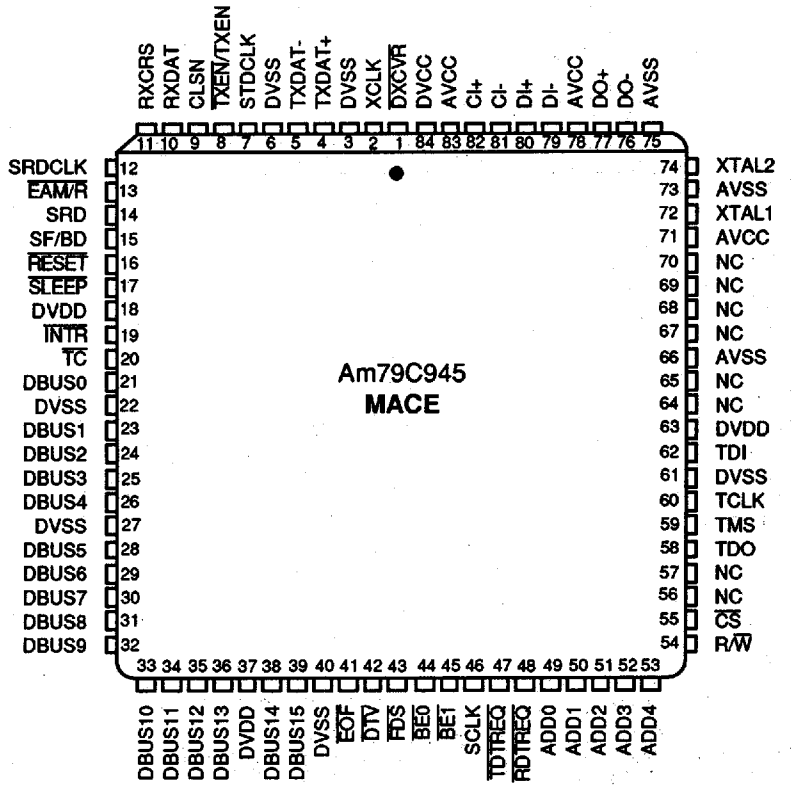
WARNING: The pin-out is subject to change prior to product release. AMD reserves the right to change without notice.

CONNECTION DIAGRAM

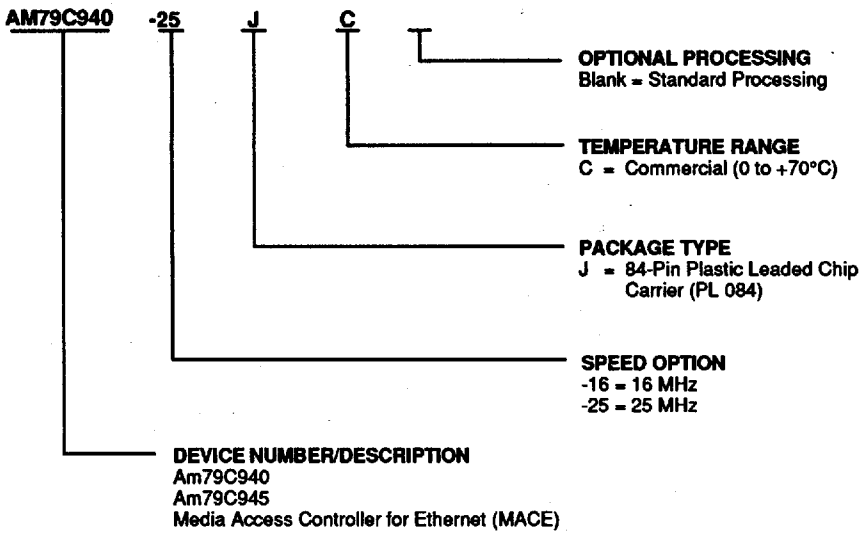


16235A-003A

WARNING: The pin-out is subject to change prior to product release. AMD reserves the right to change without notice.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:



Valid Combinations	
AM79C940-16 AM79C940-25 AM79C945-16	JC

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN SUMMARY

Pin Name	Pin Function	Type
Attachment Unit Interface (AUI)		
DO+/DO–	Data Out	O
DI+/DI–	Data In	I
CI+/CI–	Control In	I
Digital Attachment Interface (DAI)		
TXDAT+	Transmit Data +	O
TXDAT–	Transmit Data –	O
$\overline{\text{TXEN}}$/TXEN	Transmit Enable	O
RXDAT	Receive Data	I
RXCRS	Receive Carrier Sense	I/O
$\overline{\text{DXCVR}}$	Disable Transceiver	O
General Purpose Serial Interface (GPSI) Extension		
STDCLK	Serial Transmit Data Clock	O
CLSN	Collision	I/O
External Address Detection Interface (EADI)		
SF/BD	Start Frame/Byte Delimiter	O
SRD	Serial Receive Data	O
$\overline{\text{EAM}}$/$\overline{\text{R}}$	External Address Match/Reject	I
SRDCLK	SRD Clock	O
System Interface		
$DBUS_{15-0}$	Data Bus	I/O
ADD_{4-0}	Address	I
R/$\overline{\text{W}}$	Read/Write	I
$\overline{\text{RDTREQ}}$	Receive Data Transfer Request	O
$\overline{\text{TDTREQ}}$	Transmit Data Transfer Request	O
$\overline{\text{DTV}}$	Data Transfer Valid	O
$\overline{\text{FDS}}$	FIFO Data Strobe	I
$\overline{\text{EOF}}$	End Of Frame	I/O
$\overline{\text{BE0}}$	Byte Enable 0	I
$\overline{\text{BE1}}$	Byte Enable 1	I
$\overline{\text{CS}}$	Chip Select	I
$\overline{\text{INTR}}$	Interrupt	O
$\overline{\text{RESET}}$	Reset	I
SCLK	System Clock	I
$\overline{\text{TC}}$	Timing Control	I
IEEE 1149.1 Test Access Port (TAP) Interface		
TCLK	Test Clock	I
TMS	Test Mode Select	I
TDI	Test Data Input	I
TDO	Test Data Out	O

PIN SUMMARY (Continued)

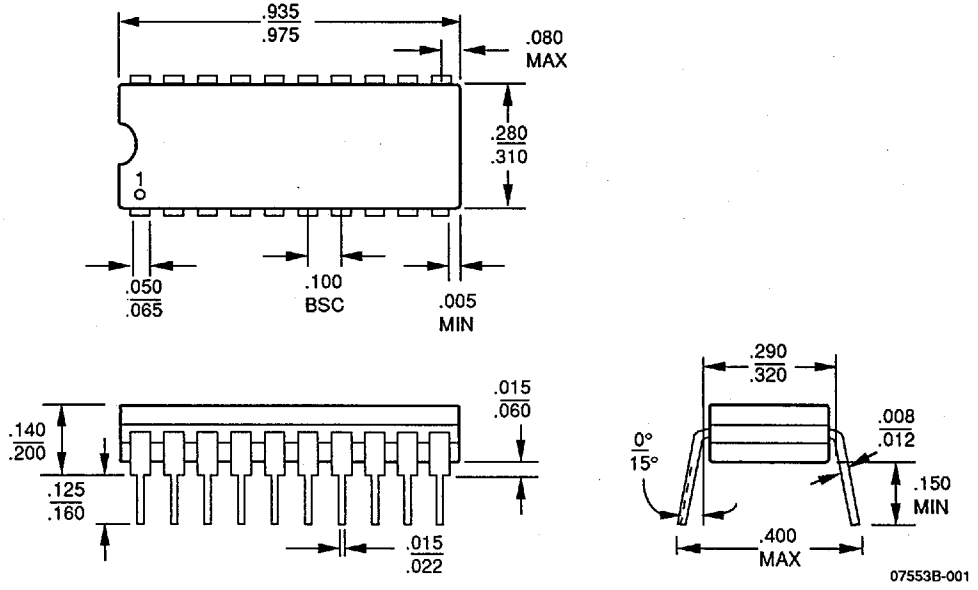
Pin Name	Pin Function	Type
General Interface		
XTAL1	Crystal Input	I
XTAL2	Crystal Output	O
XCLK	Crystal Clock	O
$\overline{\text{SLEEP}}$	Sleep Mode	I
DV_{DD}	Digital Power (4 pins)	P
DV_{SS}	Digital Ground (6 pins)	P
AV_{DD}	Analog Power (3 pins)	P
AV_{SS}	Analog Ground (3 pins)	P
Twisted Pair Transceiver Interface (10BASE-T) Am79C940 only		
TXD+/TXD–	Transmit Data	O
TXP+/TXP–	Transmit Pre-Distortion	O
RXD+/RXD–	Receive Data	I
$\overline{\text{LNKST}}$	Link Status	O
$\overline{\text{RXPOL}}$	Receive Polarity	O

SECTION 5

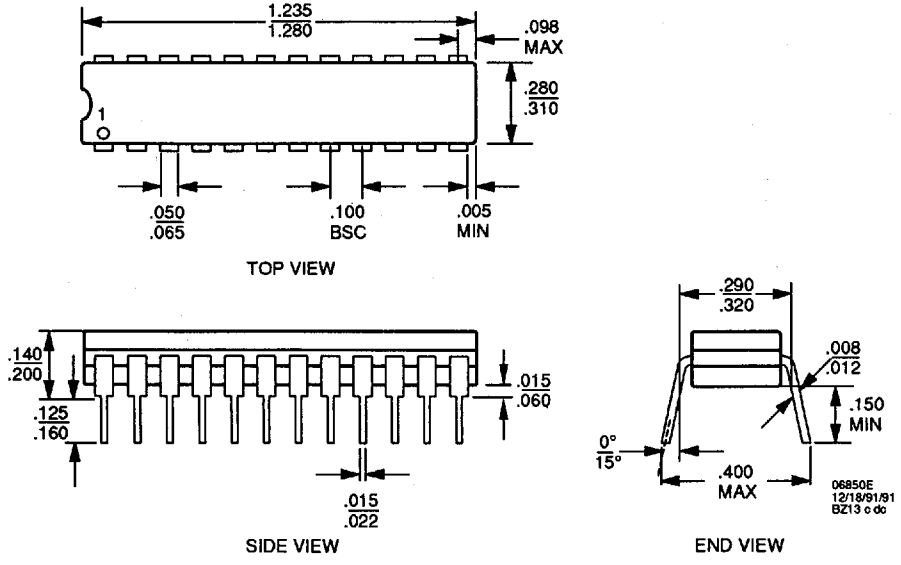
T-90-20

Physical Dimensions

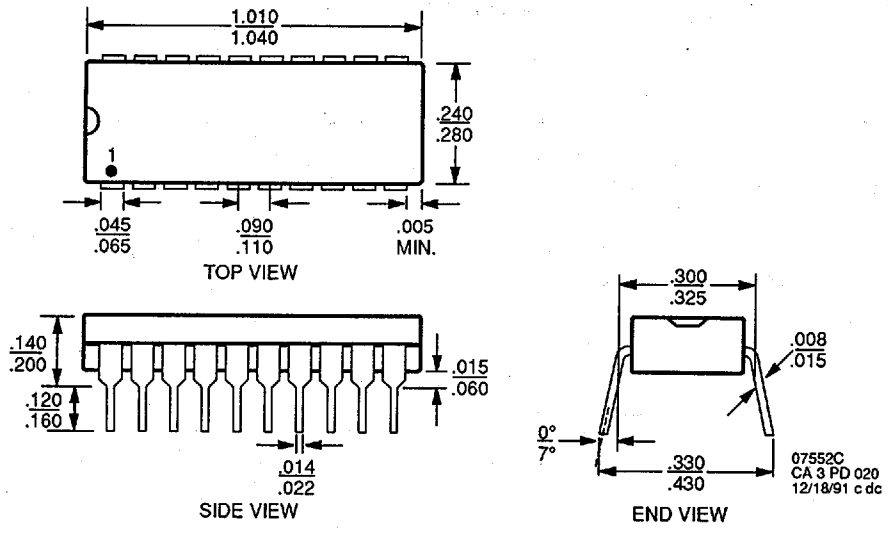
CD 020
20-Pin Ceramic DIP



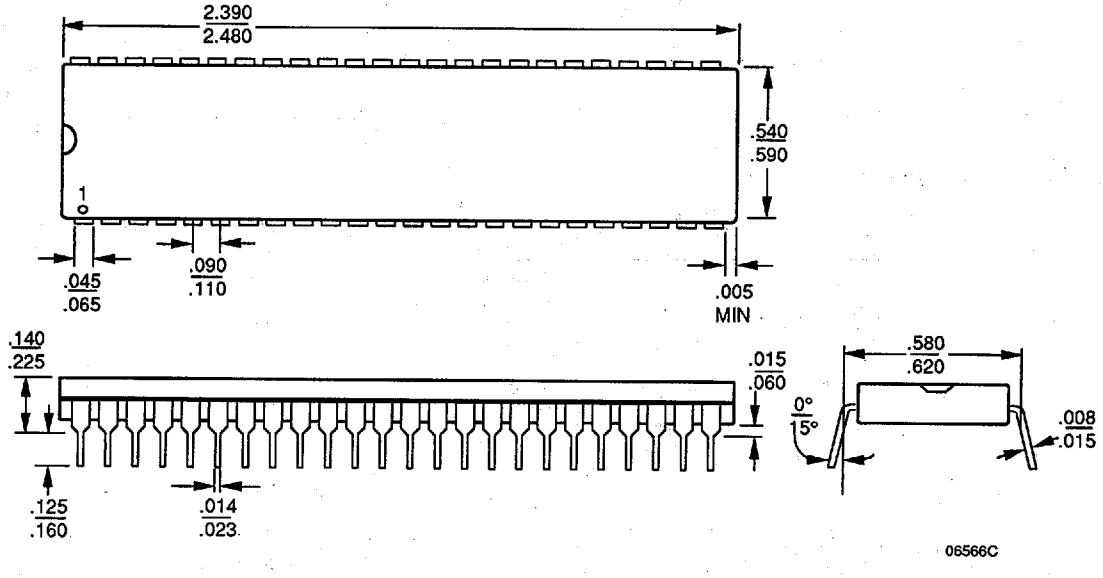
CD3024
24-Pin (Slim) Ceramic DIP



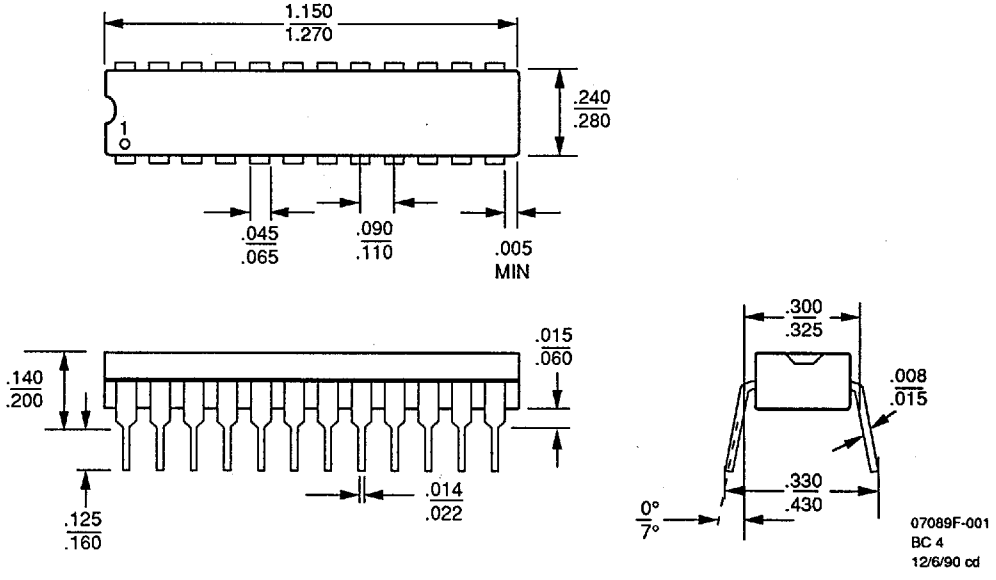
PD 020
20-Pin Plastic DIP



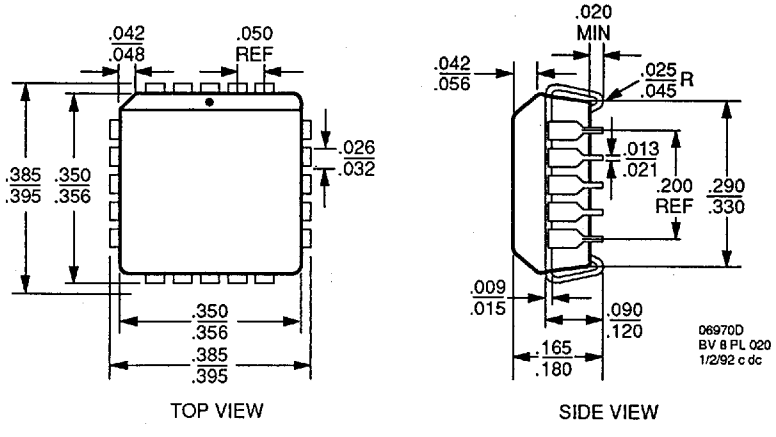
PD 048
48-Pin Plastic DIP



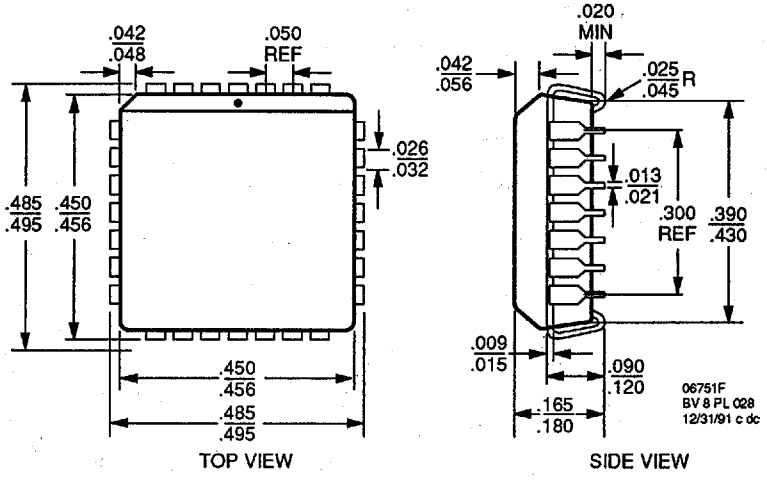
PD3024
24-Pin (Slim) Plastic DIP



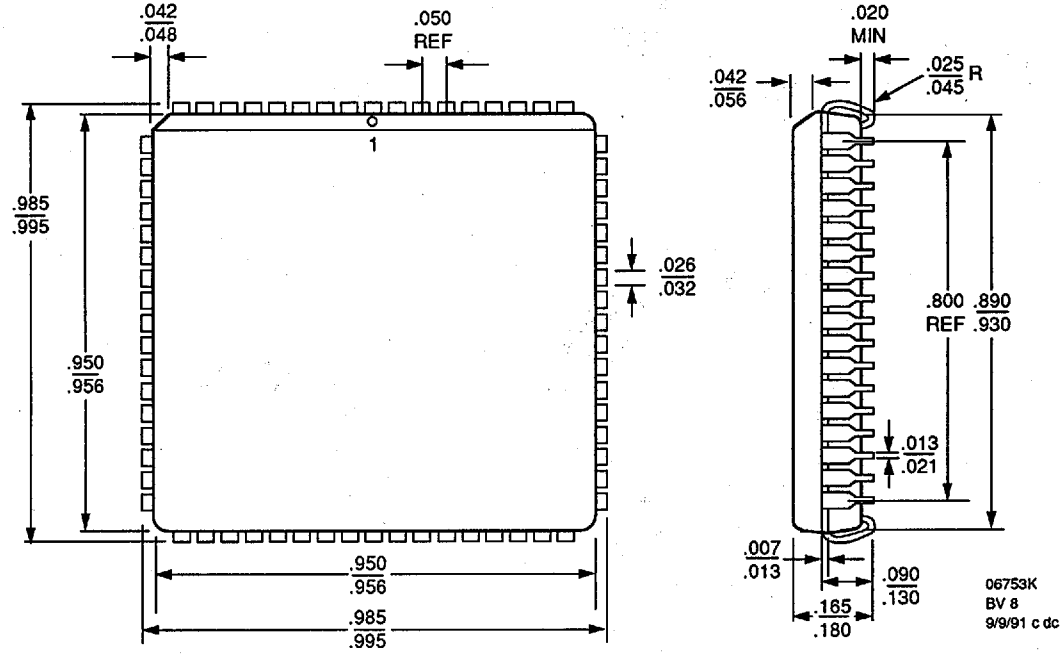
PL 020
20-Pin Plastic Leaded Chip Carrier



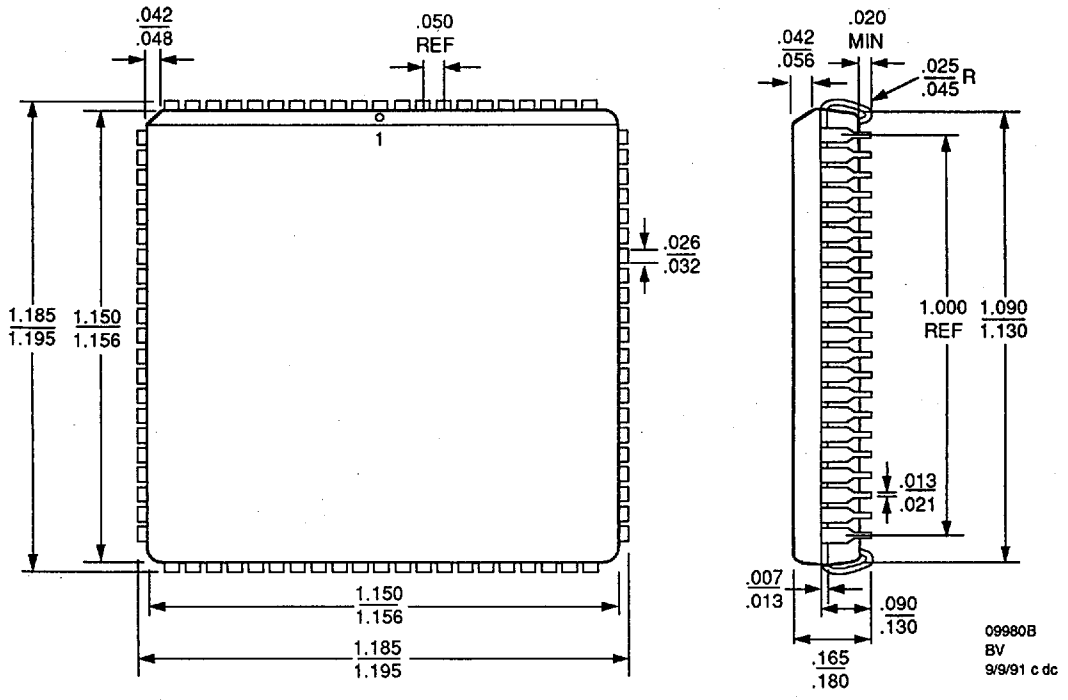
PL 028
28-Pin Plastic Leaded Chip Carrier



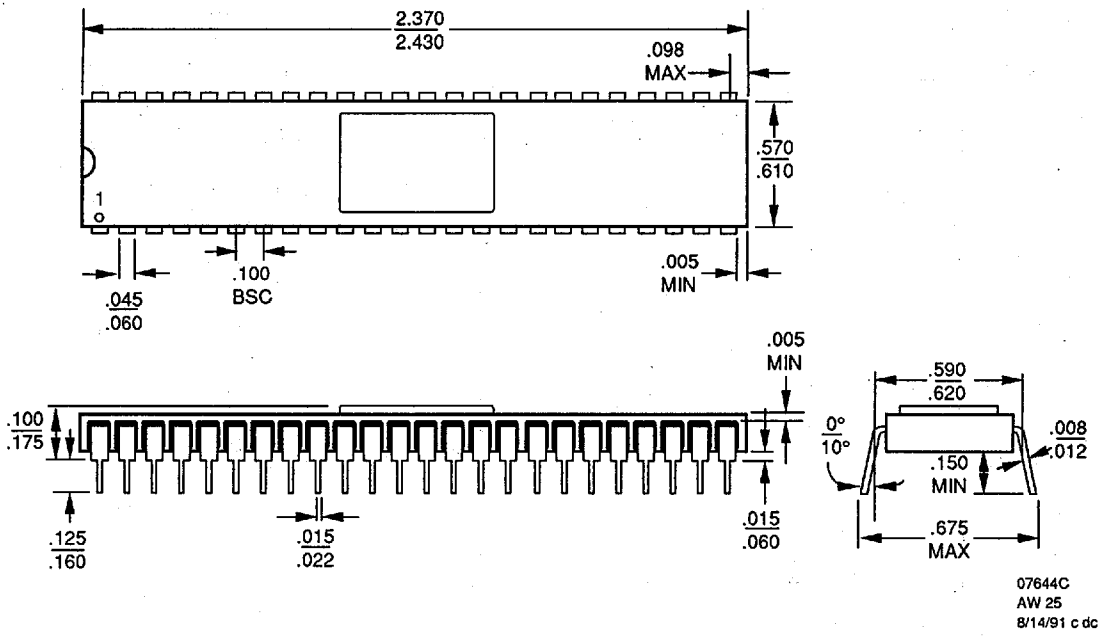
PL 068
68-Pin Plastic Leaded Chip Carrier



PL 084
84-Pin Plastic Leaded Chip Carrier



SD 048
48-Pin Sidebrazed Ceramic DIP



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